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Development of FTK Architecture: A Fast Hardware Track Trigger for the ATLAS Detector

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As the LHC luminosity is ramped up to the design level of 10ˆ34 cm−2 s−1 and beyond, the high rates, multiplicities, and energies of particles seen by the detectors will pose a unique challenge. Only a tiny fraction of the produced collisions can be stored on tape and immense real-time data reduction is needed. An effective trigger system must maintain high trigger efficiencies for the physics we are most interested in, and at the same time suppress the enormous QCD backgrounds. This requires massive computing power to minimize the online execution time of complex algorithms. A multi-level trigger is an effective solution for an otherwise impossible problem.

The Fast Tracker (FTK)[1], [2] is a proposed upgrade to the current ATLAS trigger system that will operate at full Level-1 output rates and provide high quality tracks reconstructed over the entire detector by the start of processing in Level-2. FTK solves the combinatorial challenge inherent to tracking by exploiting massive parallelism of associative memories that can compare inner detector hits to millions of pre-calculated patterns simultaneously. The tracking problem within matched patterns is further simplified by using pre-computed linearized fitting constants and leveraging fast DSP's in modern commercial FPGA's. Overall, FTK is able to compute the helix parameters for all tracks in an event and apply quality cuts in approximately one millisecond. By employing a pipelined architecture, FTK is able to continuously operate at Level-1 rates without deadtime.

The system design is defined and studied with respect to high-Pt Level-2 objects: b-jets, tau-jets, and isolated leptons. We test FTK algorithms using ATLAS full simulation with WH events at the LHC design luminosity. The reconstruction quality is evaluated comparing FTK results with the tracking capability of an offline tracking algorithm. Finally, we compare several architectural choices to optimize the latency and hardware system size.

References

[1] A. Annovi et al. The fast tracker processor for hadronic collider triggers. IEEE Transactions on Nuclear Science, 48:575–580, 2001.

[2] A. Annovi et al. Hadron collider triggers with high-quality tracking at very high event rates. IEEE Transactions on Nuclear Science, 51:391–400, 2004.

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