

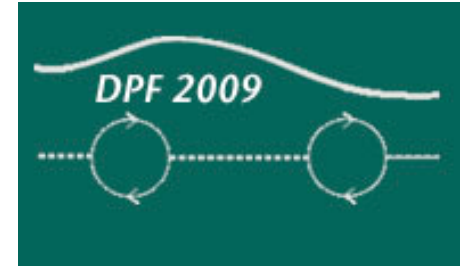
Optical Link ASICs for LHC Upgrades

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The Ohio State University

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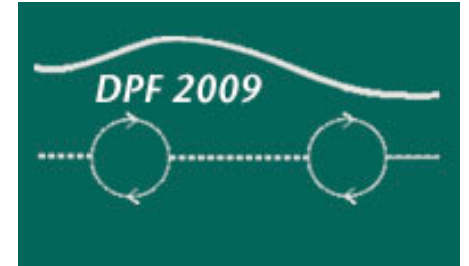
Outline



- Introduction
- VCSEL driver chip
- PIN receiver/decoder chip
- Clock multiplier
- Summary



Introduction

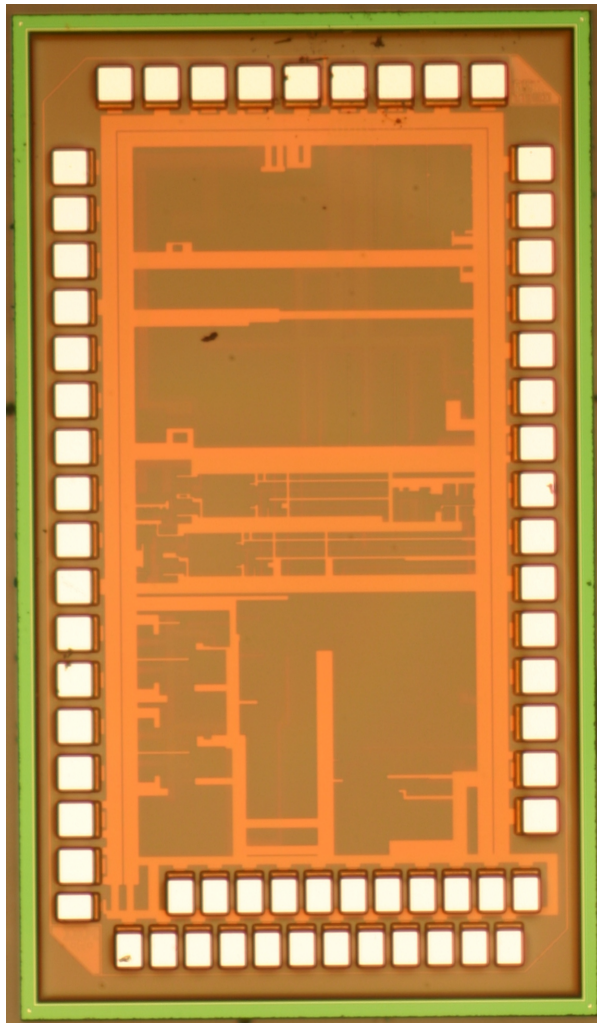


- 1st phase of LHC upgrade is planned for 2014:
 - ◆ 3 times increase in luminosity to $3 \times 10^{34} \text{ cm}^{-2} \text{ s}^{-1}$
 - ◆ expect significant degradation in the ATLAS pixel detector
 - ⇒ add an insertable barrel layer (IBL) at radius of 3.5 cm
- Possible upgrade for on-detector optical readout system for the IBL:
 - ◆ add new functionalities to correct for deficiencies in current system
 - ◆ upgrade current optical chips to run at higher speed
 - ◆ some of the development could be of interest to SLHC upgrade
 - ◆ use 130 nm CMOS 8RF process
 - ◆ prototype chips received/irradiated in July/August 2008
 - ⇒ results will be presented below



Opto-Chips

DPF 2009

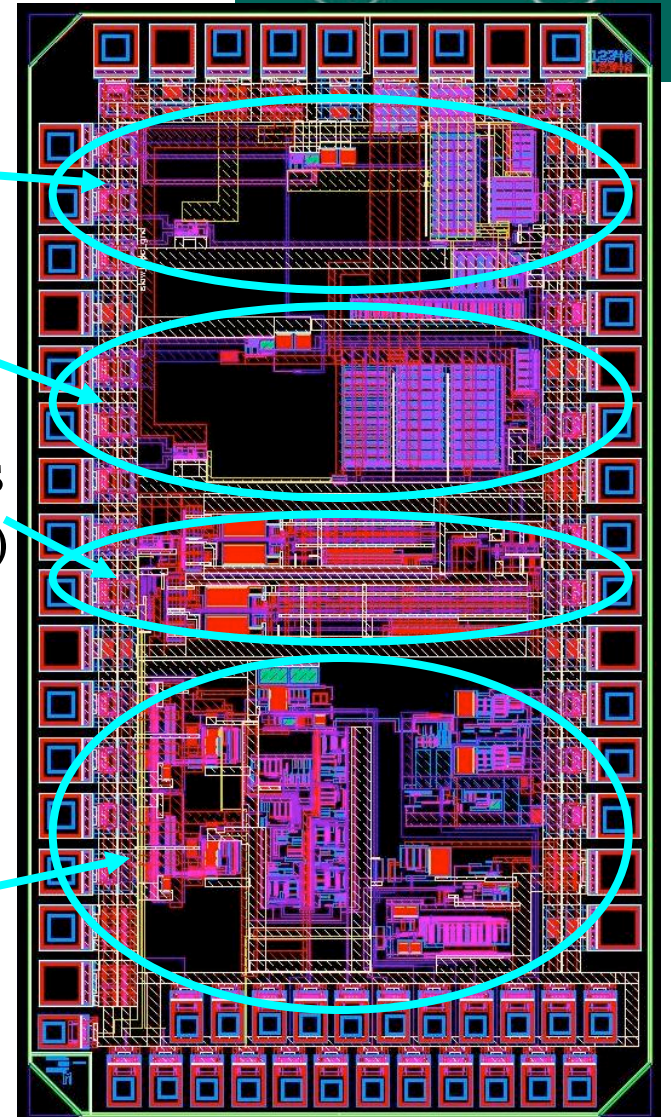


640 Mb/s VCSEL driver

3.2 Gb/s VCSEL driver

640 MHz clock multipliers
(4 x 160 and 16 x 40 MHz)

PIN receiver/decoder
(40, 160, 320 Mb/s)



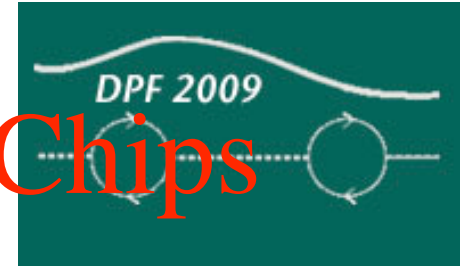
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2.6 mm x 1.5 mm



Testing the 130 nm Opto-Chips



- chips were tested in the lab at Ohio State University
- chips were irradiated with 24 GeV protons to SLHC dose at CERN
 - ◆ 8 VCSEL drivers: 4 “slow” + 4 “fast”
 - ◆ 4 PIN receivers/decoders (purely electrical testing)
 - ◆ 4 PIN receivers/decoders coupled to PIN
 - ◆ 4 clock multipliers
 - ◆ long cables limited testing of drivers/receivers to 40 Mb/s
 - ◆ special designed card allows testing of clock multiplier at 640 MHz

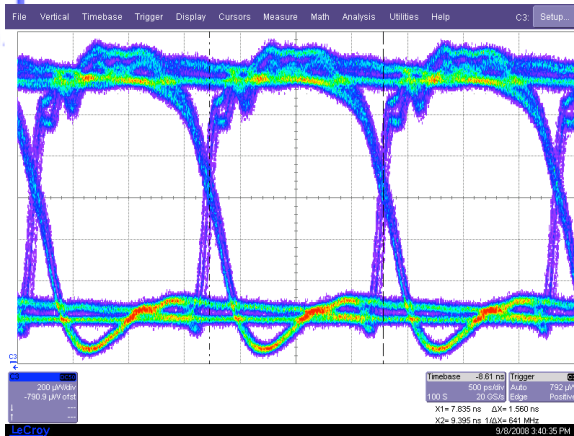
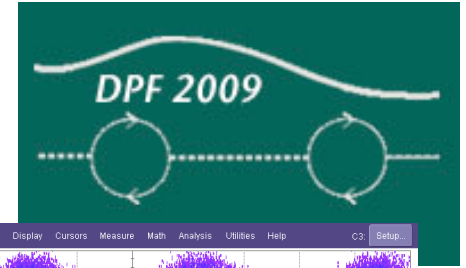


protons

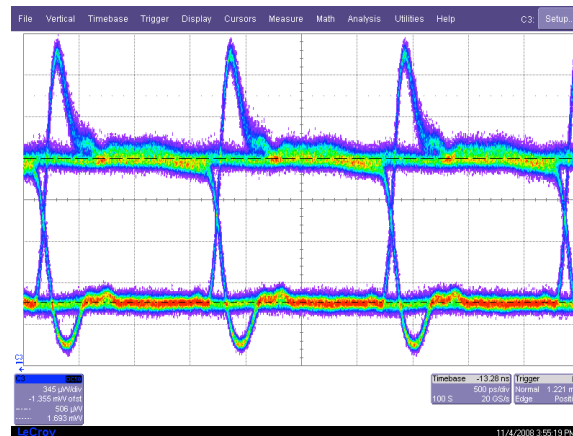
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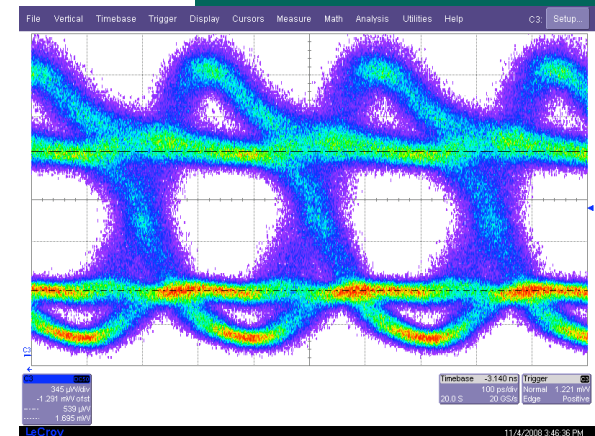
VCSEL Driver Chip



Slow VDC
640 Mb/s
~ 14 mA max



Fast VDC
640 Mb/s
~ 9 mA max

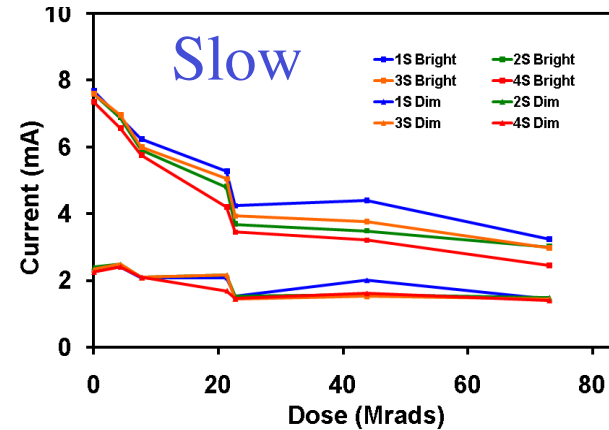
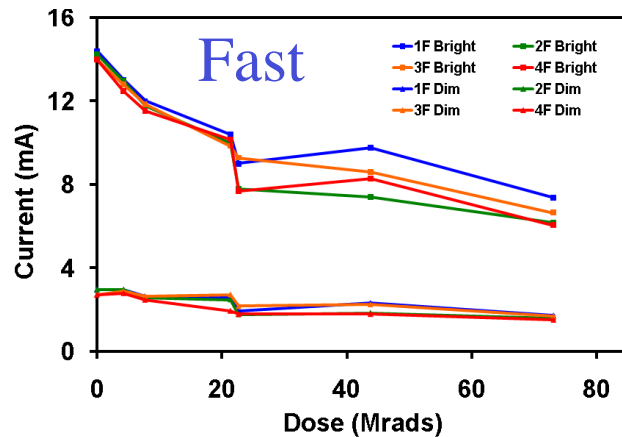
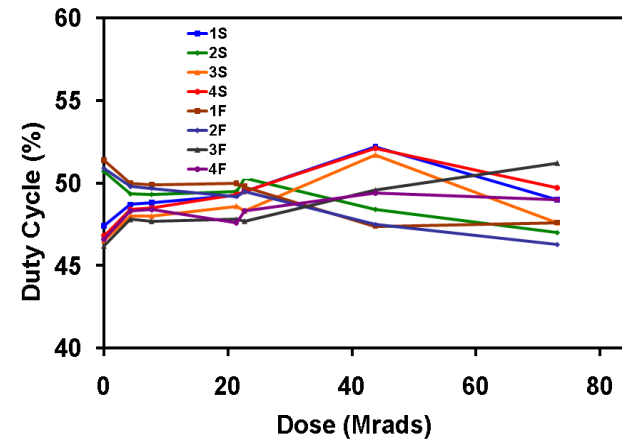
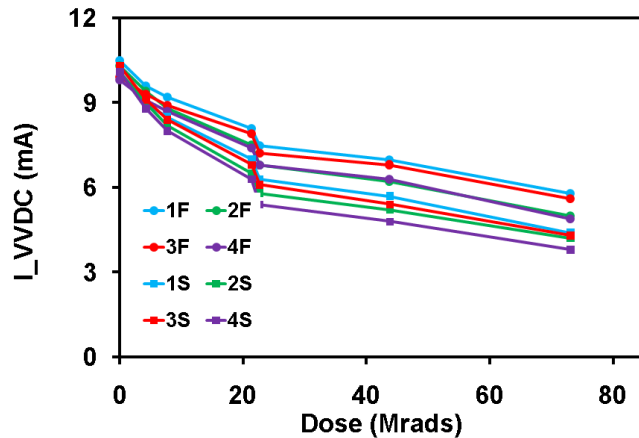
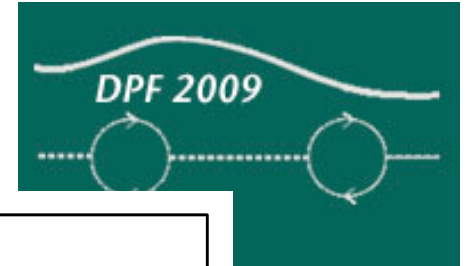


Fast VDC
3.2 Gb/s

- both slow/fast chips are working
- LVDS receiver/VCSEL driver work at high speed
 - ◆ BER < 10^{-13} @ 4 Gb/s using 10 Gb/s AOC VCSEL



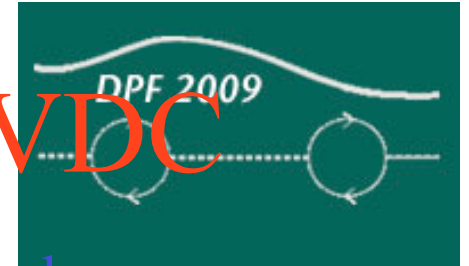
VDC Irradiation



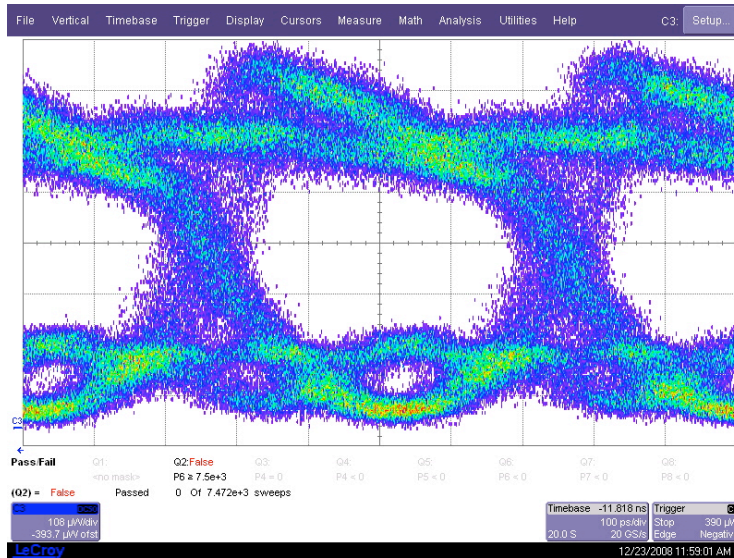
- VDC driving 25Ω with constant control current (I_{set})
- drive current decreases with radiation for constant I_{set}
- ◆ driver circuit fabricated with thick oxide process



Unirradiated vs. Irradiated VDC

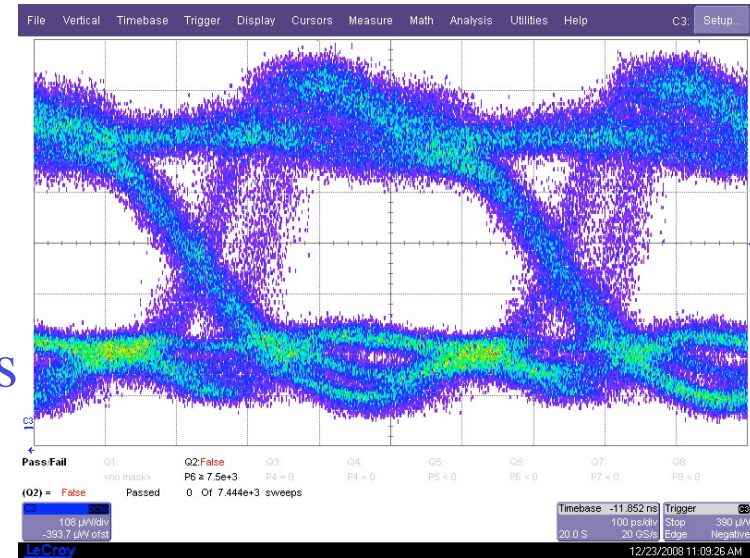


Unirradiated



2 Gb/s

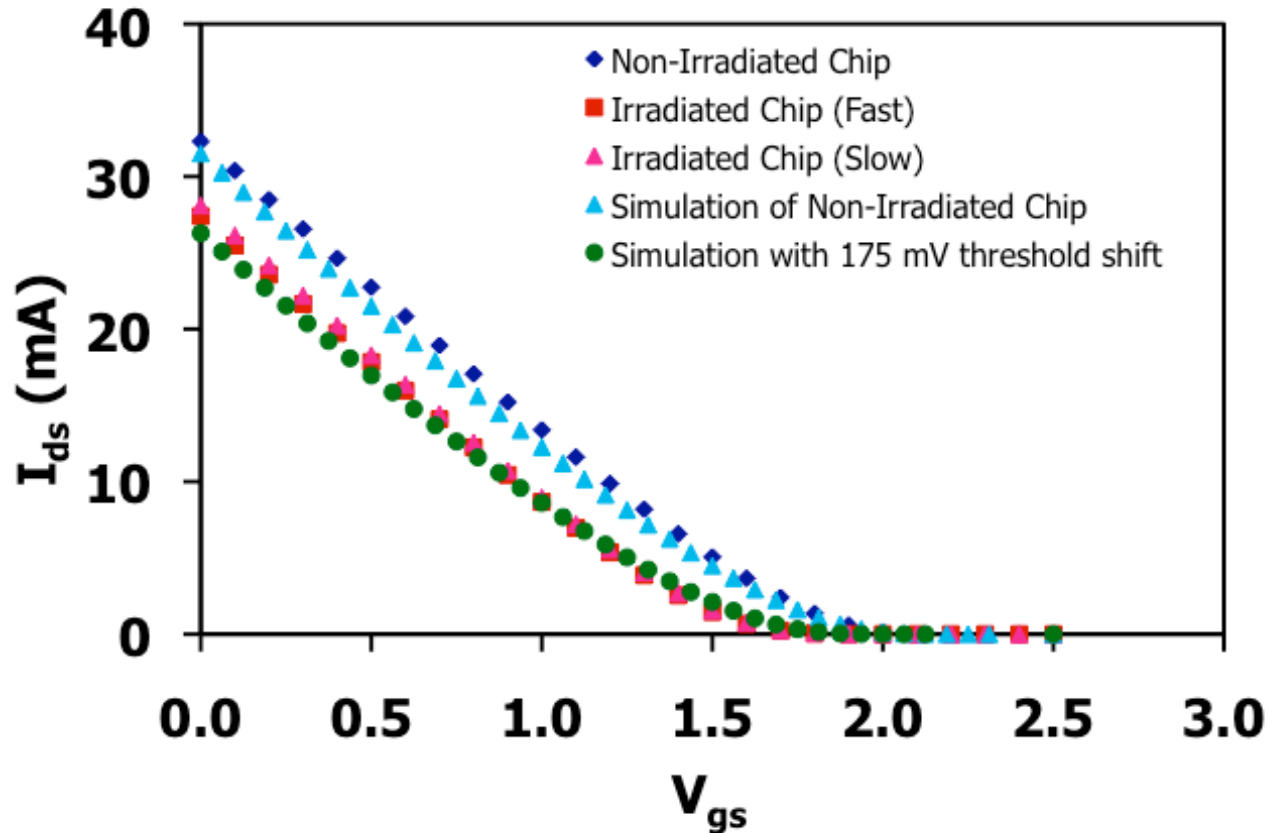
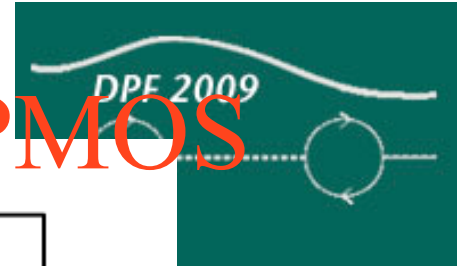
Irradiated



- VDC driving 2.5 Gb/s Optowell VCSEL
- Possible to obtain similar eye diagram by adjusting control currents
 - ◆ radiation induced changes in control current circuitry



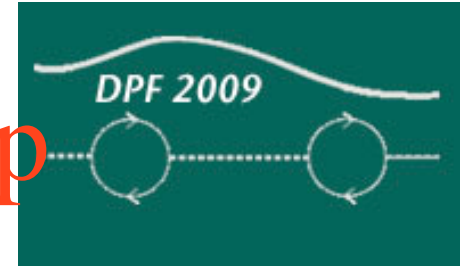
Threshold Shift in Irradiated PMOS



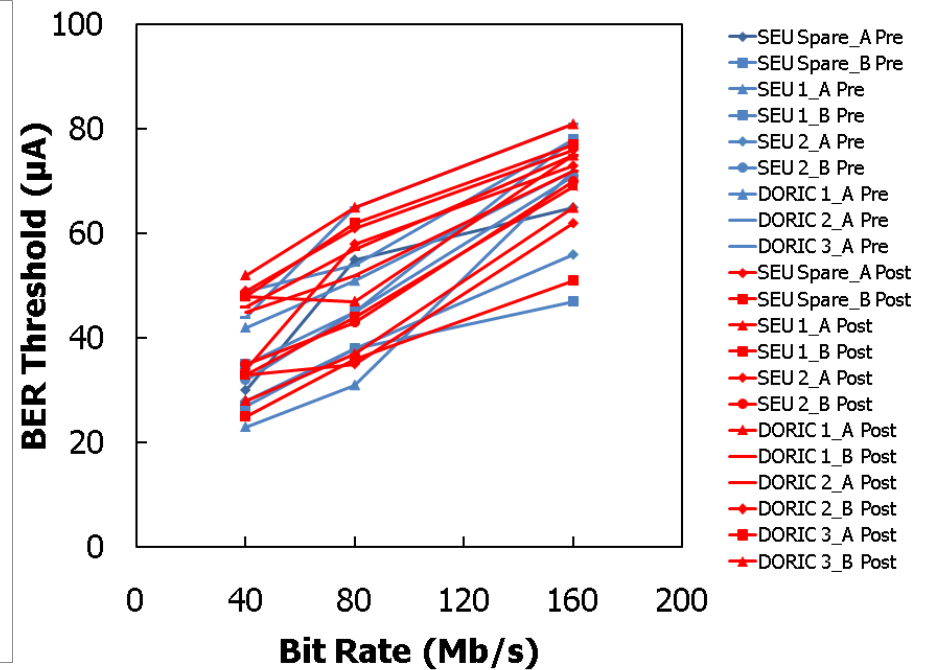
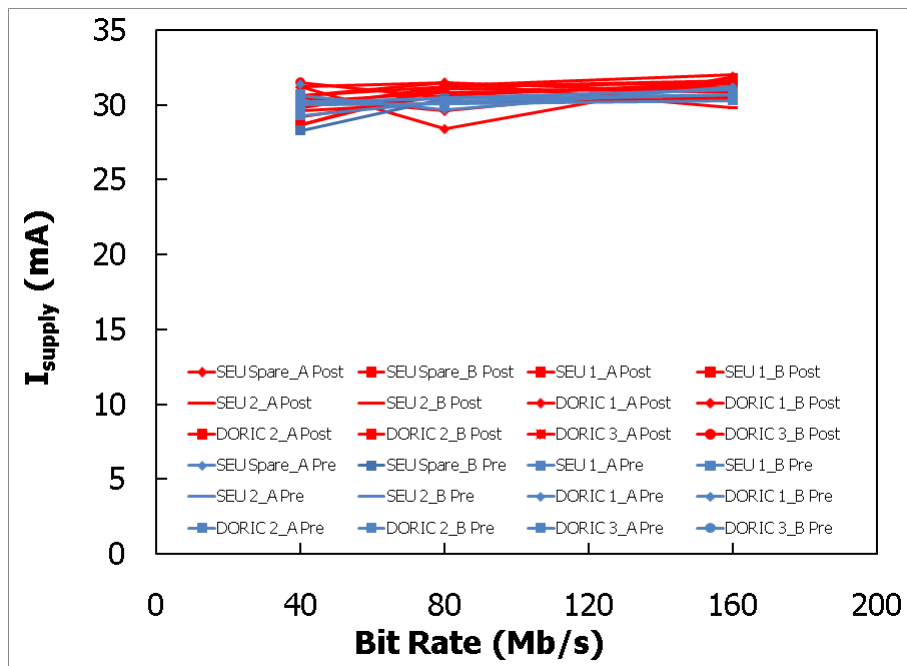
- Have access to two transistors for characterization
 - ◆ simulation with 300 mV threshold shift reproduces observed V vs. I
 - ◆ PMOS and NMOS have different threshold voltage shifts
 - ⇒ will use only PMOS in the current mirror



Receiver/Decoder Chip



- Designed to operate at 40, 160, and 320 Mb/s
 - ◆ achieve only 250 Mb/s due to lack of time for design optimization before submission
 - ◆ no significant degradation up to SLHC dose

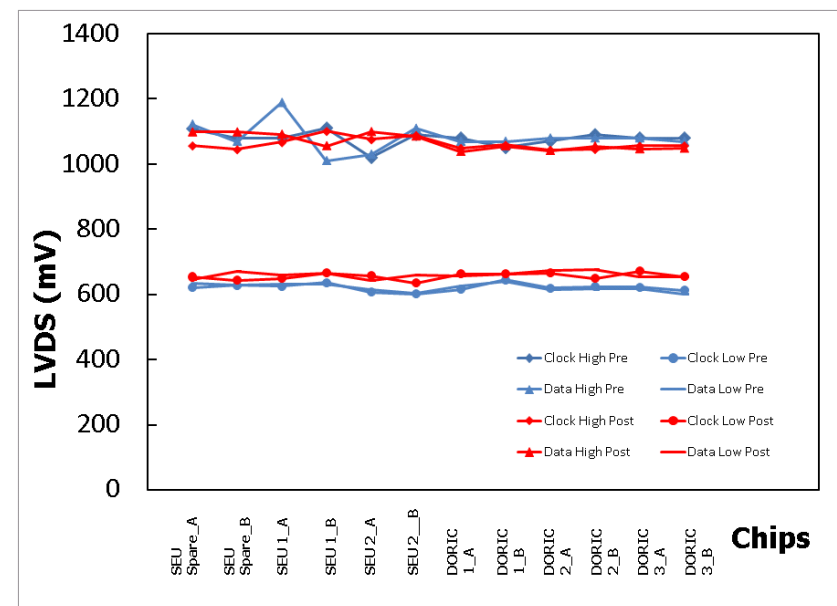
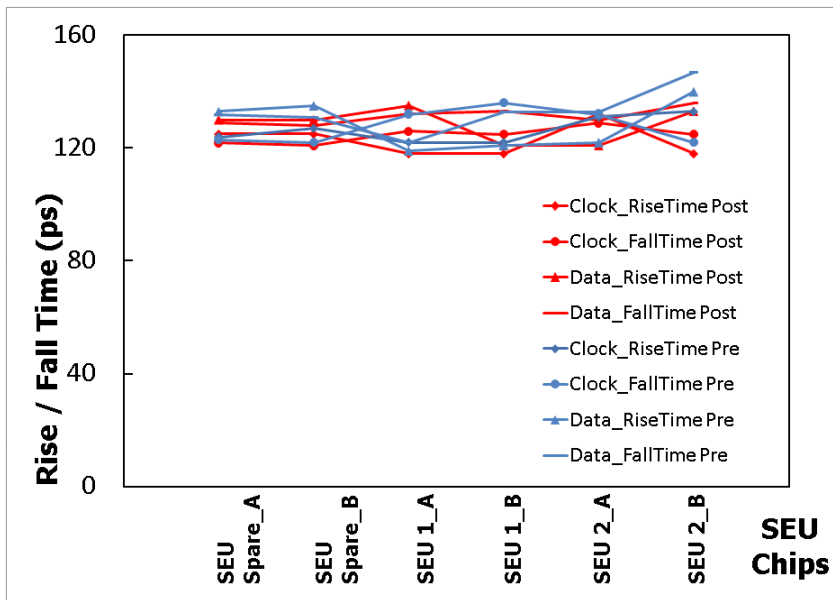




Low Voltage Differential Driver



- output has fast rise and fall times
- output has proper amplitude and baseline
 - ◆ small clock jitter, e.g. < 50 ps (1%) @ 160 MHz
 - ◆ no significant degradation up to SLHC dose

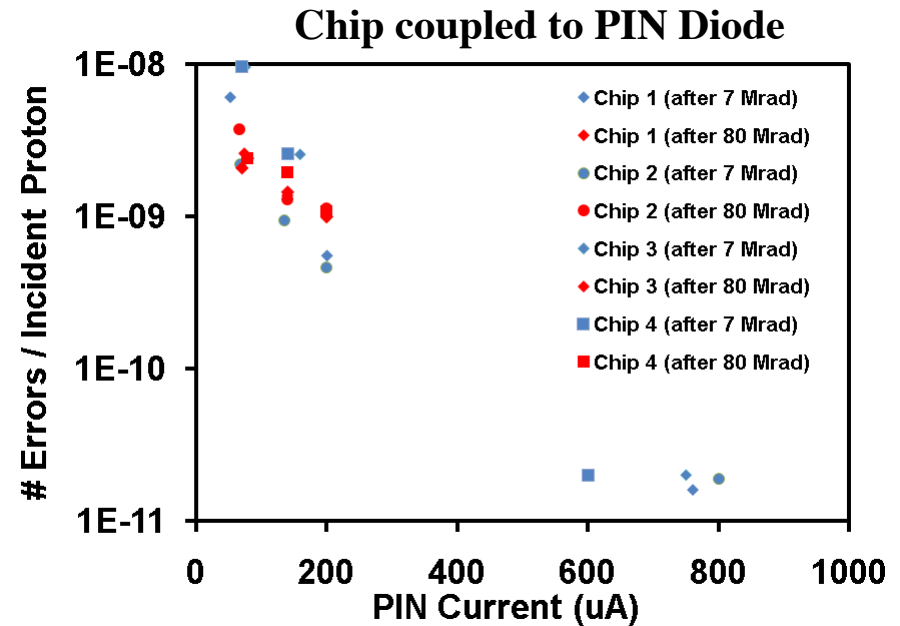
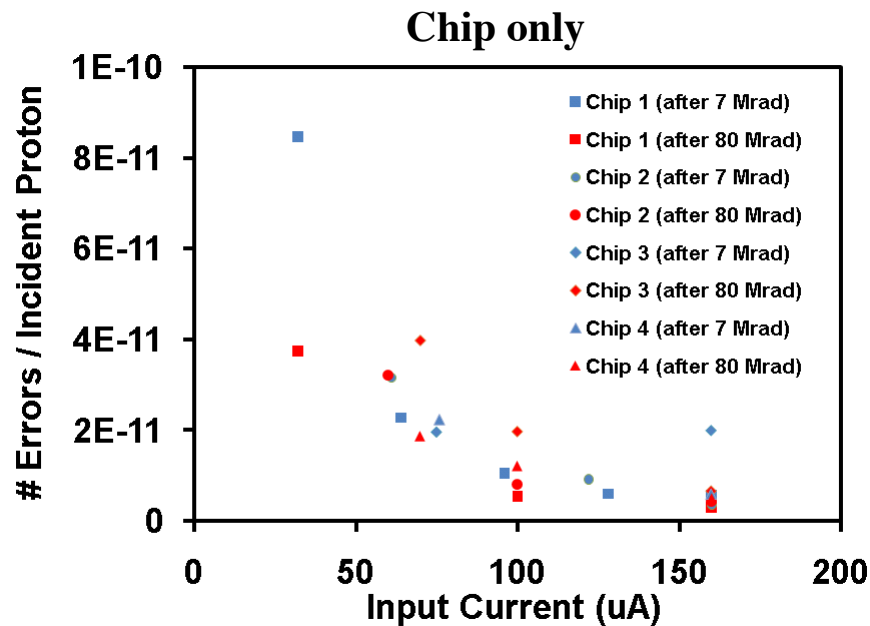




Single Event Upset

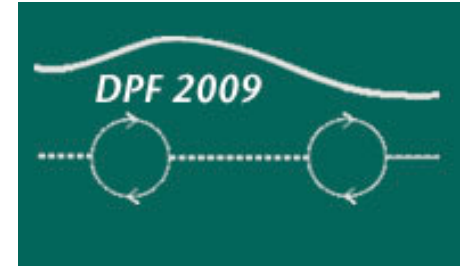


- Single event upset (SEU) measured with receiver/decoder coupled to a Taiwan PIN for 40 Mb/s operation
 - ◆ SEU rate much higher for chip coupled to PIN as expected
 - ◆ no significant degradation with radiation observed

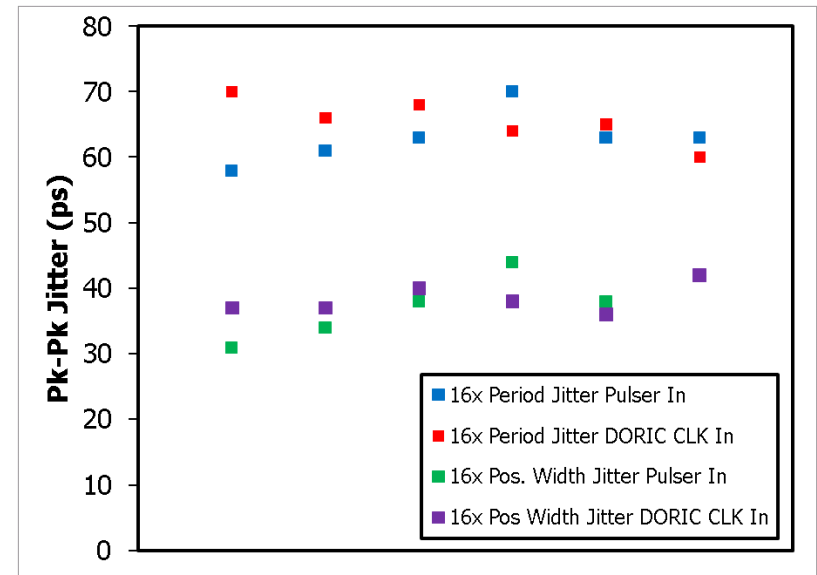
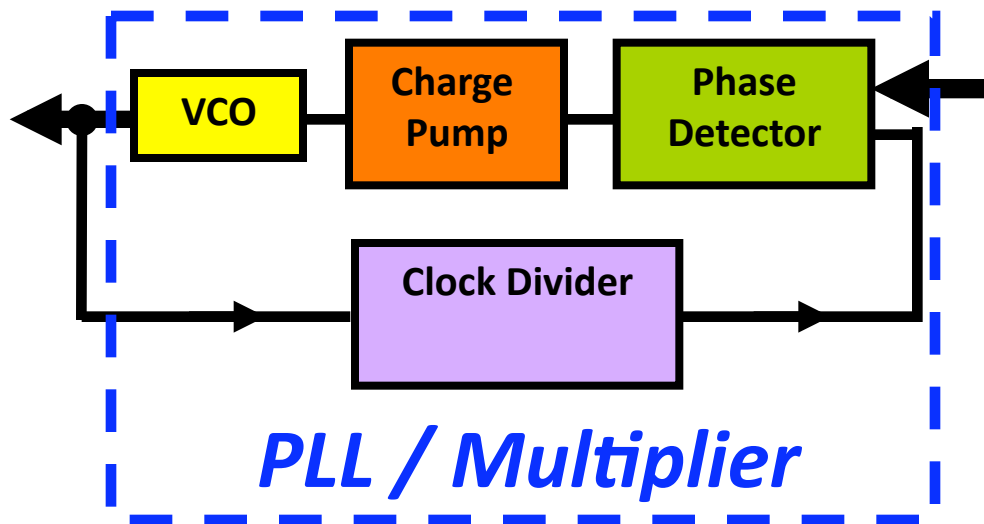




Clock Multiplier

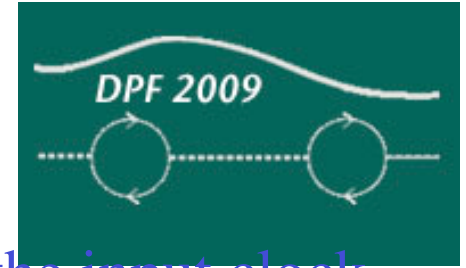


- clock multiplier needed to serialize high speed data
- both 4 x 160 MHz and 16 x 40 MHz clock multipliers work
 - ◆ use of recovered clock as input does not increase jitter

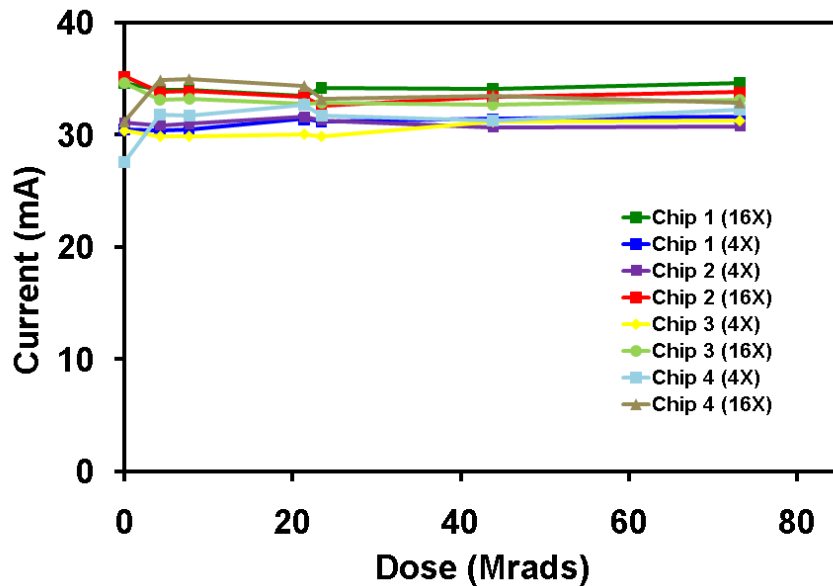




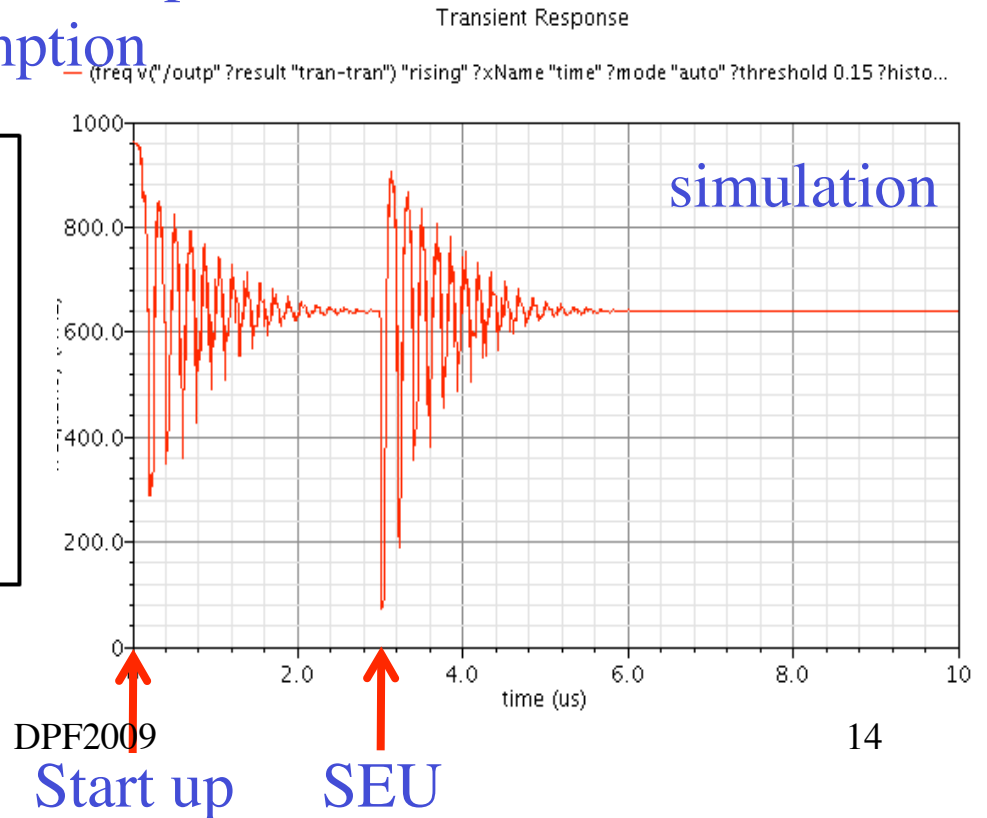
Clock Multiplier



- SEU in PIN coupled to data/clock decoder disturbed the input clock
 - ⇒ observation confirmed with simulation
 - ◆ output clock takes $\sim 3 \mu\text{s}$ to recover
 - ◆ two of the four chips lost lock during irradiation
 - need power cycling to resume operation at 640 MHz
 - ◆ no change in current consumption

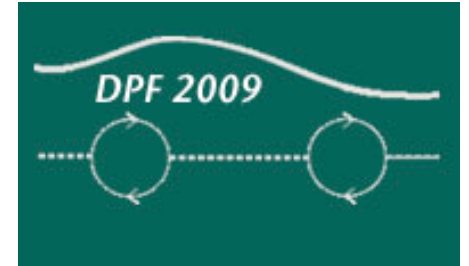


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Summary



- first 130 nm submission mostly successful
- no significant degradation up to 73 Mrad
 - ◆ observe threshold shift in thick oxide transistors
- aim for next iteration in autumn 2009 with new functionalities
 - individual control of VCSEL currents
 - redundancy: ability to bypass a bad VCSEL/PIN channel



Artistic view of an ATLAS SCT Endcap Disk

RD09 9th International Conference
on Large Scale Applications
and Radiation Hardness of
Semiconductor Detectors

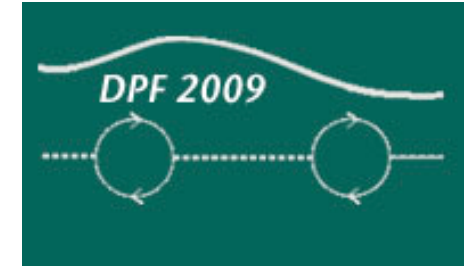
Semiconductor Detectors - Tracking Systems - Radiation Effects and Hardness - Electronics

September 30 - October 2, 2009, Florence, Italy
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