# Fast Timing and TOF in HEP

Henry Frisch
Enrico Fermi Institute, University of Chicago

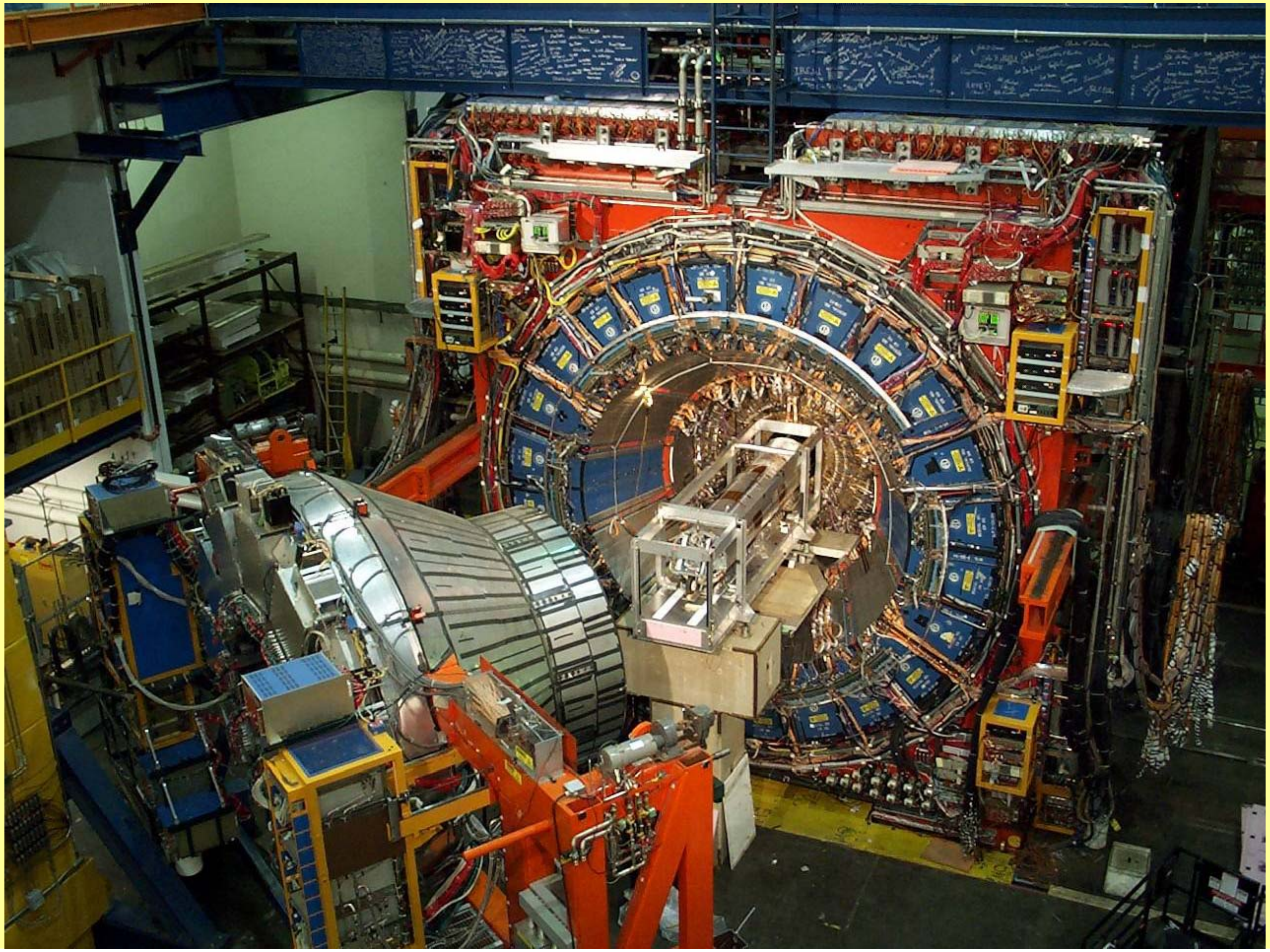
**Long-standing motivation- understanding the basic forces and particles of nature- hopefully reflecting underlying symmetries**

Discoveries:
Top quark

B_s Mixing

Measurements:

Many many many- and many more not done yet



**CDF-1979 to present**

But small compared to Atlas and CMS (tho 5000 tons)

# Fast Timing and TOF in HEP

Henry Frisch
Enrico Fermi Institute, University of Chicago

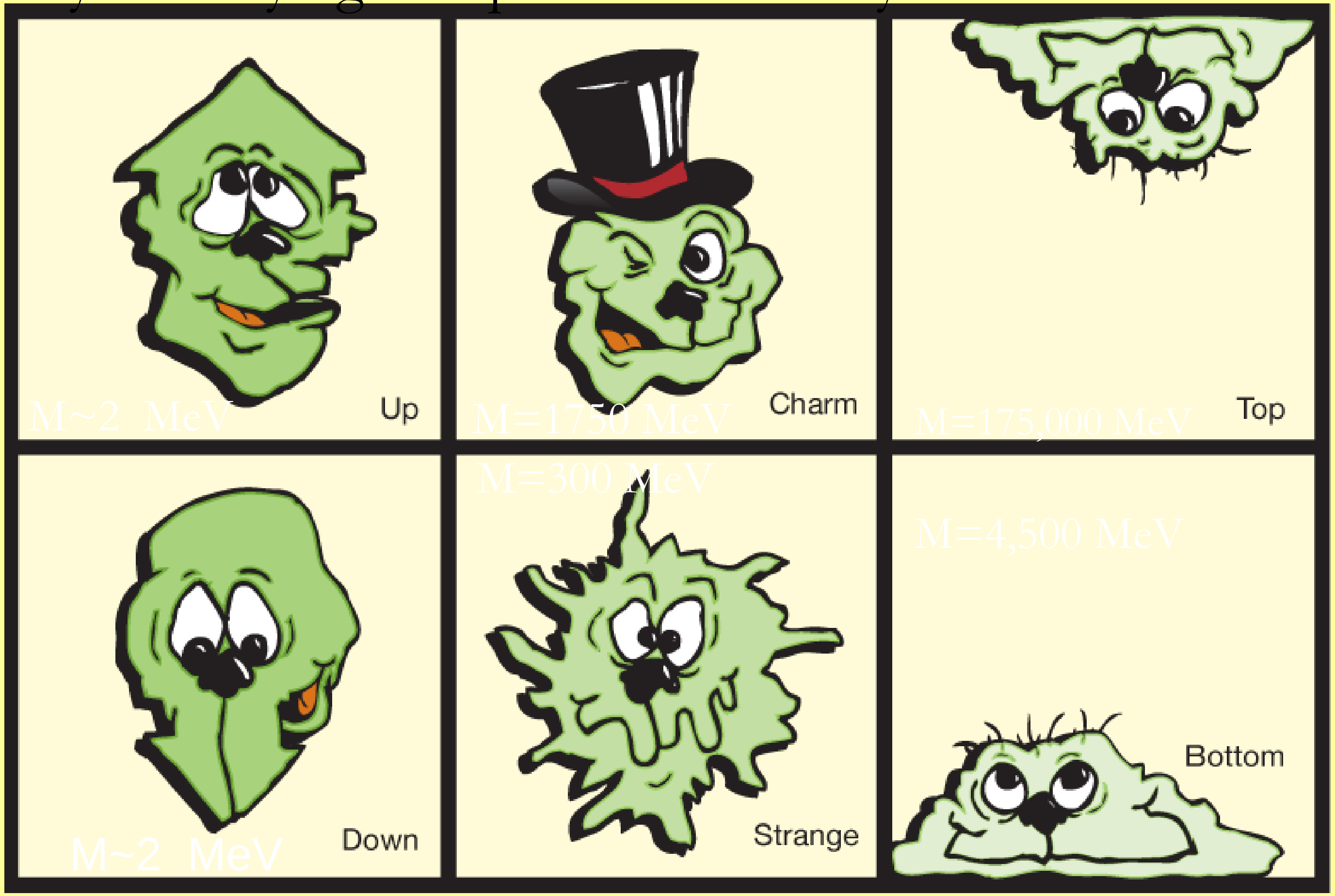
- 1. Moving from the hadron level to the quark level- we measure 3-momenta of hadrons, but can't follow the flavor-flow of quarks.
- 2. Quarks are distinguished by different masses- up and down are light (MeV), strange a few 100 MeV, charm 1.7 GeV, bottom 4.5 GeV, top 170.
- To follow the quarks- 2 direct ways- lifetime (charm,bottom), measuring the mass (strange).
- To measure the mass, measure $\vec{p}$ and $\vec{v}$: ($v=L/\delta t$)

# The unexplained structure of basic building blocks-e.g. quarks

The up and down quarks are light (few MeV), but one can trace the others by measuring the mass of the particles containing them. Different models of the forces and symmetries predict different processes that are distinguishable by identifying the quarks. Hence my own interest.

**Q=2/3**

**Q=-1/3**




Nico Berry (nicoberry.com)

# Fast Timing and TOF in HEP

Henry Frisch
Enrico Fermi Institute, University of Chicago

- I believe that the existence of 'flavor'- up, down, strange, charm, bottom, and top is essential, in the sense that if we can't understand it in a deeper way, we're in the grip of initial conditions rather than fundamental symmetries or principles.
- Disclaimer- View not shared by some (esp. string) theorists-

# 2 TeV (> 3ergs) pbar-p collisions

The Basics- Page 1

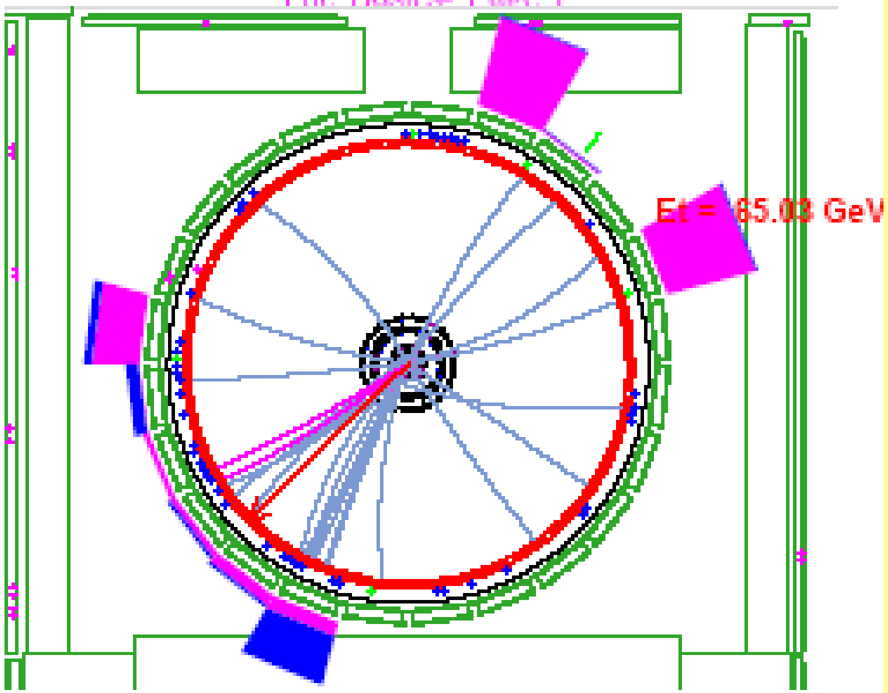



Figure 2:

For each track, $\beta = L/\Delta t$, where $L \equiv$ track length (helix) from vertex to outer radius, and:

$\Delta t$= (time at outer radius $-t_0$), where $t_0$ is the time of interaction.

**Beam's Eye View**

The Basics- Page 2

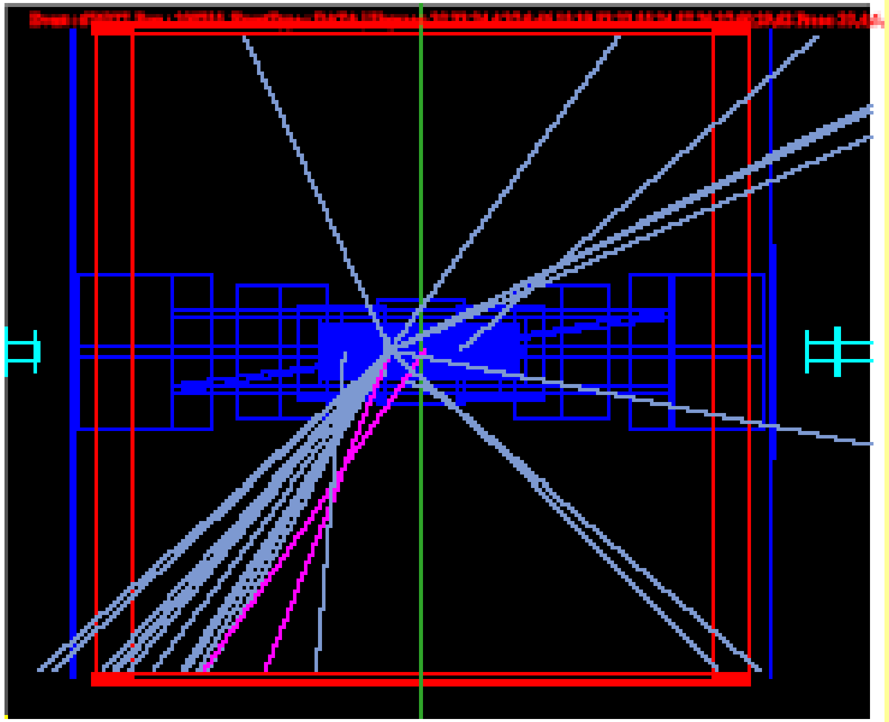


Figure 3:

R-Z (side) view of the same event. Note the mis-reconstructed tracks in this view (no slouch detector-96 layers of COT, 7 or 8 silicon).

**Side View**

# A real CDF Top Quark Event

T-Tbar -> $W^+bW^-$bbar

Measure transit time here (stop)

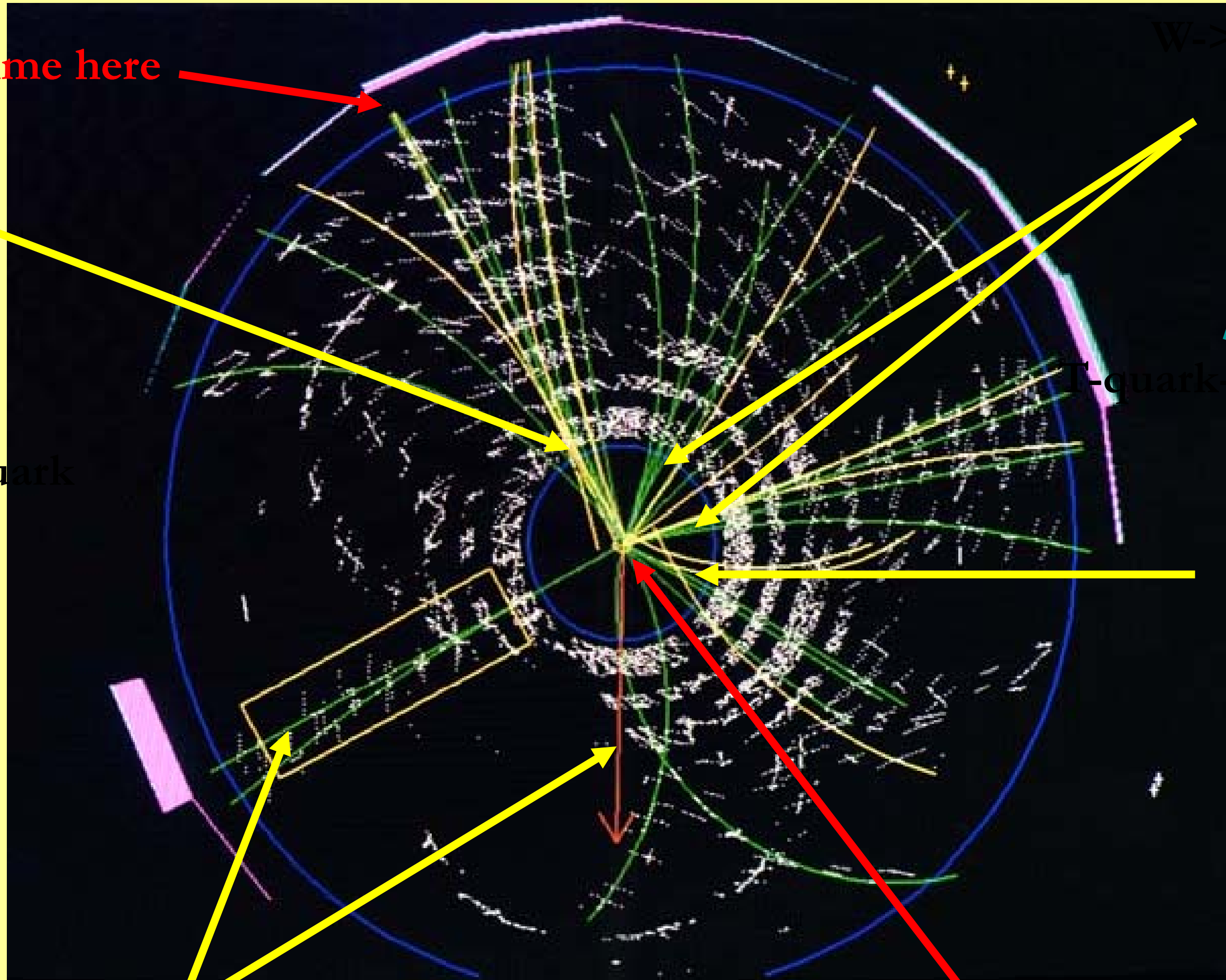
W->charm sbar

B-quark

T-quark->W+bquark

T-quark->W+bquark

B-quark



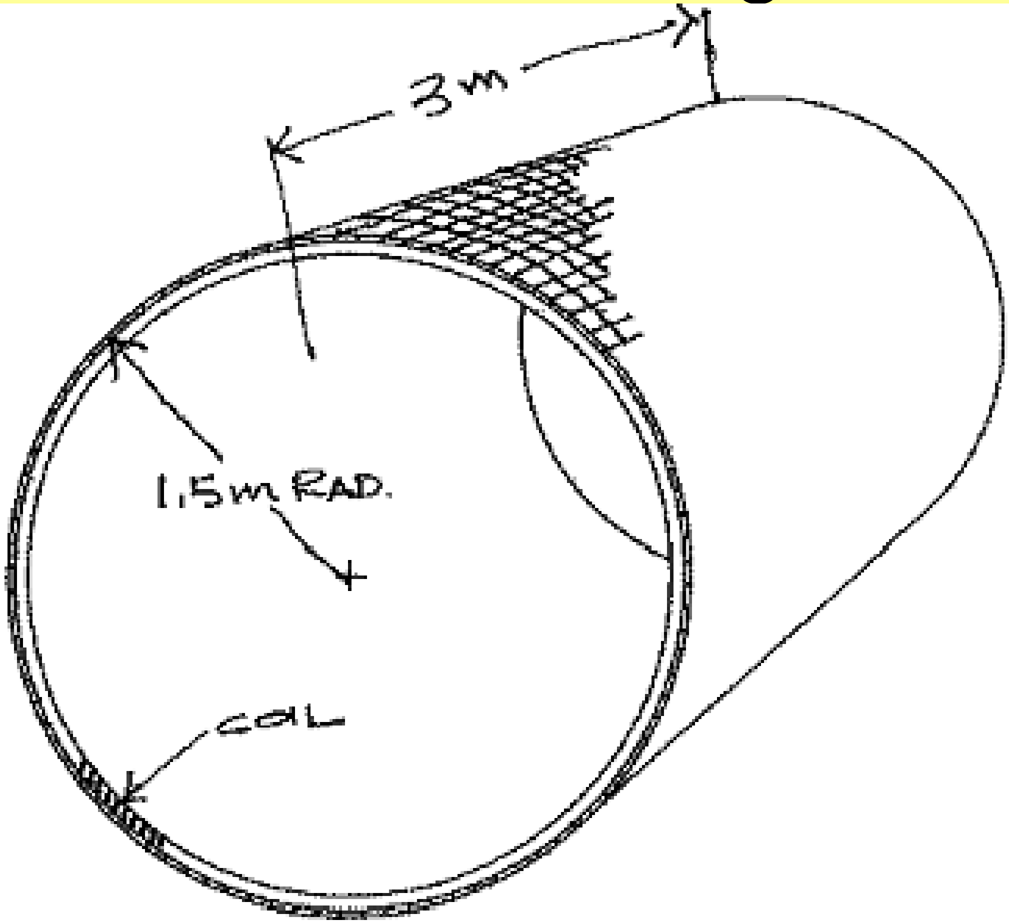
Cal. Energy
From electron

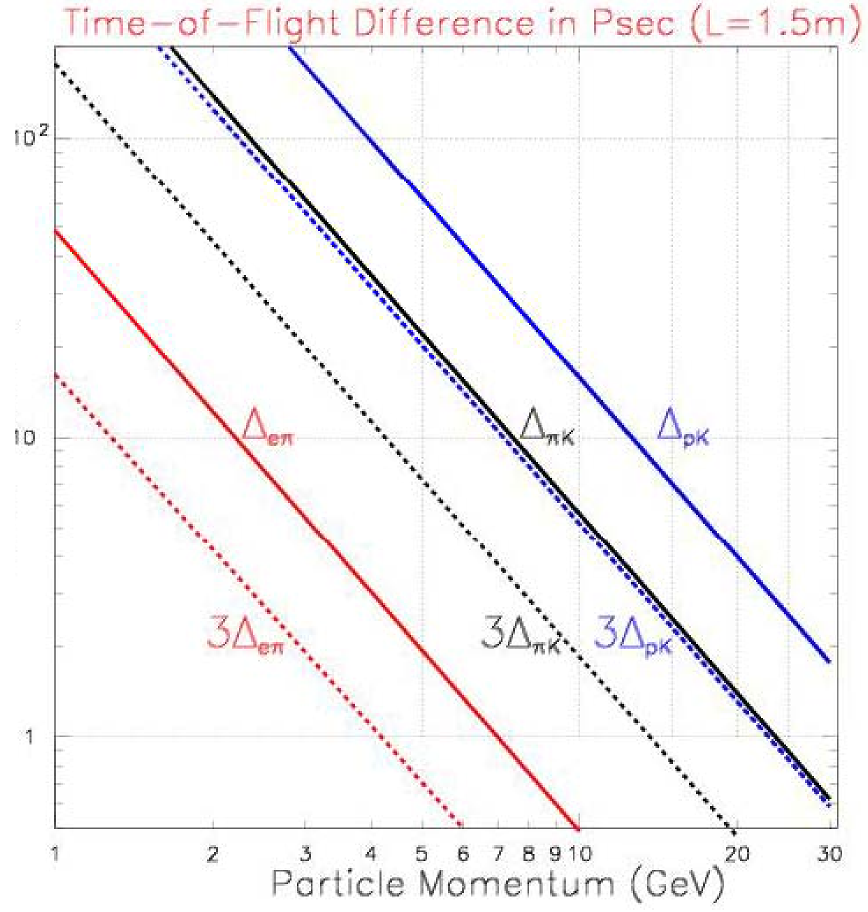
W->electron+neutrino

**Fit $t_0$ (start) from all tracks**

Can we follow the color flow through kaons, cham, bottom? TOF!

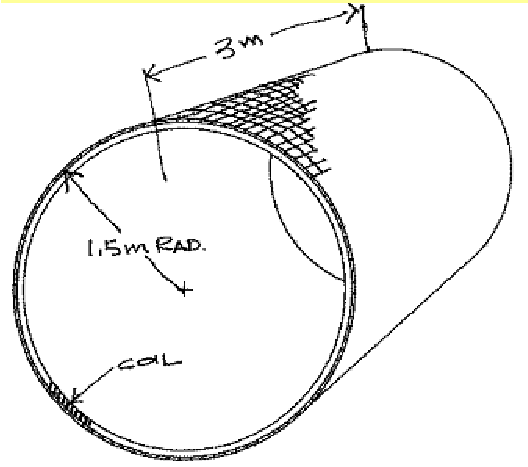
# Application 1- Collider Detector Upgrade Charged Particle ID



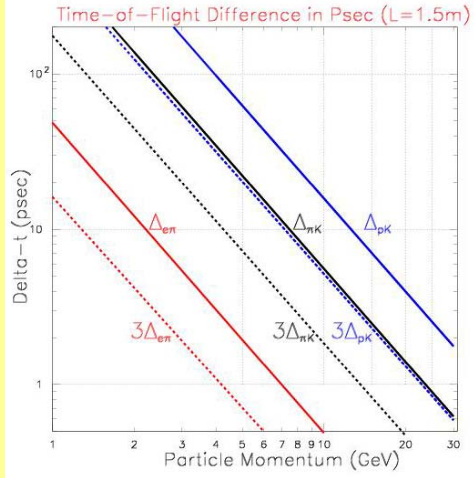




- E.g- Tevatron 3rd-generation detector (combine D0 and CDF hardcore groups); ATLAS Upgrade (true upgrade)

# Application 1- Collider Detector Upgrades




- Precision Measurements that rely on measuring quark-flow

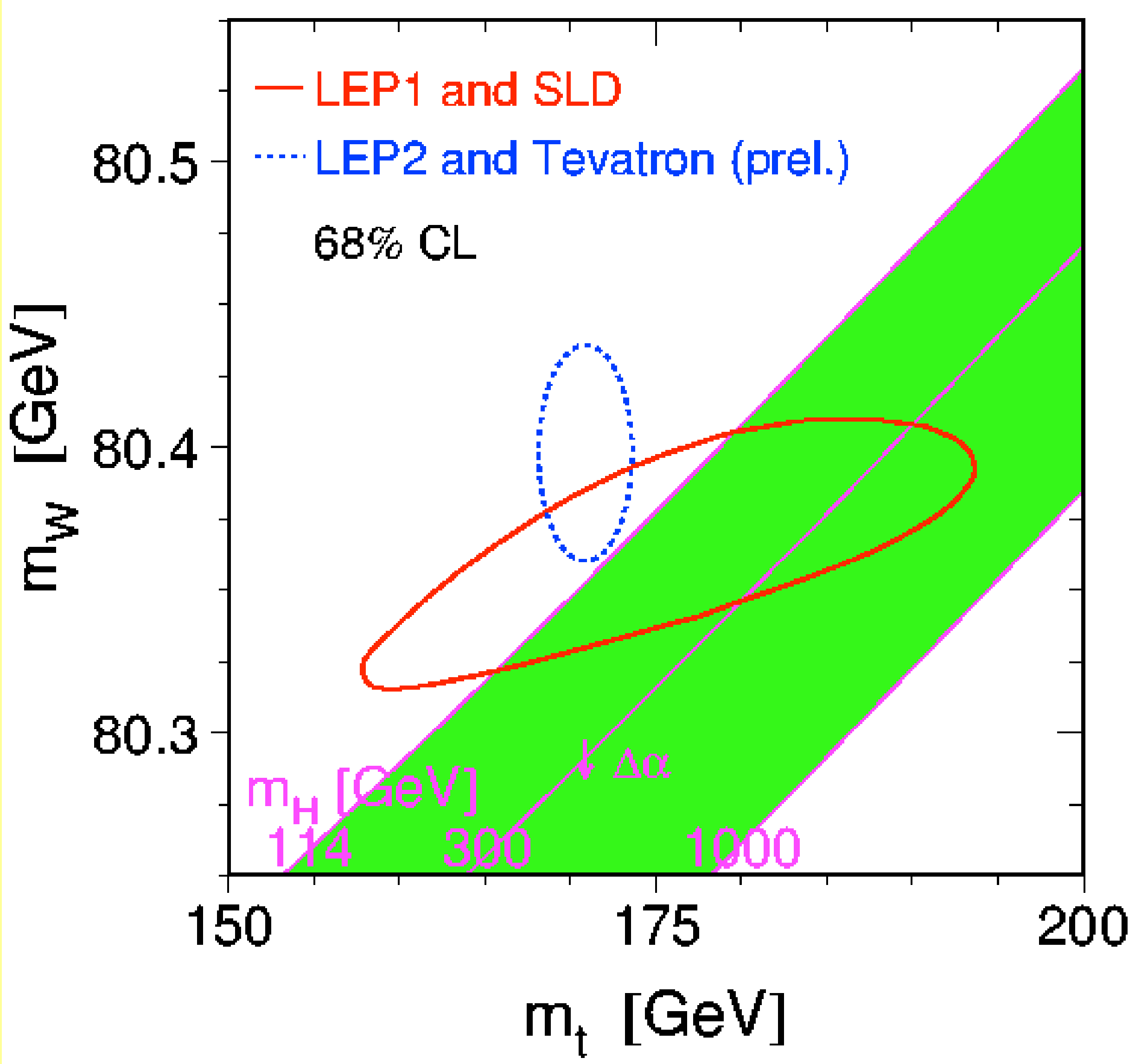



**W-mass: W->c+sbar or u+dbar- different kaon production**

**Top-mass: t+tbar -> W+W-b+bbar; need to tell b from bbar**

**E.g.- ATLAS, Tevatron-III**

# MW-Mtop Plane




$M_W$= 80.398 \pm 0.025 GeV (inc. new CDF 200pb$^{-1}$)

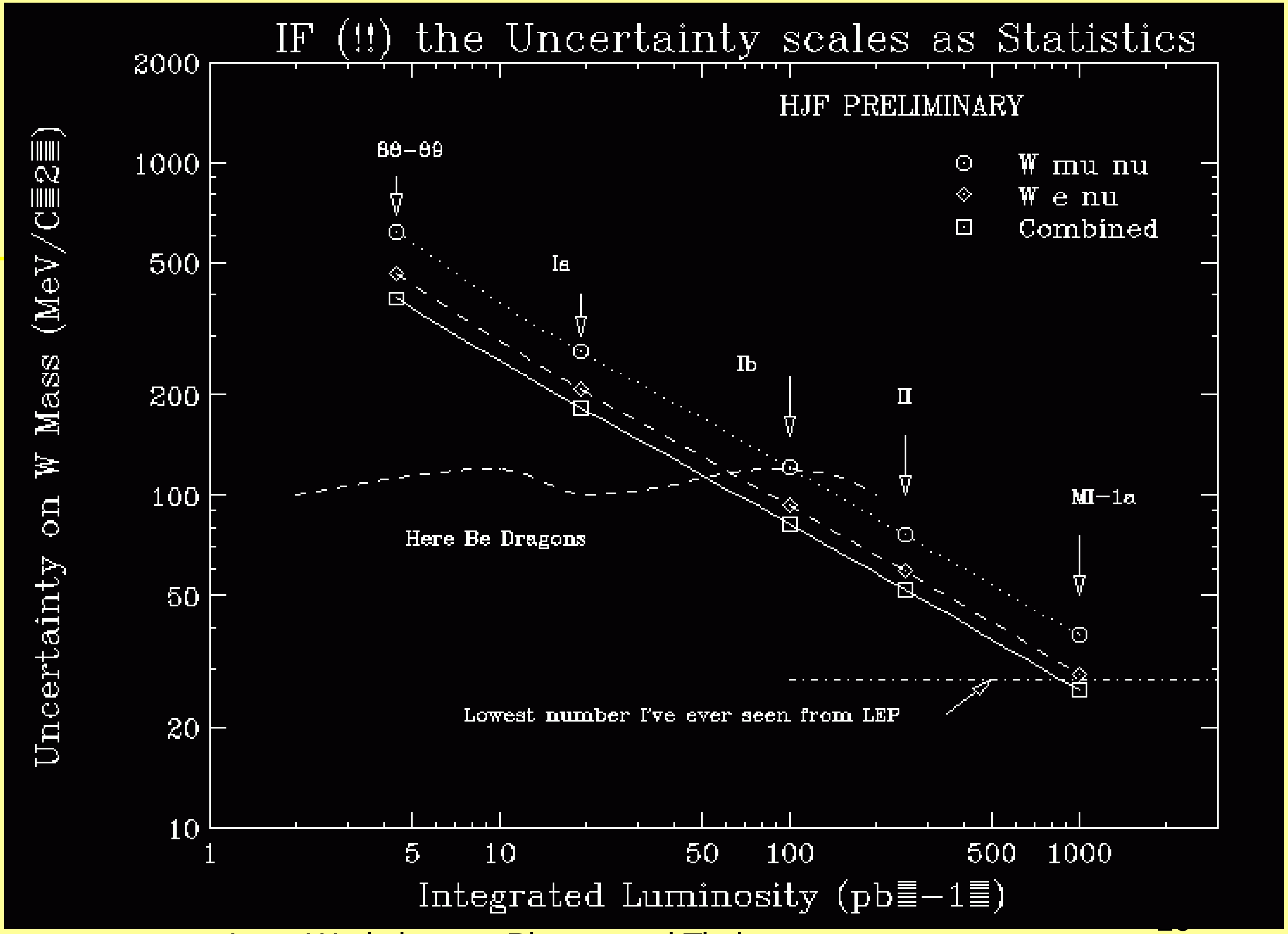
$M_{Top}$ = 170.9 \pm 1.8 GeV (March 2007)

# Application 1- Collider Detector Upgrades

Take a systematics-dominated measurement: e.g. the W mass.

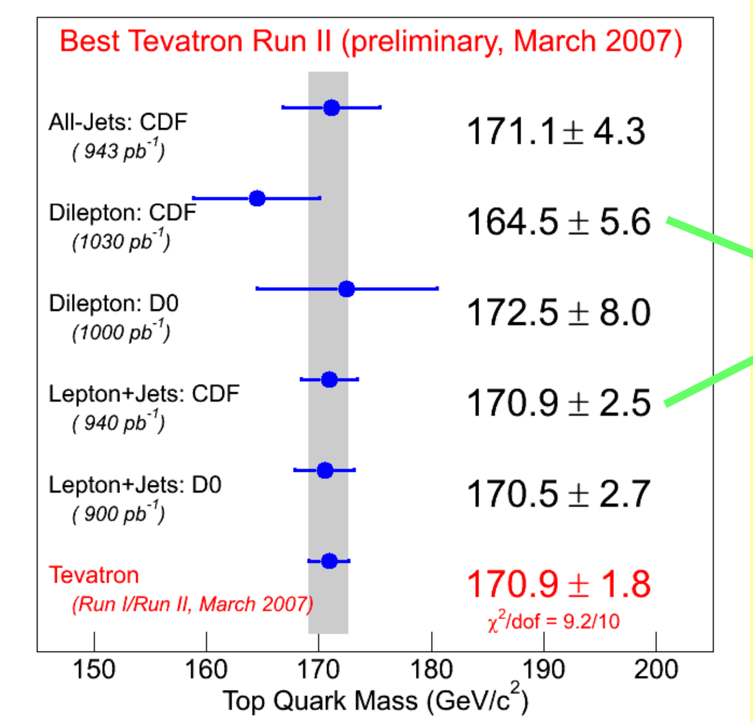
Dec 1994 (12 yrs ago)-

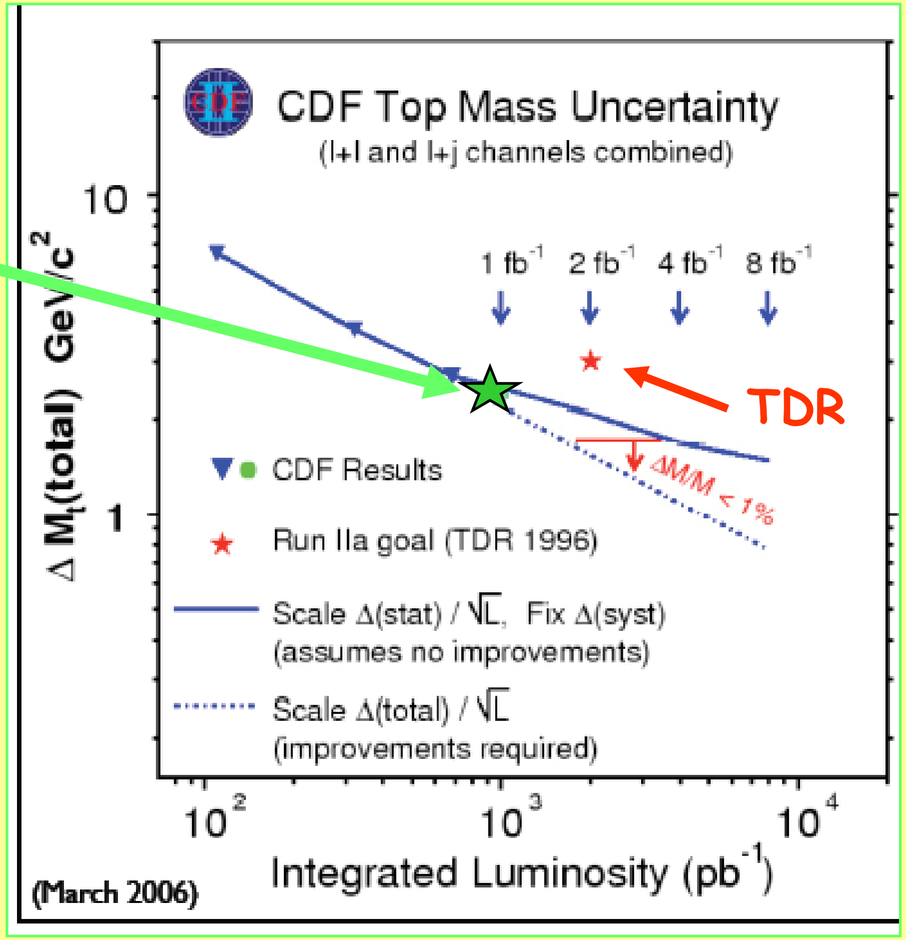
`Here Be Dragons' Slide: remarkable how precise one can do at the Tevatron (MW,Mtop, Bs mixing, …)- but has taken a long time- like any other precision measurements requires a learning process of techniques, details, detector upgrades….




Theorists Too(SM)

# Precision Measurement of the Top Mass




**Aspen Conference Annual Values**
**(Doug Glenzinski Summary Talk)**

Jan-05: $\Delta$Mt = +/- 4.3 GeV
Jan-06: $\Delta$Mt = +/- 2.9 GeV
Jan-07: $\Delta$Mt = +/- 2.1 GeV

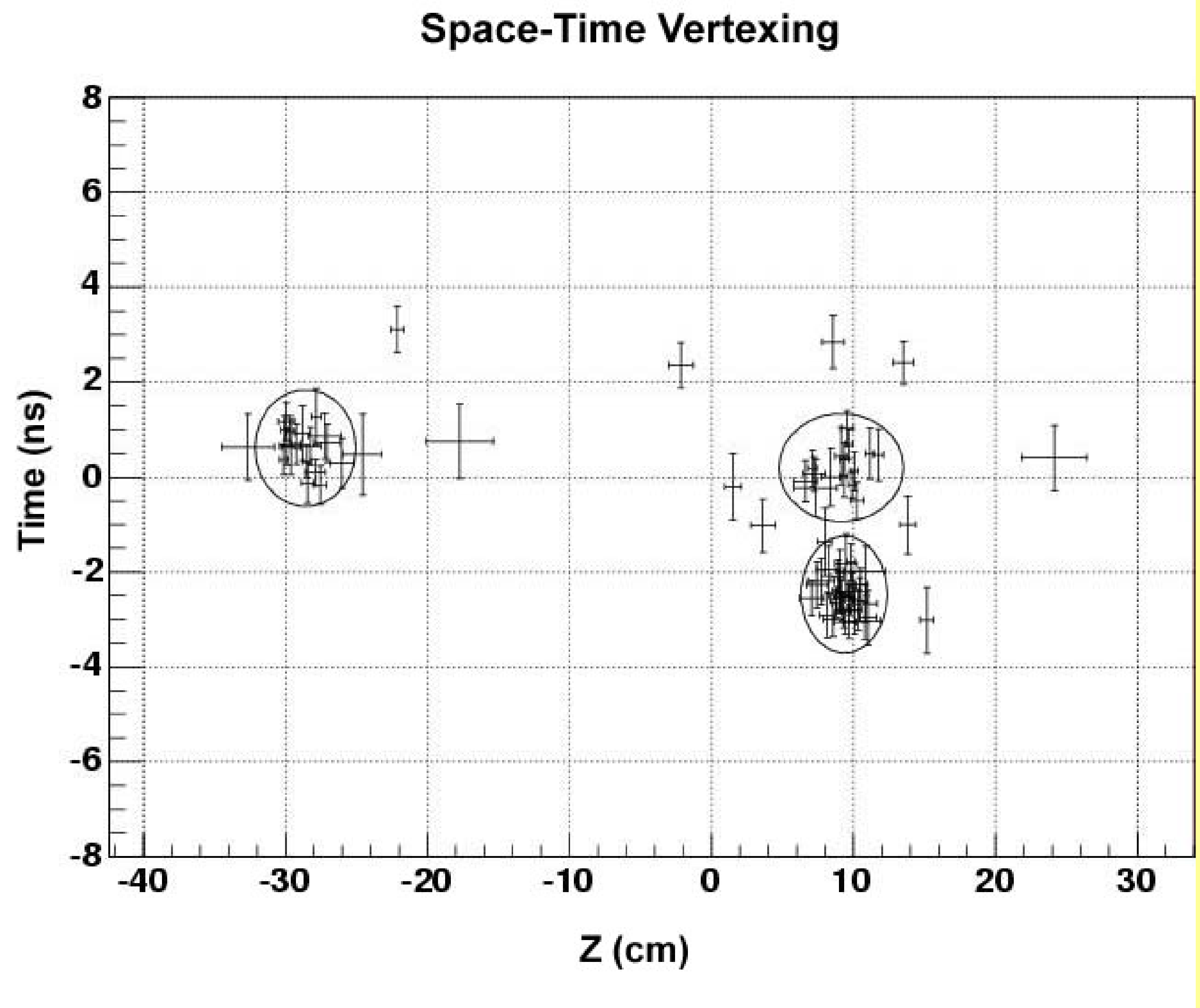
Note we are doing almost 1/root-L even now

**Setting JES with MW puts us significantly ahead of the projection based on Run I in the Technical Design Report (TDR). Systematics are measurable with more data (at some level- but W and Z are bright standard candles.)**

# Real Possibility

- No SM Higgs is seen at the LHC
- The M-top/M-W plane says the Higgs is light.
- Serious contradiction inside the SM- `smoking gun’ for something really new…
- It will be critical to measure M_W and M-top with different systematics…

# Application 1a- Collider Detector Upgrade Photon Vertexing



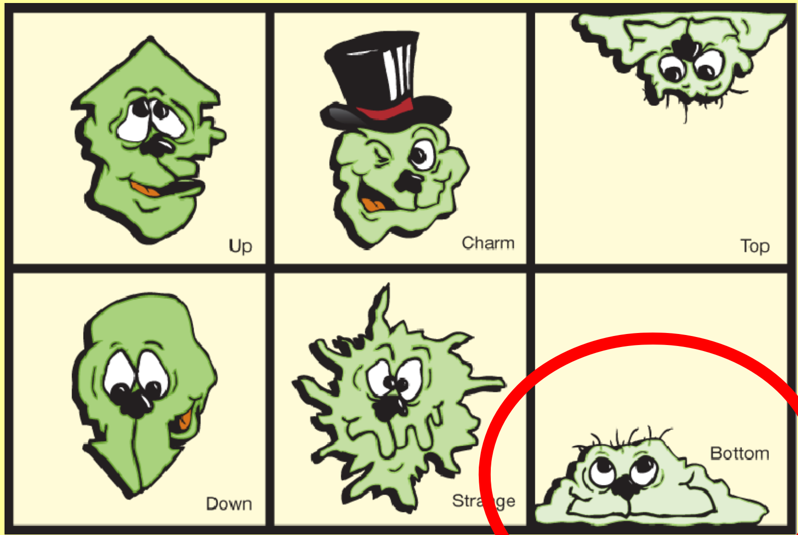

- Atlas Upgrade- Higgs to gamma-gamma?

# Application 2- Forward LHC Detectors

- - Idea is to do missing-mass search for new heavy states (e.g. Higgs) by looking at the quasi-elastic protons forward and backward;
- Need few psec timing resolution to beat down backgrounds (accidentals);
- Different problems- close to LHC beam (i.e rad hard), in tunnel, long distances for clock distribution (but use beam), but few channels- (small MCP's?);
- Good early application- see talks by Christophe, Krzystof, Andrew,..

# Application 3-Super-B Factories

- Particle ID for precision b-physics measurements in larger angle regions
- Probe energy frontier via precision/small $\sigma$
- See talks by Gary and Jerry



# Application 4: Fixed-target Geometries Particle ID and Photon Vertexing

- - Consider LHCb and JPARC $K_L^o \to \pi^0 \nu\nu$

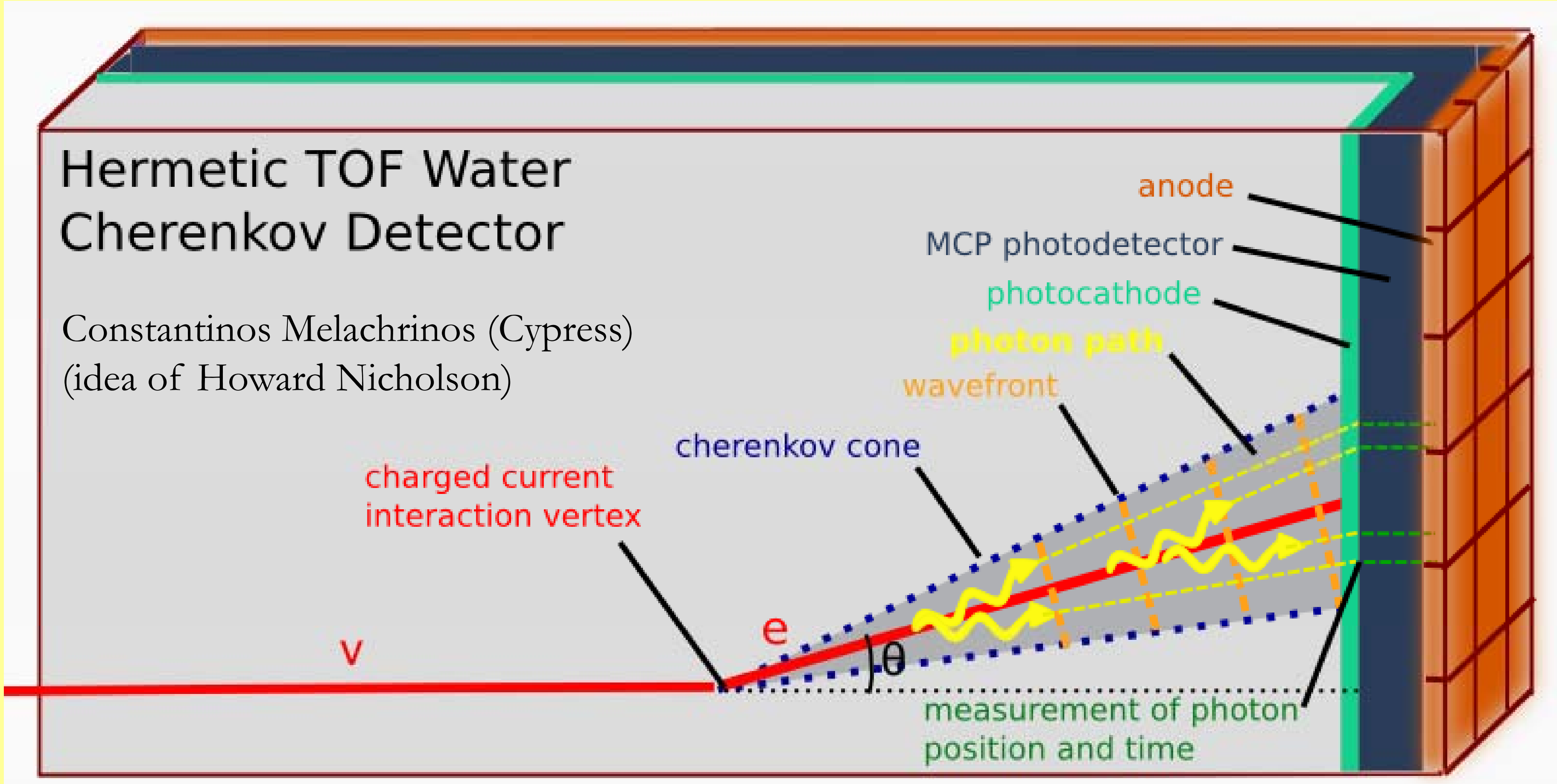
Geometry is planar- i.e. the event is projected onto a detection plane. Timing gives the path length from the point on the plane*-

Critical **new** information for vertexing, reconstruction of $\pi^0$ 's from 2 photons, direction of long-lived particles.

Very thin in 'z'-direction, unlike Cherenkov counters.

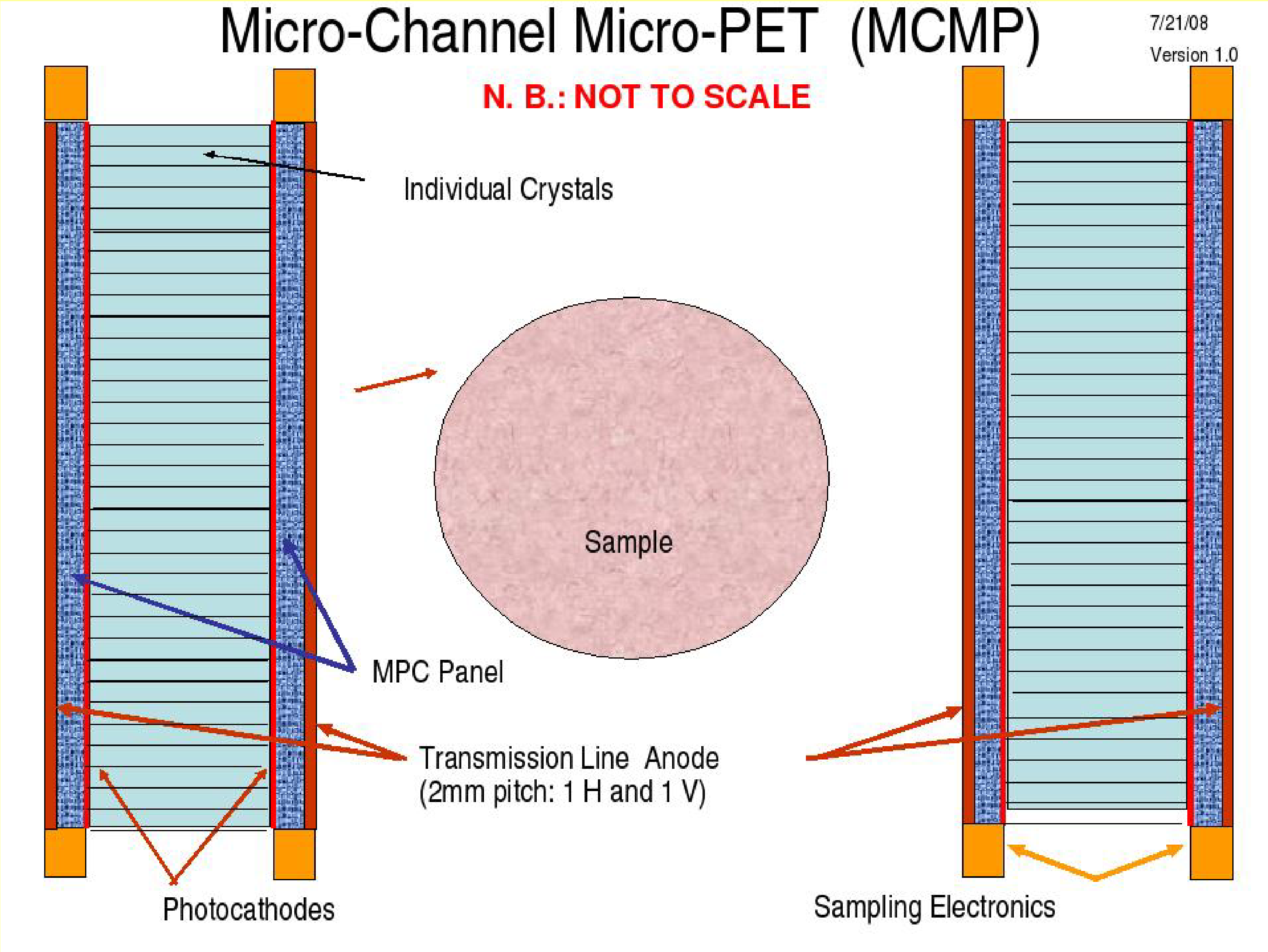
Gives a space-point with all 3 coordinates- x,y and z, correlated for reconstruction- i.e. 'tomographic'.

# Application 5- Neutrino Physics




- Example- DUSEL detector with 100% coverage and 3D photon vertex reconstruction.

# Application 6- Medical Imaging (PET)



# Characteristics we need

- Feature size <~ 300 microns
- Homogeneity (ability to make uniform large-area- think amorphous semicndtr solar-panel)
- Fast rise-time and/or constant signal shape
- Lifetime (rad hard in some cases, but not all)
- System cost << silicon micro-vertex system

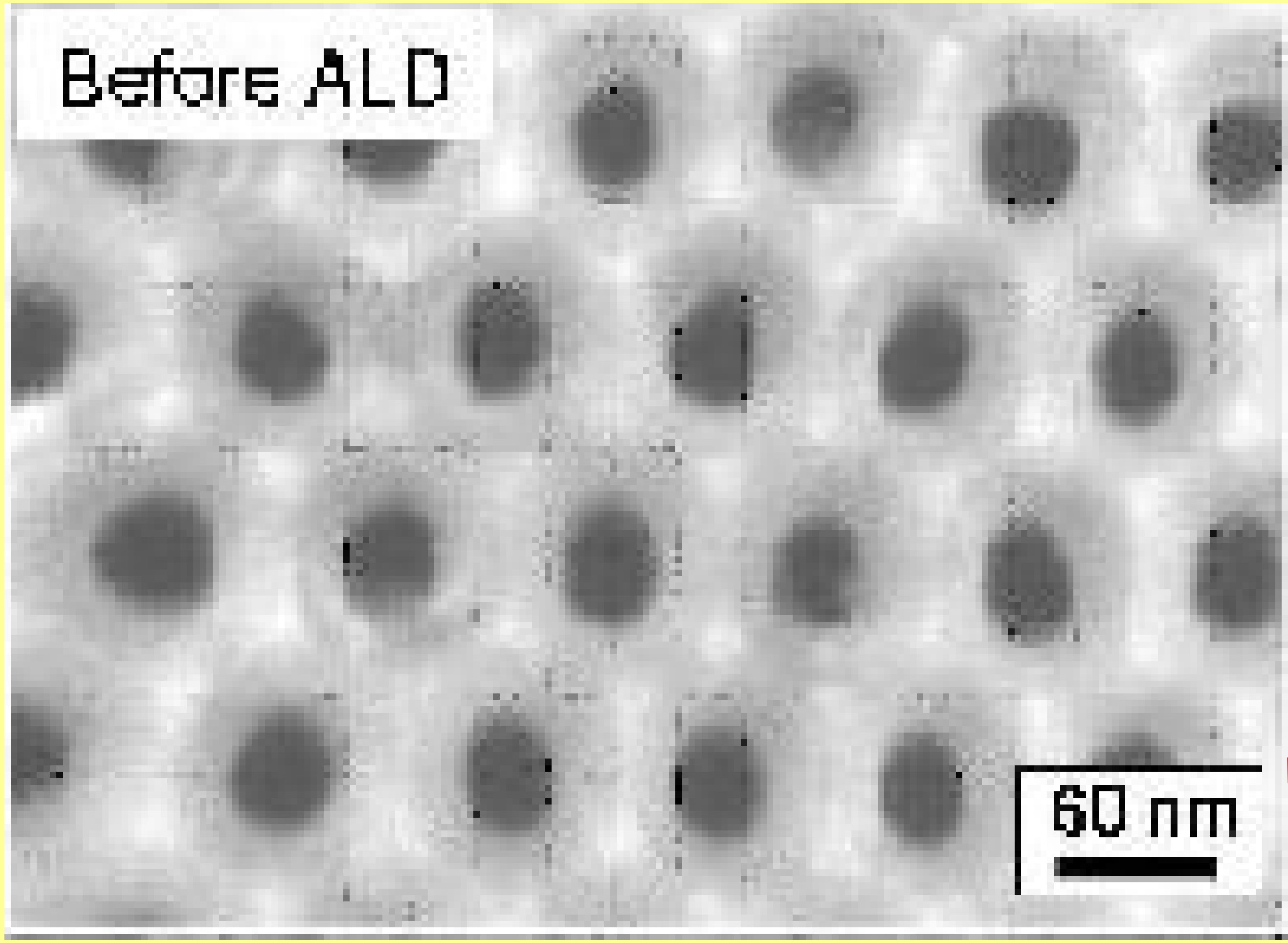
# Detector Development- 3 Prongs

- 1. Electronics- have settled on wave-form sampling
  - **Already demonstrated by Breton, Delanges,Ritt, and Varner- many `pieces' exist, main change is going to faster process and pooling expertise.**
  - **Reasonable precision (see talk by Genat)- few psec with present rise times, ~1 with faster MCP design.**
  - **Gives much more than time- space, pileup, etc. (Tang)**

  2. MCP development- techniques and facilities (probably) exist- ALD, anodic alumina--will require industry, natl labs,

  3. Simulation –
  - **Electronics simulation in good shape**
  - **Rudimentary `end-to-end' MCP device simulation exists-**
  - **Validation with laser teststand and beam line started**

# GOAL: to Develop Large-Area Photo-detectors with Psec Time and mm SpaceResolution




Too small- can go larger-

(But how does multiplication work- field lines?)

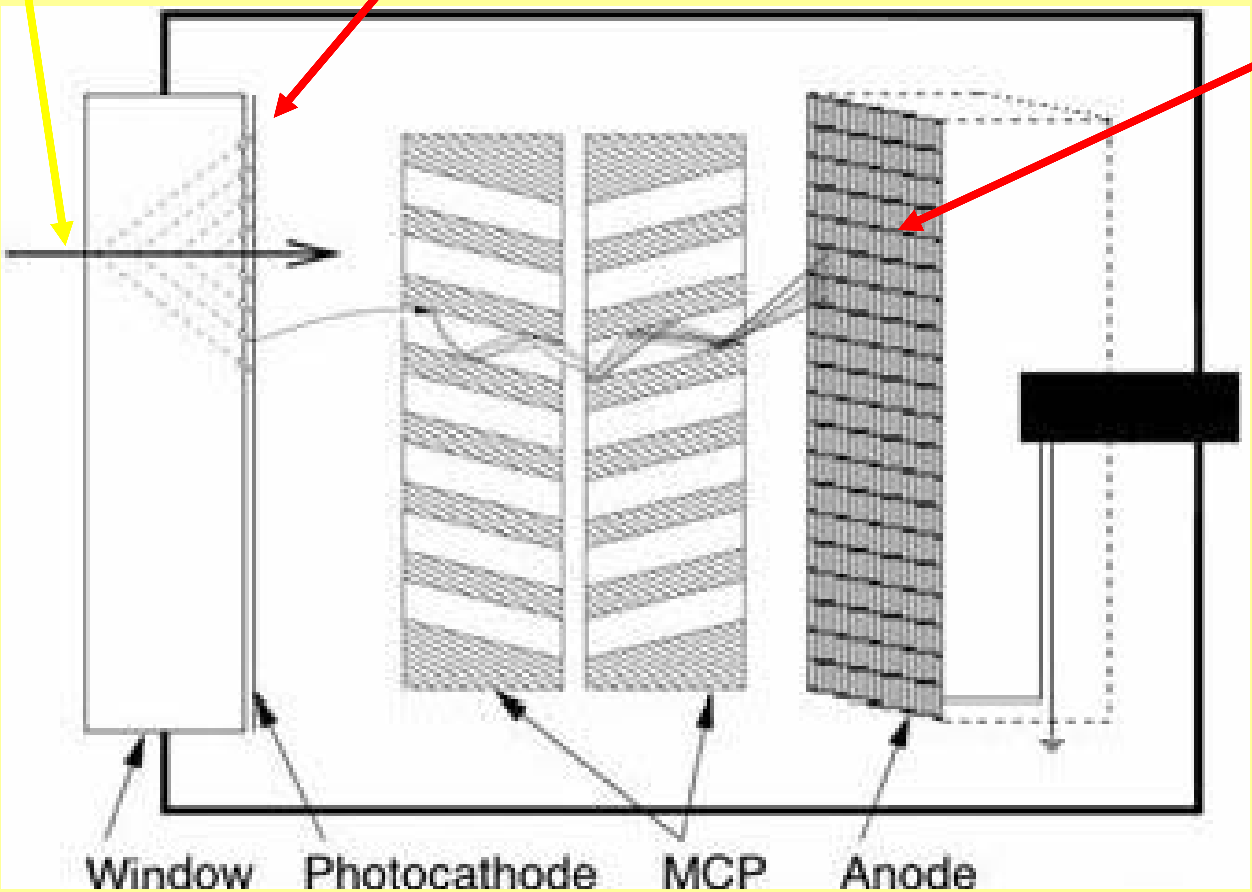
**From Argonne MSD ALD web page- can we make cheap (relatively) ultra-fast planar photo-detector modules?**

# Generating the signal for relativistic particles (HEP, nuclear, astro, accelerator)

Incoming rel. particle

## Use Cherenkov light - fast

Custom Anode




Present work is with commercial MCP's: e.g. Burle/Photonis Planicons. Expensive (!), hard to get, little flexibility.

BUT- it works. And well.

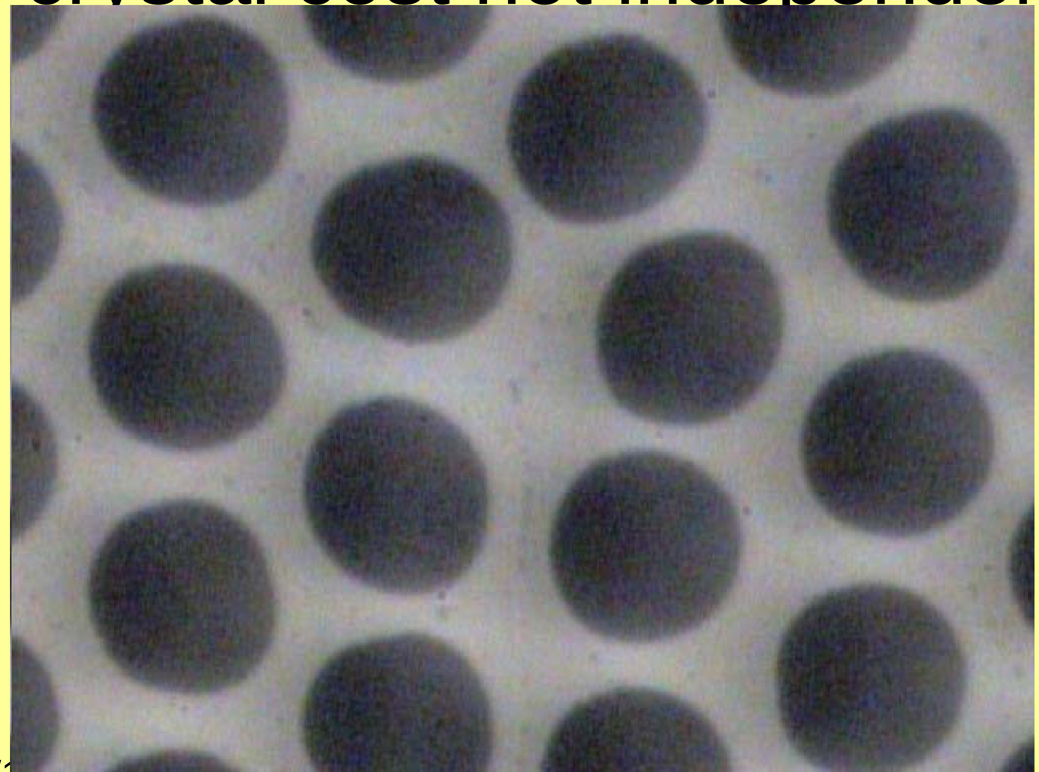
# Design Goals

Colliders: ~ 1 psec resolution, < 100K$/m²

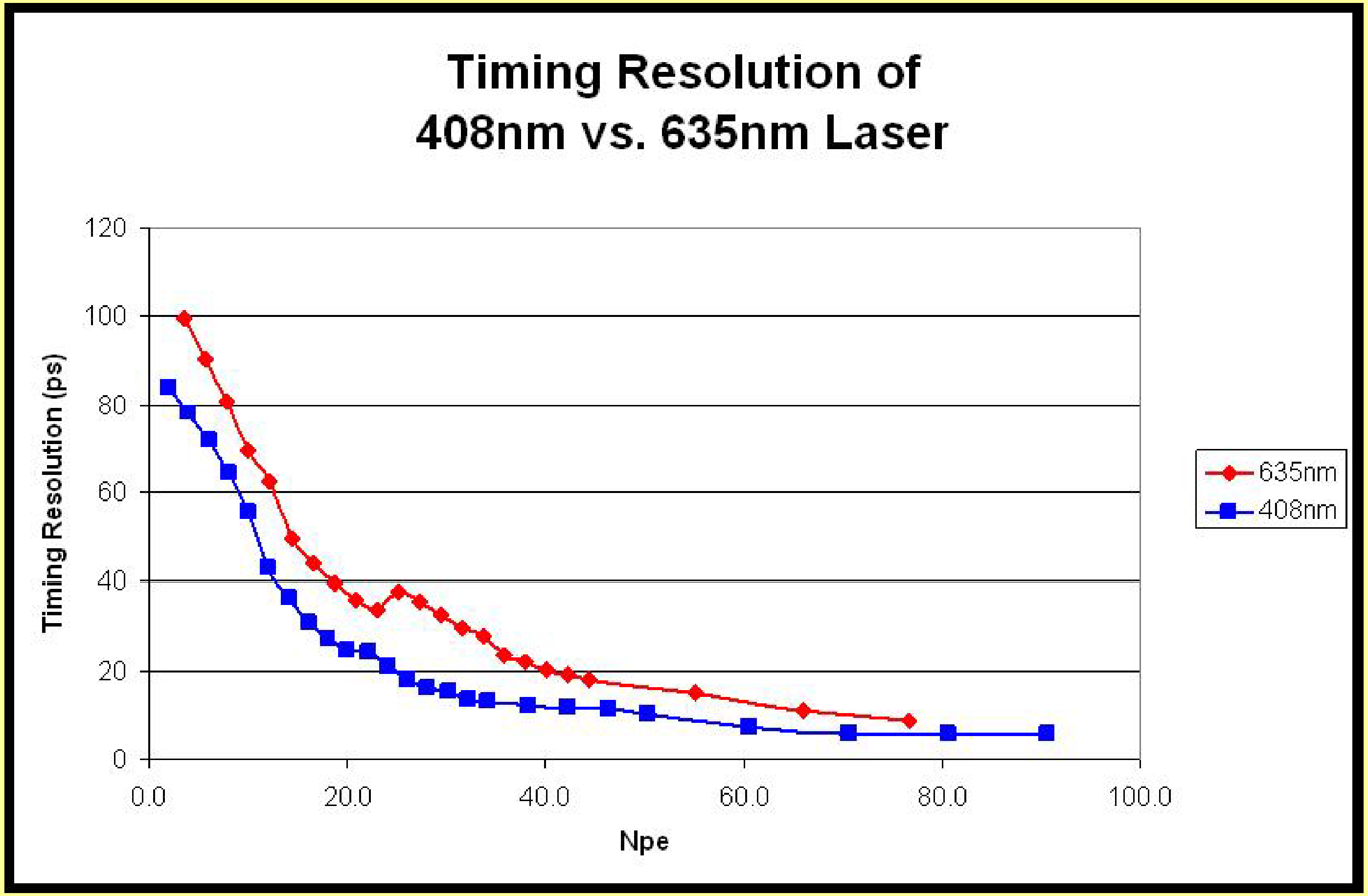
Neutrino H2O: ~100 psec resolution, < 1K$/m²

PET: ~ 30 psec resolution, < 20% of crystal cost

(but crystal cost not independent of readout!)



**Micro-photograph of Burle 25 micron tube- Greg Sellberg (Fermilab)- ~2M$/m²- not including readout**




**Camden Ertley results using ANL laser-test stand and commercial Burle 25-micron tube**

**(note- pore size may matter less than current path!- we can do better with ALD custom designs (transmission lines))**

# Understanding the contributing factors to 6 psec resolutions with present Burle/Photonis/Ortec setups- Jerry Vavra's Numbers

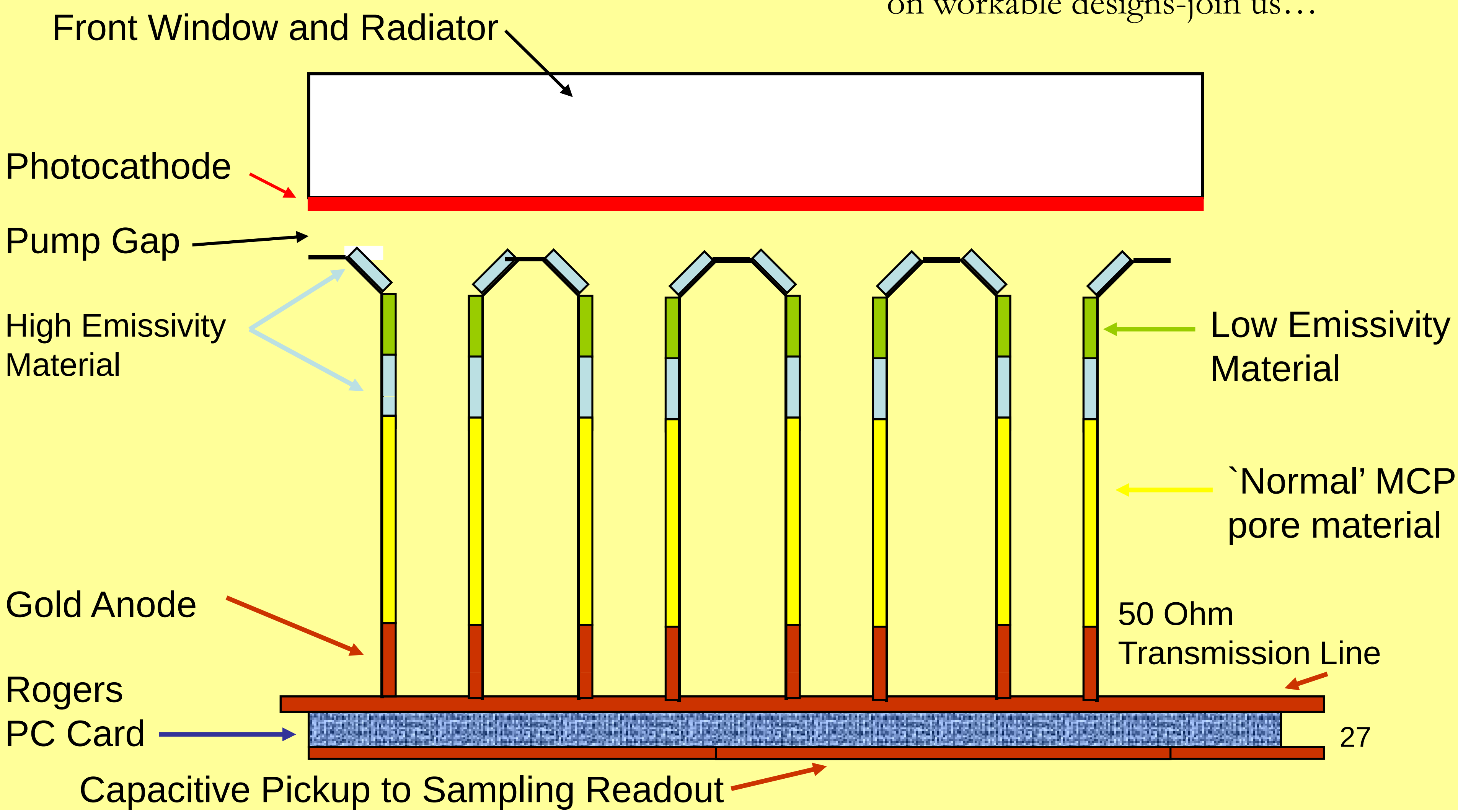
1. TTS: 3.8 psec (from a TTS of 27 psec)
2. Cos(theta)_cherenk 3.3 psec
3. Pad size 0.75 psec
4. Electronics 3.4 psec

# `Photo-multiplier in a Pore'

- Idea is to build a PMT structure inside each pore- have a defined dynode chain of rings of material with high secondary emissivity so that the start of the shower has a controlled geometry (and hence small TTS)
- One problem is readout- how do you cover a large area and preserve the good timing?
- Proposed solution- build anode into pores, capacitively couple into transmission lines to preserve pulse shape.

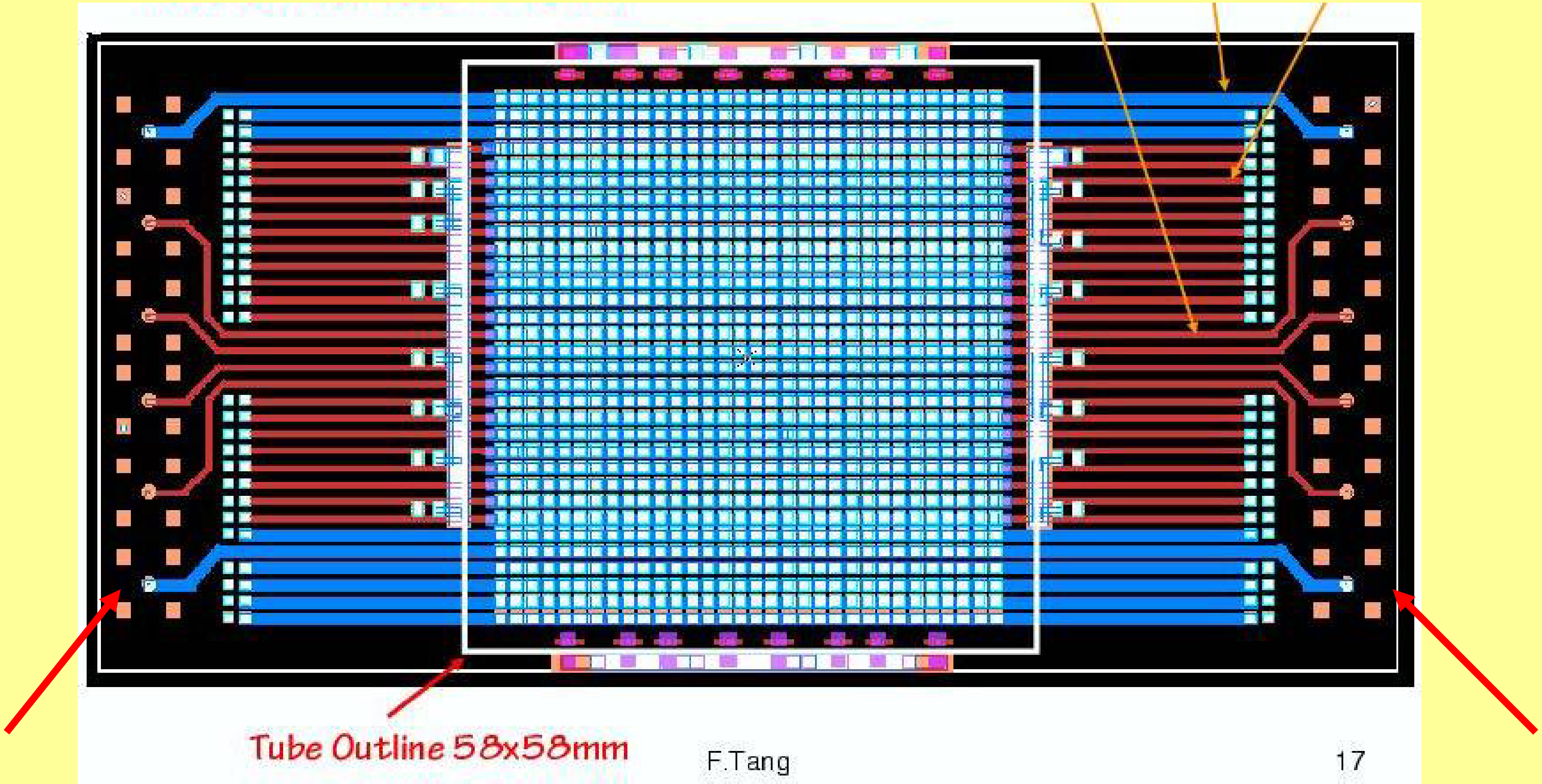
# Psec Large-area Micro-Channel Plate Panel (MCPP)- LDRD proposal to ANL (with Mike Pellin/MSD)

N.B.- this is a `cartoon’- working on workable designs-join us…



# Get position AND time

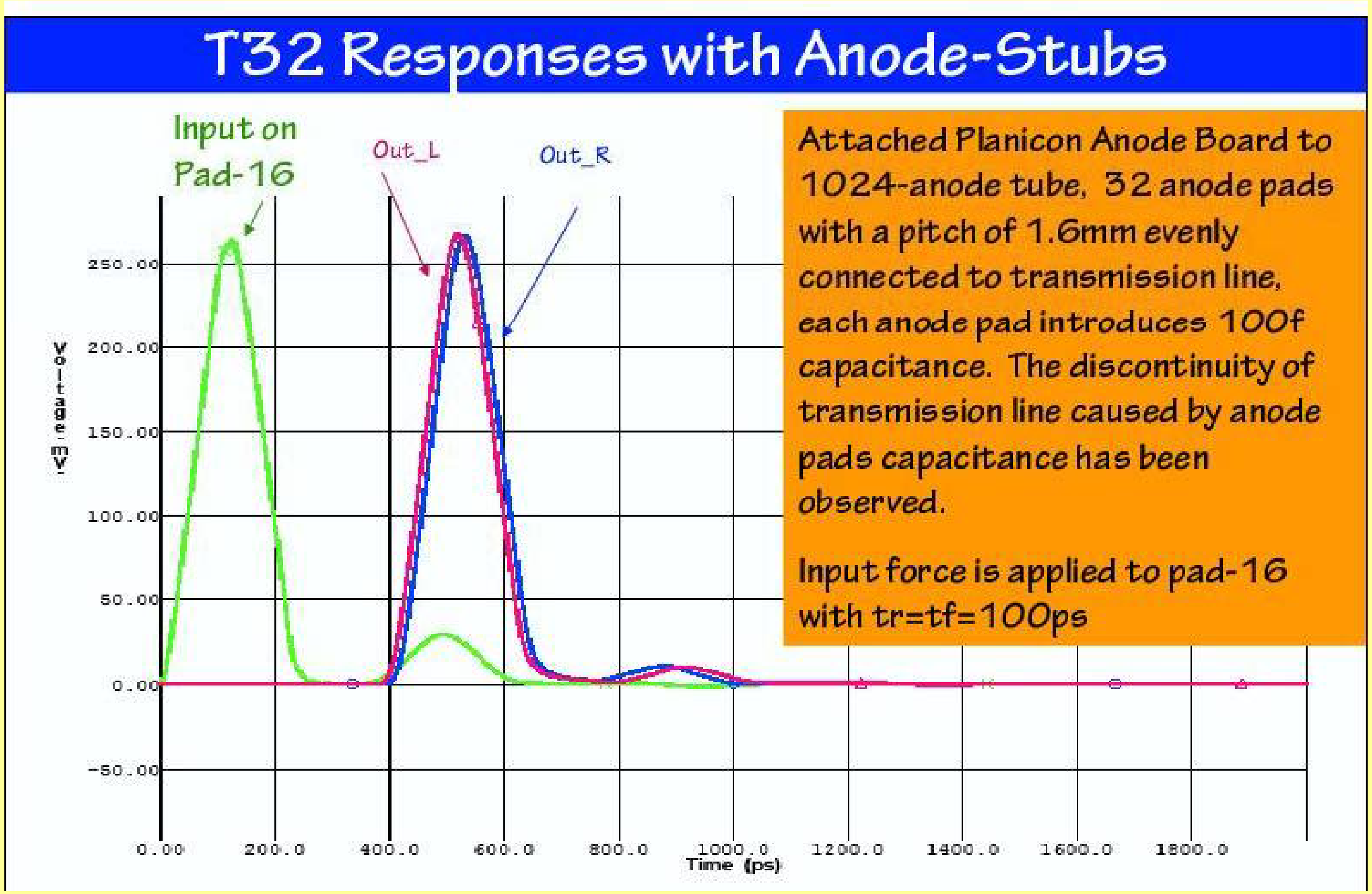
## Anode Design and Simulation(Fukun Tang)




- Transmission Line- readout both ends=> pos and time
- Cover large areas with much reduced channel account.

# Expected Performance

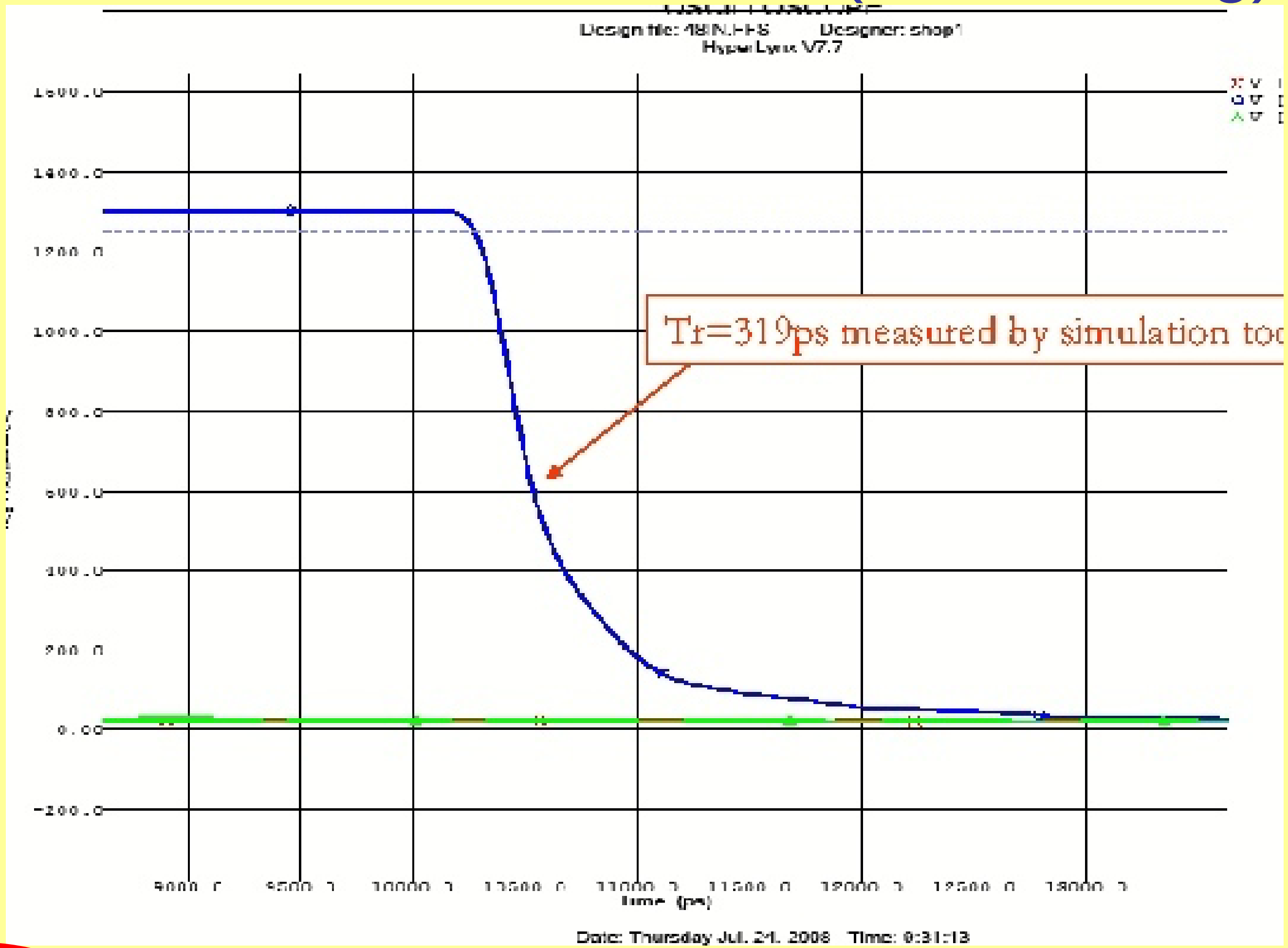
## Anode Design and Simulation(Fukun Tang)




- Transmission Line- simulation shows 3.5GHz bandwidth- 100 psec rise (well-matched to MCP)
- Board has been made-

# Scaling Performance to Large Area

## Anode Simulation(Fukun Tang)

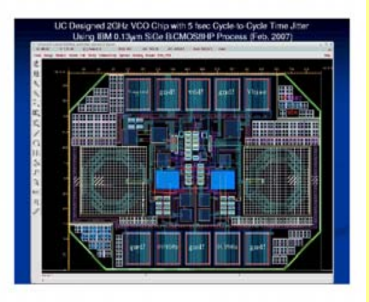



- 48-inch Transmission Line- simulation shows 1.1 GHz bandwidth- still better than present electronics.

# Front-end Electronics

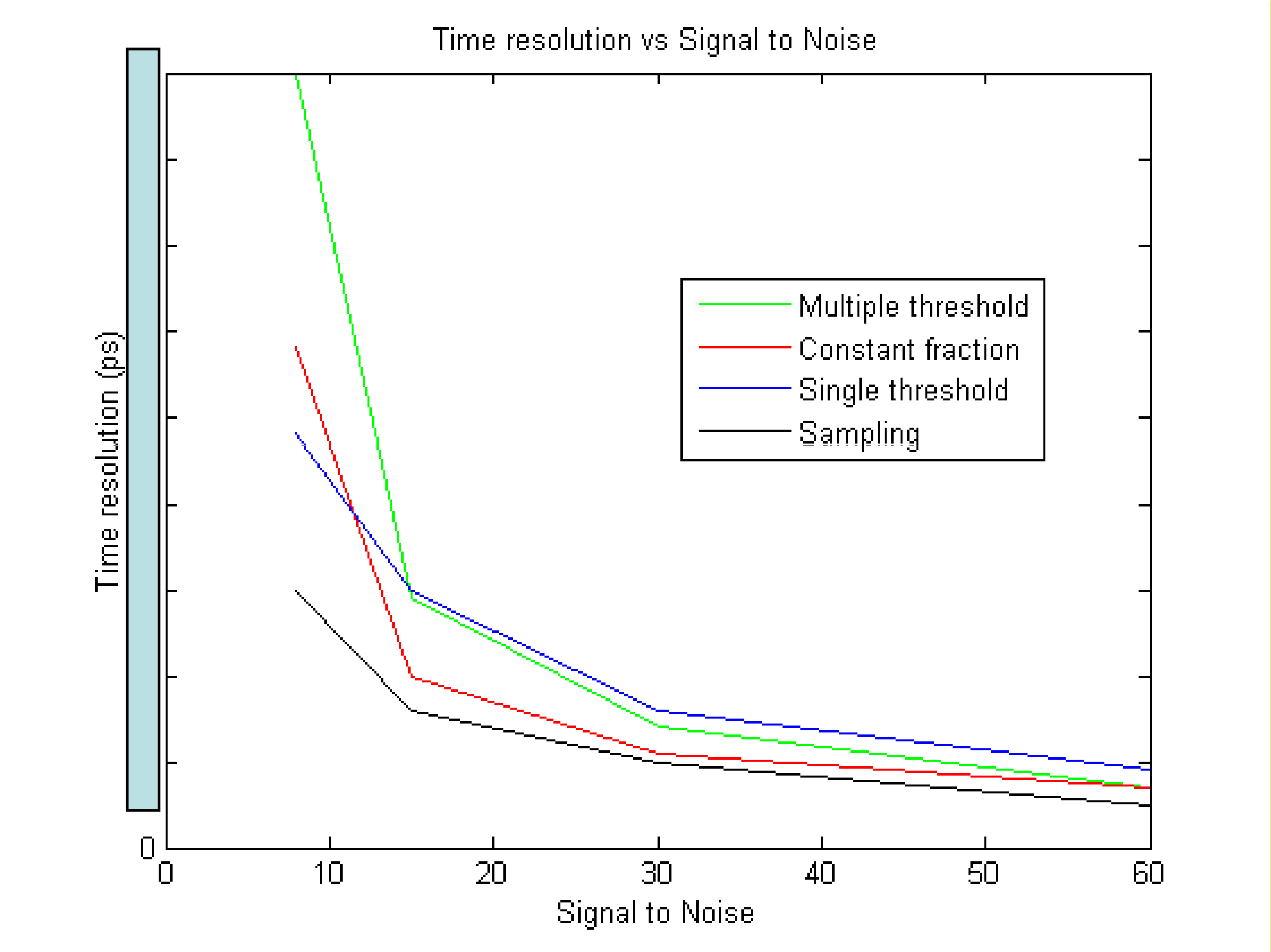
## Critical path item- probably the reason psec detectors haven't been developed

- We had started with very fast BiCMOS designs- IBM 8HP-Tang designed two (really pretty) chips




- Realized that they are too power-hungry and too 'boutique' for large-scale applications
- Have been taught by Gary Varner, Stefan Ritt, Eric DeLanges, and Dominique Breton that there's a more clever and elegant way- straight CMOS – sampling onto an array of capacitors
- Have formed a collaboration to do this- have all the expert groups involved (formal with Hawaii and France)- see talks by Tang and Jean-Francois

# Front-end Electronics




Old plot- apologies (didn't get to update it before leaving)

## II STATE OF THE ART

Several circuits have already been designed in the HEP community for fast pulse sampling, mainly to record photo-multipliers pulse shapes. As detailed in section I, fast timing requires higher sampling rates, but smaller dynamics ranges.

| | Hawaii | | Orsay/Saclay | | PSI | | PSEC |
|---|---|---|---|---|---|---|---|
| | Lab 3 | Planned Blab2 | Sam | Planned | DRS3 | Planned DRS4 | This proposal |
| Sampling frequency | 20 MHz-3.7 GHz | 1-10 GHz | 0.7-2.5 GHz | 10 GHz | 10 MHz-5 GHz | 5 GHz | 40 GHz |
| Analog bandwidth | 900 MHz | 850 MHz | 300 MHz | 650 MHz | 450 MHz | > DRS3 | > 1 GHz |
| Number of Channels | 9 | 16 | 2 | | 12/6/2/1 | 8/4/2/1 | 16 |
| Triggered mode | Common Stop | Channel trigger on sums | Common Stop | | Common Stop | Common Stop | Channel trigger |
| Resolution | | 10 bit | 11.6 bit | | 11.6 bit | 11.5 bit | 8-10 bit |
| Samples | 256 | 4/8 rows of 512 | 256 | 2048 | 1024-12288 | 1024-8192 | 64 |
| Clock | 33 MHz | 33 MHz | 66 MHz | | 20 MHz | fsamp/2048 | 60 MHz |
| Max latency | | | 5ms | | 0.6 ms | | |
| Input Buffers | | TIA (5kOhm gain) | Yes | No | No | No | Yes |
| Differential Inputs | No | Pseudo-diff | Yes | | Yes | Yes | Pseudo diff |
| Input impedance | 50 Ohms Ext | 30-70 Ohms adjustable | > 10 MOhm | | | 7-11pF | |
| Readout clock | | 1 GHz Wilkinson | 16 MHz | | 33 MHz | 33 MHz | 60 MHz |
| Readout time | 150µs | 512µs | < 2 µs | | 30ns * n samples | 30ns * n samples | < 1 µs |
| Locked delays | Ext DAC | Ext DLL | Int DLL | | Ext PLL | Int PLL | |
| On-chip ADC | Yes | 1 GHz Wilkinson | No | | No | No | Yes |
| R/W simultaneous | | Yes | No | | No | Yes | No |
| Power/ch | 50mW | 20mW/sample 0.2W/read | 150 mW | | 1-13mW | 2-20mW | |
| Dynamic range | | 1mV/1V | 0.65mV-2V | | 0.35mV/1.1V | 0.35/1V | 1V |
| Xtalk | Average << 10% | < 0.1% | 0.30% | | <0.5% | <0.5% | |
| Sampling jitter | | TBD | 40ps | | 200ps (Ext PLL) | Ext PLL | 10ps |
| Power supplies | 2.5V | 2.5V | 0-3.3V | | 2.5V | 2.5 V | 1.8V |
| Process | TSMC 0.25 | TSMC 0.25 | AMS 0.35 | AMS 0.18 | UMC 0.25 | UMC 0.25 | CMOS 0.13 |
| Chip area | 2.5 mm2 | 12 mm2 | 10 mm2 | | 25 mm2 | 25 mm2 | 1 mm2 |
| Cost/channel | | 500$/40 10$/2k | 15.7$/12k | | | 10-15$ | |

Table 1. State of the art, this proposal. The yellow column is from Gary Varner's group at the University of Hawaii (USA) [12], the light blue from Dominique Breton from the University of Paris-Sud (Orsay) [10] and Eric Delagnes from CEA (Saclay), (France) [11]. The orange column from Stefan Ritt at PSI (Switzerland) [13]. The dark blue is this proposal.

# Jerry's #'s re-visited : Solutions to get to <several psec resolution.

1. **TTS: 3.8 psec (from a TTS of 27 psec)**

   **MCP development- reduce TTS- smaller pores, smaller gaps, filter chromaticity, ANL atomic-deposition dynodes and anodes.**

2. **Cos(theta)_cherenk 3.3 psec**

   **Same shape- spatial distribution (e.g. strips and time-differences measure spot)**

3. **Pad size 0.75 psec-**

   **Transmission-line readout and shape reconstruction**

4. **Electronics 3.4 psec –**

   **fast sampling- should be able to get < 2 psec (extrapolation of simulation to faster pulses)**

# Modus Operandi so far

- In Nov. 2005, we had our 1st workshop- idea was to invite folks working or interested in related subjects- didn't know many (most) of them
- Have developed tools and knowledge- also contact with pioneers and practictioners (Ohshima, Howorth, Va'vra,…; Breton, Delanges, Ritt, Varner)
- Development clearly too big for one group- devices, electronics, applications- have worked collaboratively with each other, national labs (see talks by Karen, Andrew,Jerry,…), and industry (Burle/Photonis, Photek, IBM,…)

# My attempt at Goals for the Workshop

(these are my goals- apologies if it's presumptious)

- To form collaborations on solving key problems
- To identify expertise- many of these questions aren't new, and somebody (probably Jon or Emil or Jerry) knows..
- To  identify and advertise facilities- e.g. the Fermilab test beam, ANL laser test-stand, CERN IBM 0.13micron kit,..
- To answer critical questions along the path…(e.g. 2ndary emission of materials,..)

# My Questions This Time-I

Note- many questions from previous workshops have been answered!

1. What is the electric field geometry in the MCP pore? (what are bulk and surface resistivities? ).
2. What is the response of a nano-carbon film to 200 eV electrons? (photons?)
3. After the first strike, can the pore be straight?
4. If one uses diamond (e.g.), do you really need fewer strikes?

# My Questions This Time-II

Note- many questions from previous workshops have been answered!

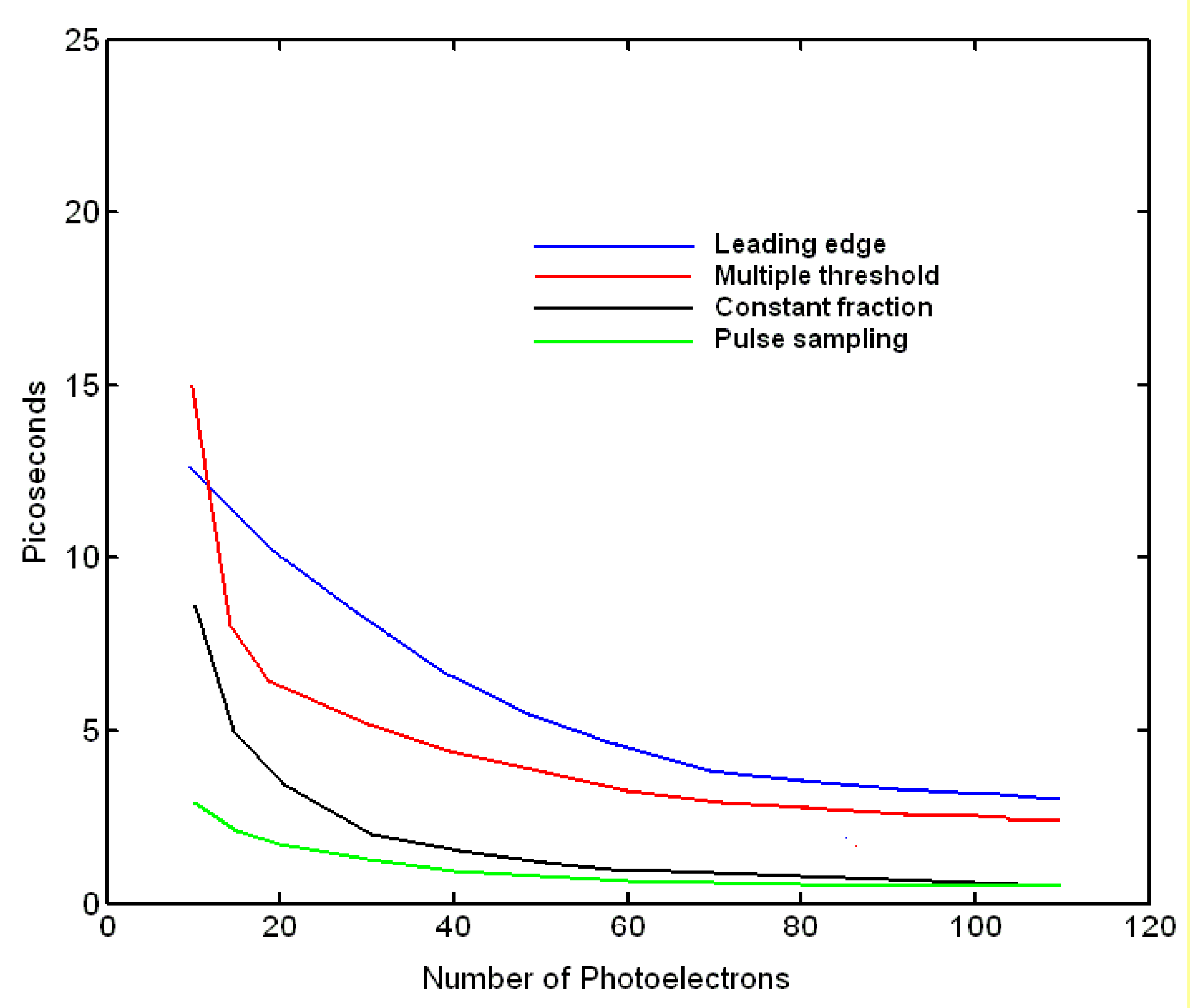
1. Other ways to make pores- e.g. Pierre Jarron's developments?
2. Who makes big photocathodes? (Pioneer?)
3. Who is interested in learning how to make big photocathodes for fast timing?
4. Is there a simulation of the internal workings of photo-cathodes out there somewhere?

# My Questions This Time-III

1. Can we get a serious simulation effort of the MCP functions started (collab with Lyon?)?
2. Funding from NSF Computing, SBIR, a a a a a European agency?
3. Are there MCP simulations already out there?
4. Can we find a Materials Science group with students, postdocs, etc. to work with us?

# Thank you

# Electronics Simulation-development of multi-channel CMOS readout




S/N=80

ABW= 1 GHz

Synthesized MCP signal

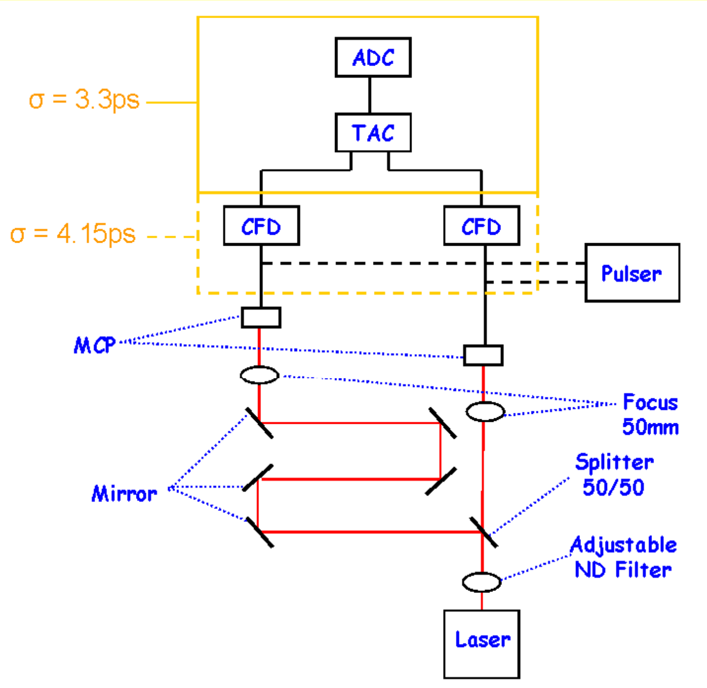
8 bit A-to-D

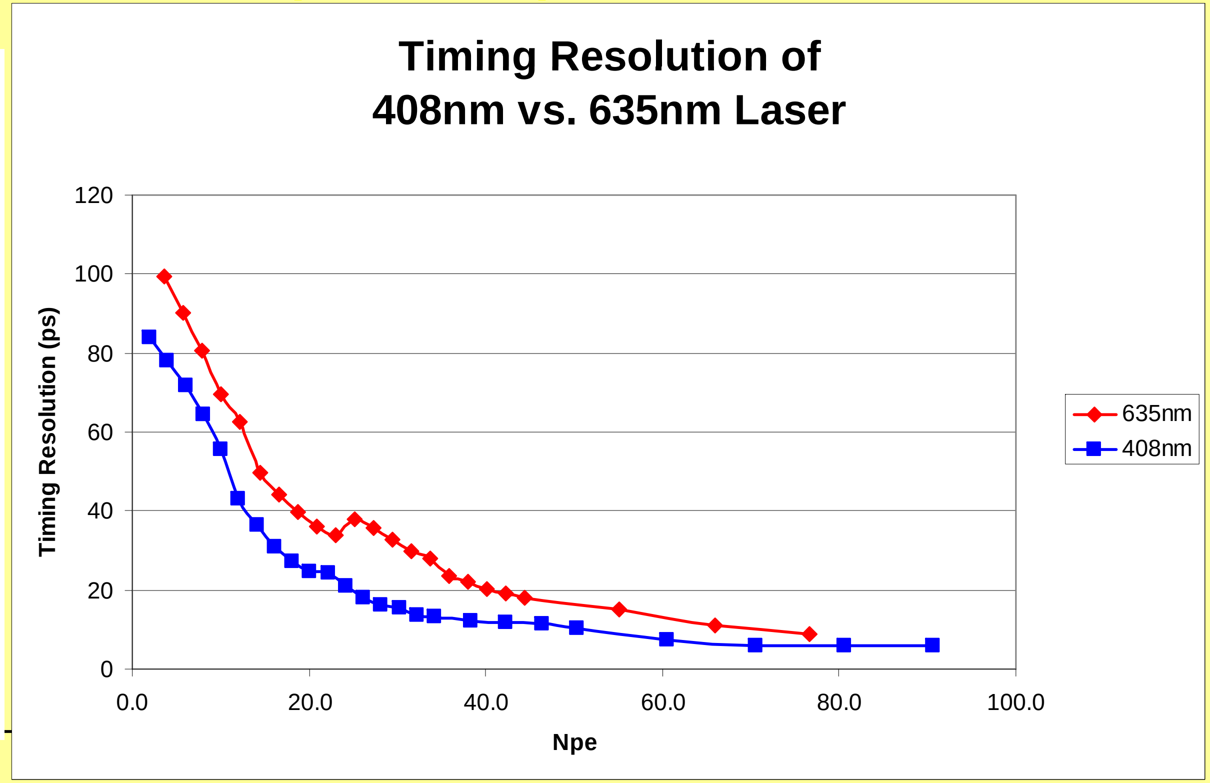
# Simulation and Measurement

- **Have started a serious effort on simulation to optimize detectors and integrated electronics**
- **Use laser test-stands and MTEST beam to develop and validate understanding of individual contributions- e.g. Npe, S/N, spectral response, anode to input characteristics,…**
- **Parallel efforts in simulating sampling electronics (UC, Hawaii) and detectors (UC,Saclay, Tom Roberts/Muons.inc).**

# Argonne Laser Lab

- Measure Δt between 2 MCP's (i.e root2 times σ); no corr for elect.
- Results: 408nm
  - 7.5ps at ~50 photoelectrons
- Results: 635nm
  - 18.3ps at ~50 photoelectrons

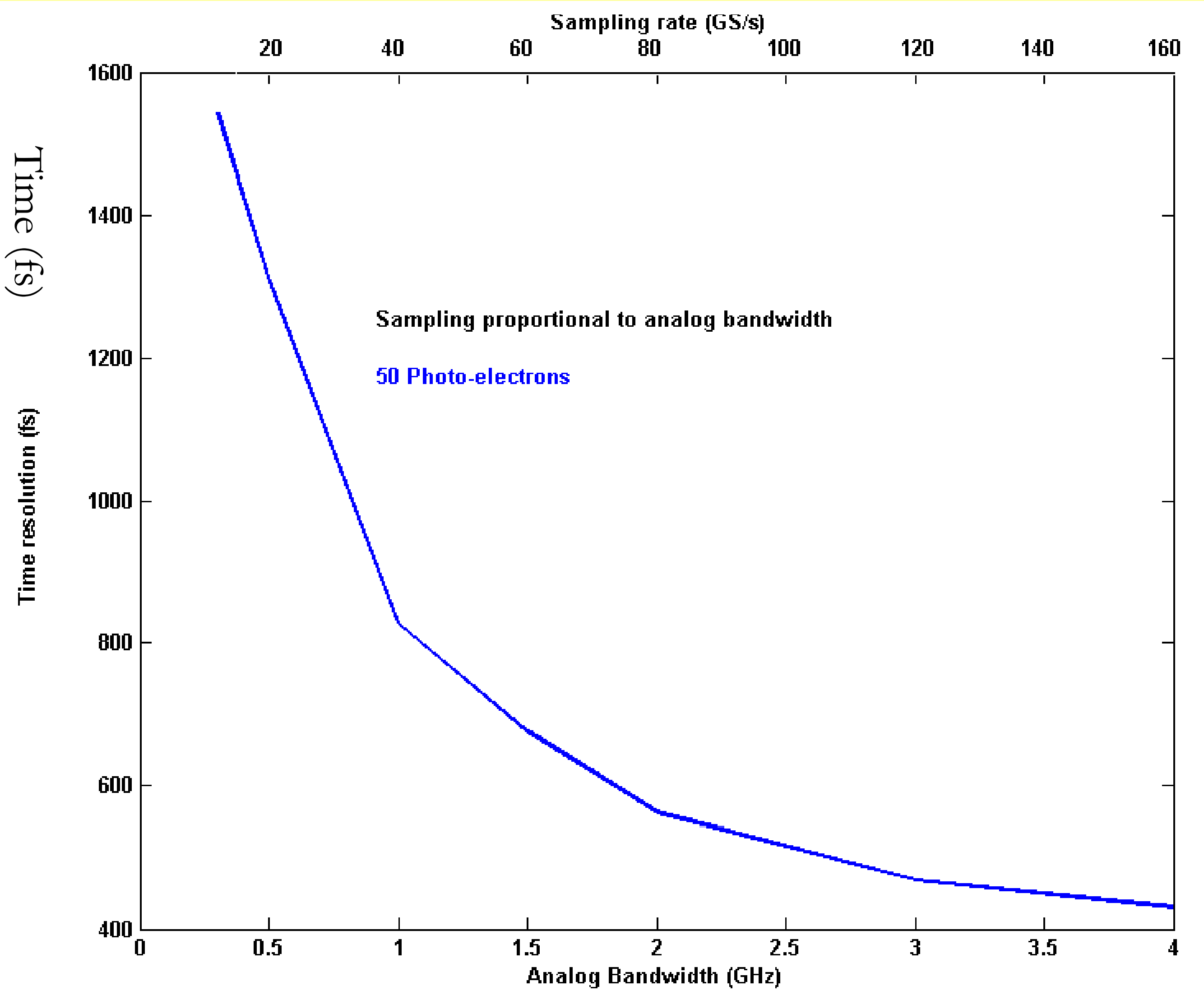


# Work in Progress

- **Our way of proceding- use laser test-stand for development, validation of simulation- then move to testbeam for comparison with simulation with beam.**
  - **Changes to electronics readout**
    - **Add Ritt and/or Varner sampling readouts (interleave 10 GS) –in works**
    - **First test via SMA; then integrate chips onto boards?**
    - **Development of 40 GS CMOS sampling in IBM 8RF (0.13micron)- proposal in draft (ANL, Chicago, Hawaii, Orsay, Saclay)**
  - **Changes to the MCPs**
    - **10um pore MCPs (two in hand)**
    - **Transmission-line anodes (low inductance- matched)- in hand**
    - **Reduced cathode-MCP_IN MCP_OUT-anode gaps- ordered**
    - **ALD module with integrated anode and capacitive**

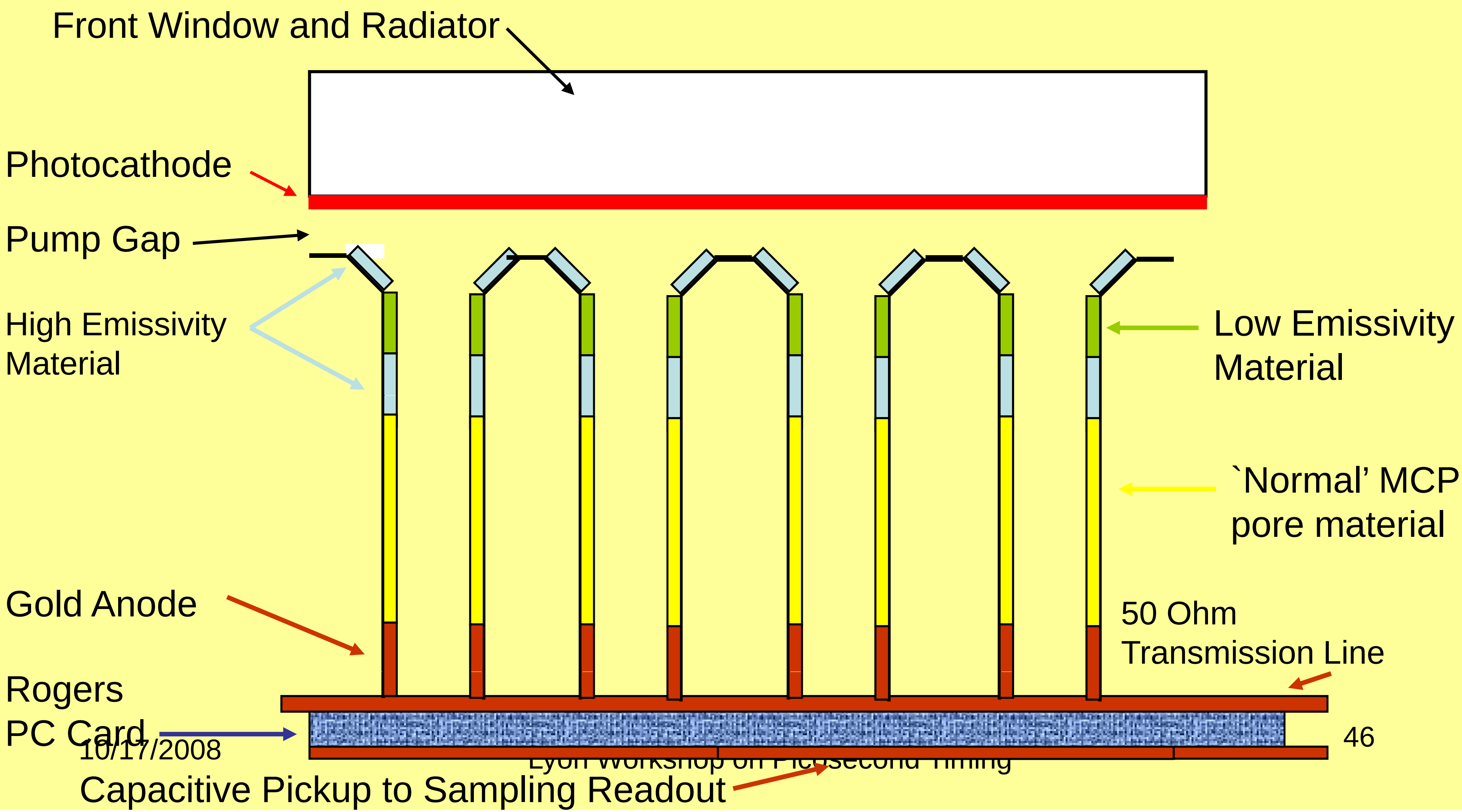
# Electronics Simulation- Sampling analog bandwidth on input at fixed S/N and sampling/ABW ratio




S/N=80
Synthesized MCP signal
8 bit A-to-D

Jean-Francois Genat

# Psec Large-area Micro-Channel Plate Panel (MCPP)- LDRD proposal to ANL (with Mike Pellin/MSD)



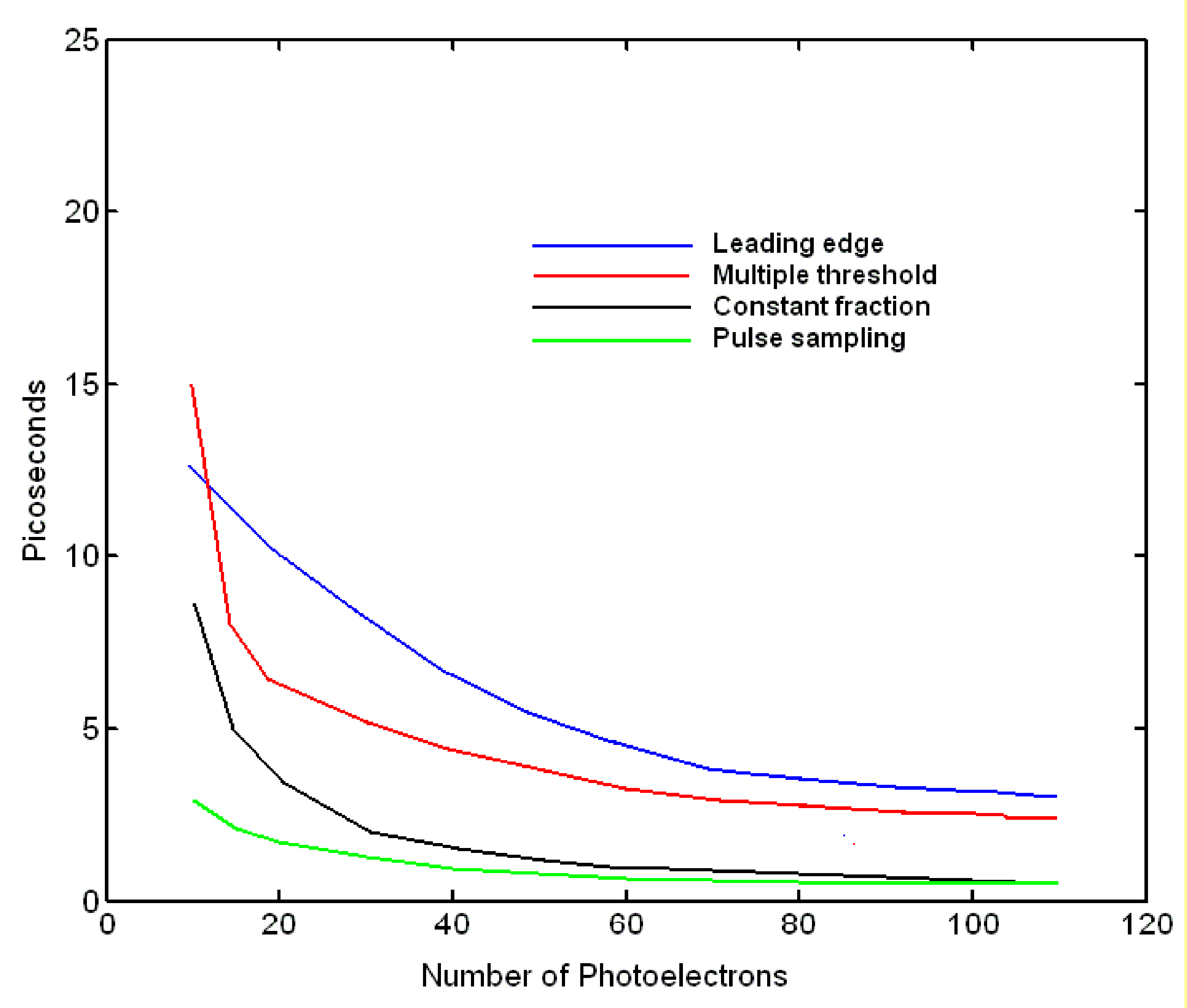
## II STATE OF THE ART

Several circuits have already been designed in the HEP community for fast pulse sampling, mainly to record photo-multipliers pulse shapes. As detailed in section I, fast timing requires higher sampling rates, but smaller dynamics ranges.

| | Hawaii | | Orsay/Saclay | | PSI | | PSEC |
|---|---|---|---|---|---|---|---|
| | Lab 3 | Planned Blab2 | Sam | Planned | DRS3 | Planned DRS4 | This proposal |
| Sampling frequency | 20 MHz-3.7 GHz | 1-10 GHz | 0.7-2.5 GHz | 10 GHz | 10 MHz-5 GHz | 5 GHz | 40 GHz |
| Analog bandwidth | 900 MHz | 850 MHz | 300 MHz | 650 MHz | 450 MHz | > DRS3 | >1 GHz |
| Number of Channels | 9 | 16 | 2 | | 12/6/2/1 | 8/4/2/1 | 16 |
| Triggered mode | Common Stop | Channel trigger on sums | Common Stop | | Common Stop | Common Stop | Channel trigger |
| Resolution | | 10 bit | 11.6 bit | | 11.6 bit | 11.5 bit | 8-10 bit |
| Samples | 256 | 4/8 rows of 512 | 256 | 2048 | 1024-12288 | 1024-8192 | 64 |
| Clock | 33 MHz | 33 MHz | 66 MHz | | 20 MHz | fsamp/2048 | 60 MHz |
| Max latency | | | 5ms | | 0.6 ms | | |
| Input Buffers | | TIA (5kOhm gain) | Yes | No | No | No | Yes |
| Differential Inputs | No | Pseudo-diff | Yes | | Yes | Yes | Pseudo diff |
| Input impedance | 50 Ohms Ext | 30-70 Ohms adjustable | > 10 MOhm | | | 7-11pF | |
| Readout clock | | 1 GHz Wilkinson | 16 MHz | | 33 MHz | 33 MHz | 60 MHz |
| Readout time | 150µs | 512µs | < 2 µs | | 30ns * n samples | 30ns * n samples | < 1 µs |
| Locked delays | Ext DAC | Ext DLL | Int DLL | | Ext PLL | Int PLL | |
| On-chip ADC | Yes | 1 GHz Wilkinson | No | | No | No | Yes |
| R/W simultaneous | | Yes | No | | No | Yes | No |
| Power/ch | 50mW | 20mW/sample 0.2W/read | 150 mW | | 1-13mW | 2-20mW | |
| Dynamic range | | 1mV/1V | 0.65mV-2V | | 0.35mV/1.1V | 0.35/1V | 1V |
| Xtalk | Average << 10% | < 0.1% | 0.30% | | <0.5% | <0.5% | |
| Sampling jitter | | TBD | 40ps | | 200ps (Ext PLL) | Ext PLL | 10ps |
| Power supplies | 2.5V | 2.5V | 0-3.3V | | 2.5V | 2.5 V | 1.8V |
| Process | TSMC 0.25 | TSMC 0.25 | AMS 0.35 | AMS 0.18 | UMC 0.25 | UMC 0.25 | CMOS 0.13 |
| Chip area | 2.5 mm2 | 12 mm2 | 10 mm2 | | 25 mm2 | 25 mm2 | 1 mm2 |
| Cost/channel | | 500$/40 10$/2k | 15.7$/12k | | | 10-15$ | |

Table 1. State of the art, this proposal. The yellow column is from Gary Varner's group at the University of Hawaii (USA) [12], the light blue from Dominique Breton from the University of Paris-Sud (Orsay) [10] and Eric Delagnes from CEA (Saclay), (France) [11]. The orange column from Stefan Ritt at PSI (Switzerland) [13]. The dark blue is this proposal.

# Electronics Simulation-development of multi-channel CMOS readout




S/N=80

ABW= 1 GHz

Synthesized MCP signal

8 bit A-to-D

# Jerry's #'s re-visited : Solutions to get to <several psec resolution.

1. **TTS: 3.8 psec (from a TTS of 27 psec)**

   **MCP development- reduce TTS- smaller pores, smaller gaps, filter chromaticity, ANL atomic-deposition dynodes and anodes.**

2. **Cos(theta)_cherenk 3.3 psec**

   **Same shape- spatial distribution (e.g. strips measure it)**

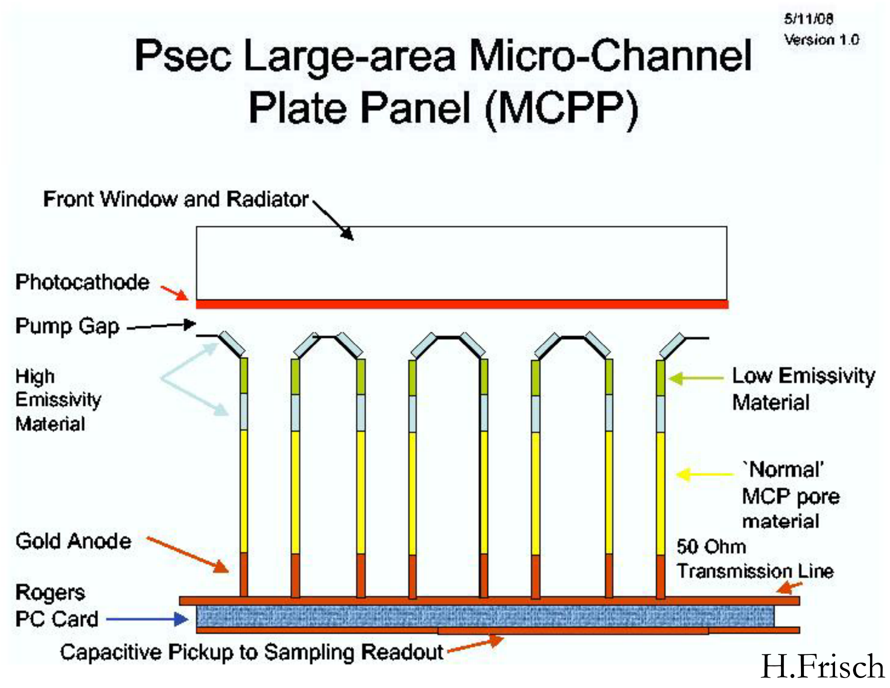
3. **Pad size 0.75 psec-**

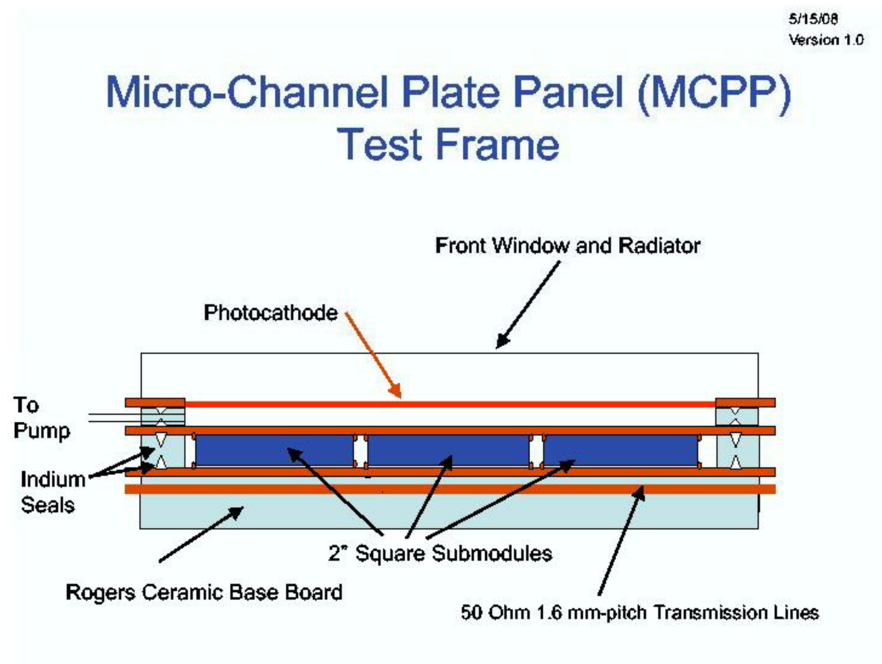
   **Transmission-line readout and shape reconstruction**

4. **Electronics 3.4 psec –**

   **fast sampling- should be able to get < 1psec**

# Muon Cooling position/time station design- LDRD (ANL) proposal



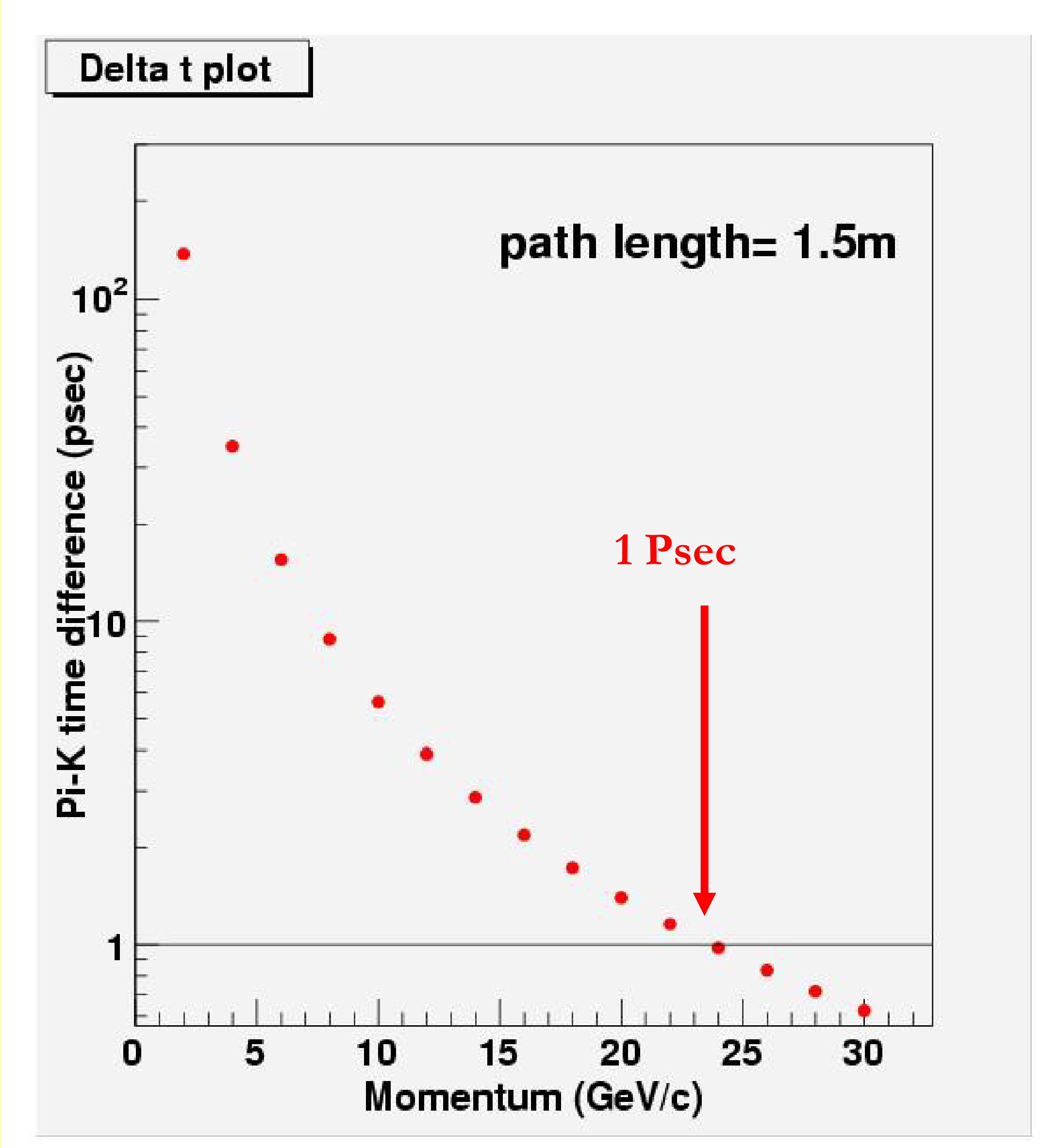




Cartoon drawings showing the custom atomic-layer disposition, the small pores, and the custom anode configuration (left) and our proposed module frame (right)

# Summary

- Next step is to make anodes that give both position and time- hope is few mm and << 10 psec resolutions. This would allow systems of (say) 6” by 6” size with ~100 channels- good first step.
- Muon cooling is a nice first application of psec tof- not to big, very important, savings of money.
- We have made a number of false starts and wrong turns (e.g. the IBM bipolar 200 GHz electronics), but the fundamentals look good- don’t see a hard limit yet.

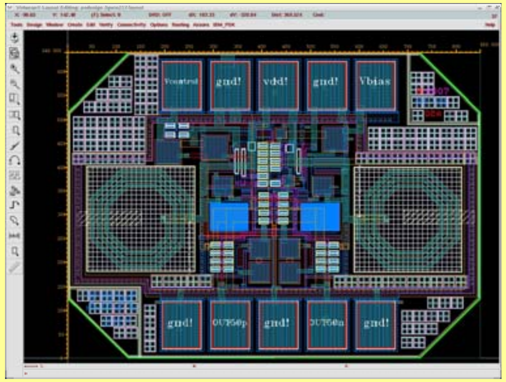
# K-Pi Separation over 1.5m

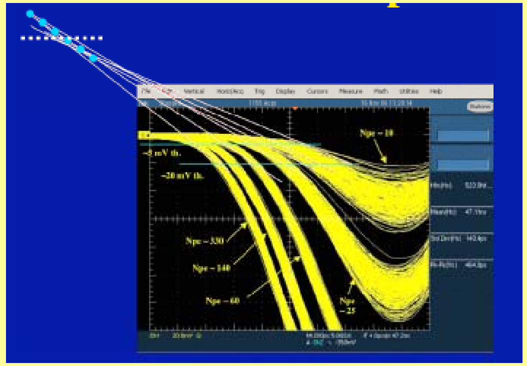



Assumes perfect momentum resolution (time res is better than momentum res!)

# Engineering Highlights

- F.Tang (UChicago) designed Voltage Control Oscillator using IBM 0.13um SiGe BiCMOS8HP
- More challenging - Time Stretcher chip (including ultra low timing jitter/walk discriminator & dual-slope ramping time stretching circuits etc.)
  - From simulations, accuracy not good enough (5-10 psecs) F.Tang
  - Power concerns
- NEW: Invented 2 new schemes - a) Multi-threshold comparators, b) 50 GHz 64-channel waveform sampling. Both schemes give energy and leading edge time.
- Current plan:  Save waveform and use multiple thresholds to digitize.   Use CMOS (J.F. Genat, UChicago)
  - Dec meeting at UChicago with UChicago, ANL, Saclay, LBL & Hawaii, IBM and Photonis





# MCP Best Results

## Previous Measurements:

– Jerry Va'vra SLAC (Presented at Chicago Sep 2007)

- Upper Limit on MCP-PMT resolution: $\sigma_{\text{MCP-PMT}} \sim 5$ ps

Burle/Photonis MCP-PMT 85012-501
(64 pixels, ground all pads except one)

•Using two 10 um MCP hole diameter

•PiLAS red laser diode (635 nm)

•1cm Quartz radiator (Npe ~ 50)

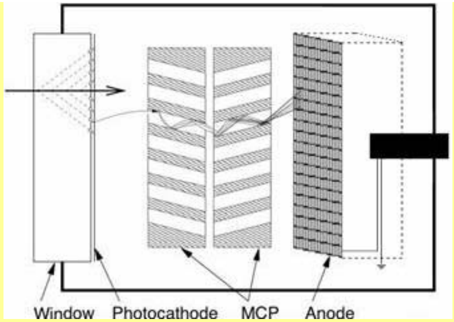
– Takayoshi Ohshima of University of Nagoya (Presented at SLAC Apr 2006)

- Reached a $\sigma_{\text{MCP-PMT}} \sim 6.2$ps in test beam


•Use 2 identical 6 micron TOF detectors in beam (Start & Stop)

•Beam resolution with qtz. Radiator (Npe ~ 50)

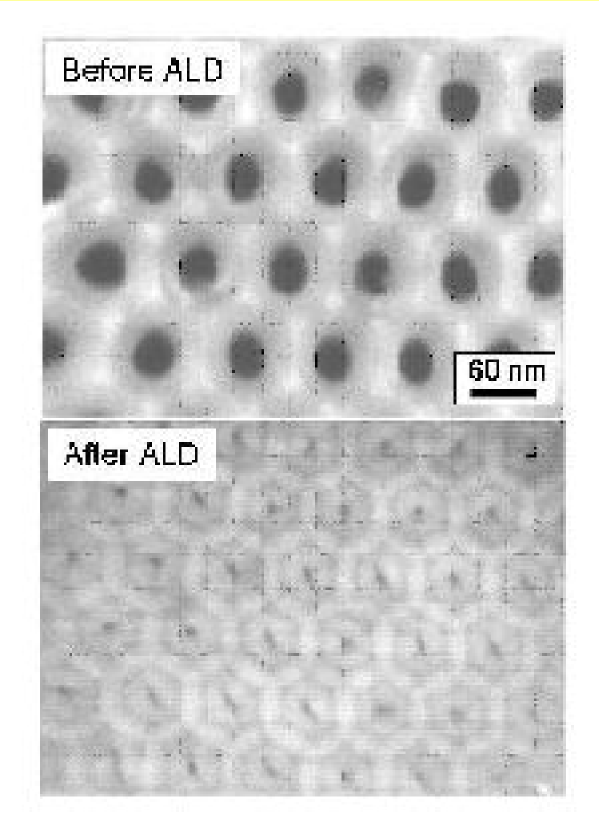
# R&D of MCP-PMT Devices




We are exploring a psec-resolution TOF system using micro-channel plates (MCP's) incorporating:

- A source of light with sub-psec jitter, in this case Cherenkov light generated at the MCP face (i.e. no bounces): Different thicknesses of Quartz Radiator
- Short paths for charge drift and multiplication: Reduced gap
- A low-inductance return path for the high-frequency component of the signal:
- Optimization of the anode for charge-collection over small transverse distances:
- The development of multi-channel psec-resolution custom readout electronics directly mounted on the anode assembly: ASIC, precision clock distribution
- Smaller pore size: Atomic Layer Deposition

# Atomic Layer Deposition



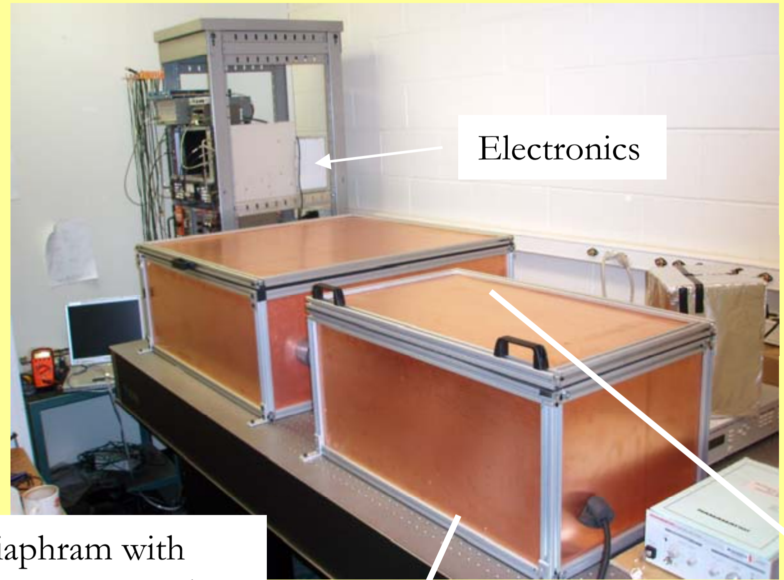

- ALD is a gas phase chemical process used to create extremely thin coatings.
- **Current 10 micron MCPs have pore spacing of 10,000 nm**. Our state of the art for Photonis MCPs is 2 micron (although the square MCPs are 10 micron).
- **We have measured MCP timing resolution folk-lore is that it depends strongly on pore size, and should improve substantially with smaller pores (betcha).**

M.Pellin, MSD

Karen Byrum slide, mostly

# FY-08 Funds –ANL

## Laser Test Stand at Argonne




**Hamamatsu PLP-10 Laser (Controller w/a laser diode head) 405 & 635nm head.**

**Pulse to pulse jitter < 10psec (Manufacture Specs)**