New trends in semiconductor detectors

Shaun Roe, CERN

New trends

- Recent History
- Review of the problem
- Silicon
  - Novel geometries: MAPS, 3D, Defect engineering: Cold, Oxygenated
- 'New' materials
  - Diamond, amorphous silicon, Silicon carbide
- Other ideas…
  - Depfet, new pixel layout

Potted history

- Rewind twelve years (pre-web!):
  - Silicon detectors operated to 100V
  - Irradiations to 10^{13} neutrons/cm^2 started, didn't look promising
  - Some LEP detectors showing radiation damage
  - Double sided detectors looked good (?)
  - Analogue electronics, water cooling, copper power and readout, OS9, PAW, FORTRAN, dial&read detector testing…

Recent history

- Last ten years of HEP investigations for LHC
  - Ordinary photodiodes investigated in neutron, proton and gamma sources reveals initially that the leakage current increases but anneals. Increase in operating voltage also seen, and capacitance effects. (RD2, RD20)
  - Increase in operating voltage seen to further increase after irradiation, and be very temperature dependent. (UCSC, RD20, RD2). Model proposed by Lindstrom, Fretwurst.
  - First projections of the model to LHC scenario show the detectors are unworkable unless kept cold, and even then there is a danger. Principle problem identified as the depletion voltage.
  - All subsequent improvements to LHC detectors have concentrated on the depletion voltage problem.

Todays snapshot

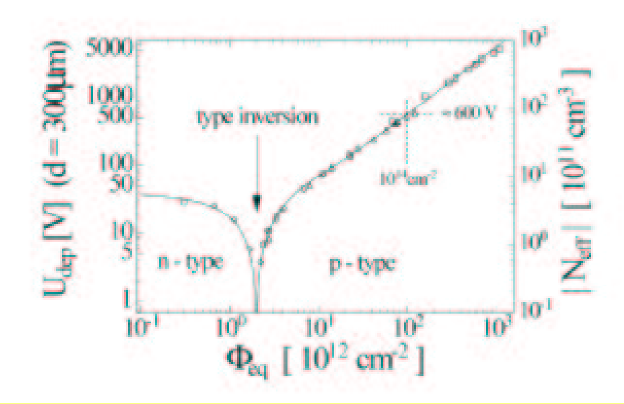
- Detectors far more robust, but cooled
  - Operate routinely to 500V
  - Evaporative or refrigerant cooling
  - Routine irradiations to >3 x 10^{14} n/cm^2
- Systems evolution
  - Optical readout
  - Cables, hybrids more adventurous
  - Testing with LabView, Linux, C++, NI-VXI or PCI (USB soon?), logic in FPGAs…

A modern module

QuickTime™ and a TIFF (Uncompressed) decompressor are needed to see this picture.

Review of radiation problems (1)

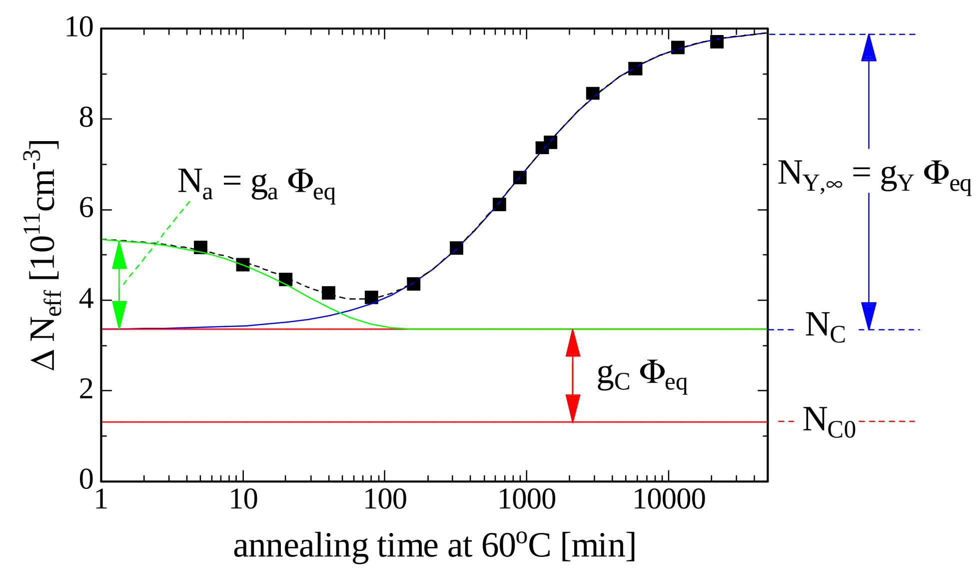
- Most obvious: Leakage current, giving rise to noise
  - Not such a problem at small shaping times
  - 3.99 x 10^{-17} A/cm (1MeV n)
- 'LHC era' problem of depletion voltage rising beyond operable limits



Michael Moll, CERN

Review of radiation problems(2)

- 'Reverse annealing'
  - Depletion voltage continues to change after irradiation
  - Strongly temperature dependent
- 'Hamburg model'



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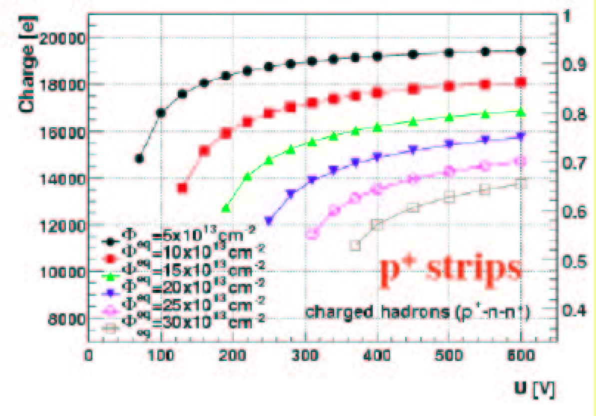
$$\Delta N_{eff}(\Phi_{eq},t) = N_a(\Phi_{eq},t) + N_C(\Phi_{eq},t) + N_Y(\Phi_{eq},t)$$

= **beneficial annealing** + **stable damage** + **reverse annealing**

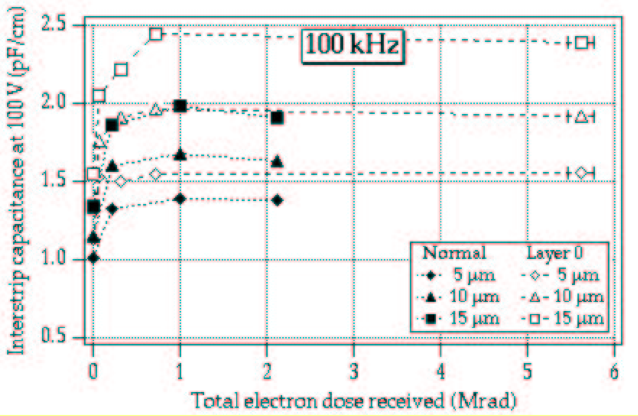
Review of radiation problems(3)

- Trapping: some charge simply 'disappears'



Gregor Kramberger, Ljubljana

- Secondary effects: increase in capacitance



Richard Wheadon, RD20

Looking forward

- New colliders may be ten times the luminosity of LHC
  - Principle challenge (for an SCT) is in the sensors
  - Depletion voltage remains a problem
  - Trapping becomes more significant
- Different approaches adopted
  - Geometrical: reduce the collection/depletion distance so a lower voltage can be used
  - Material: treat the silicon or use a different material to reduce radiation damage

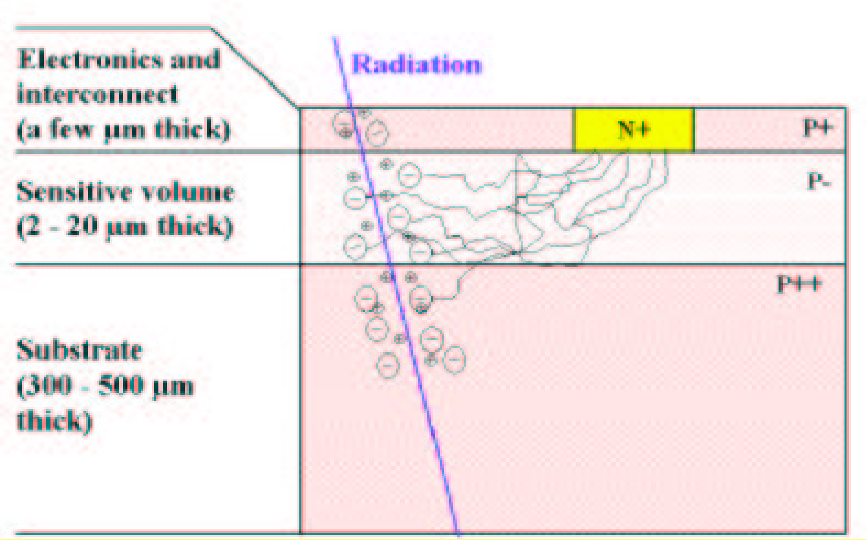
MAPS: Monolithic active pixel sensors

- Sensitive detector layer is manufactured with the electronics

  Active Pixel Sensor technologies have been around since 1993 for commercial application

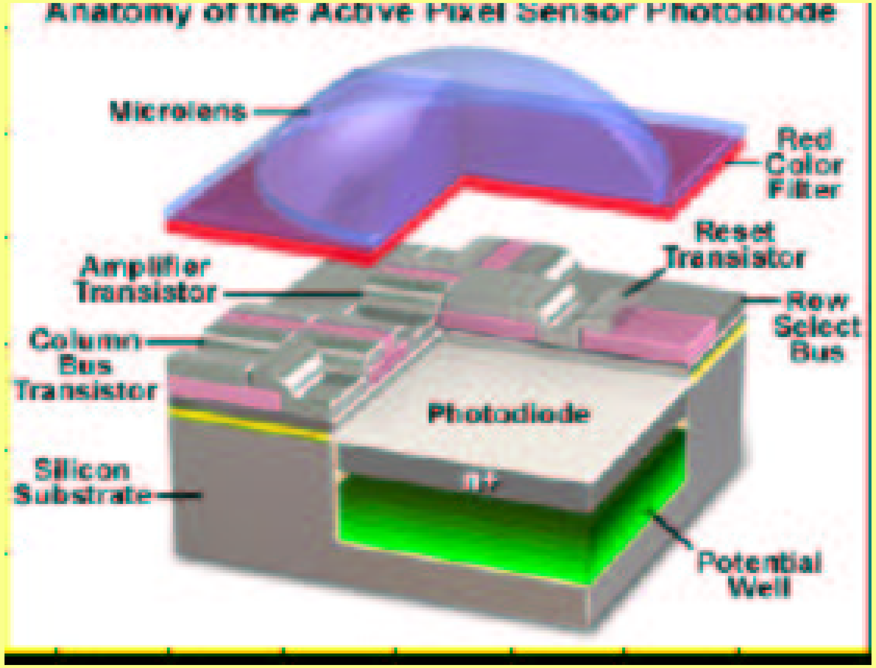
  Specific designs required for HEP application (1999)

  Groups: Strasbourg, RAL (thanks: Renato Turchetta)



NIM A458(2001) 677-689

MAPS tests



First prototype: 512x512

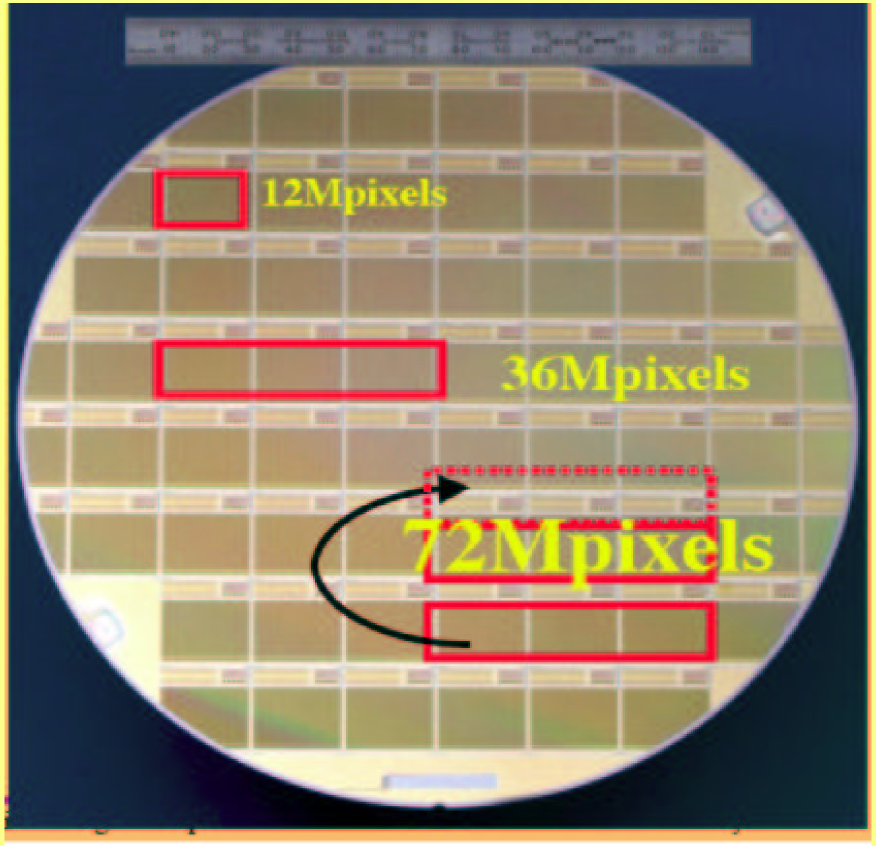
MAPS design for HEP/space

- Specific design necessary:

– To increase active area ratio	already achieved
– Low noise, high dynamic range, faster	specific CMOS design
– Thin sensors for reduced material	Backthinning to 50μm achieved
– Sensors should be larger than the reticle	Stitching or clever dicing investigated
– Radiation resistance	Apply bias to epitaxial layer

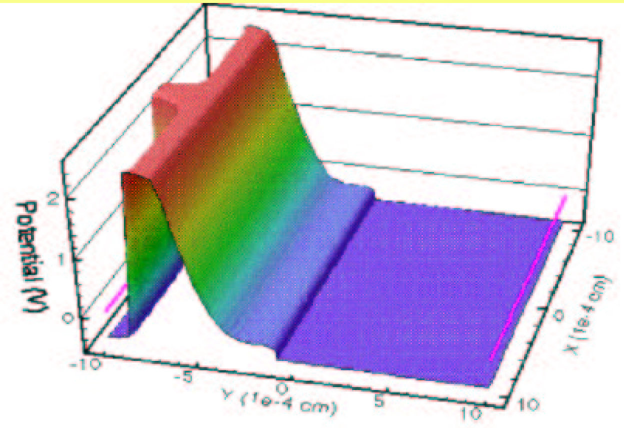
MAPS beam tests

- 99.5% efficiency
- S/N of 40 (20μm thick epitaxy)
- 1.5μm resolution on 20μm pitch
- Deterioration seen at 6kGy, 10^{11}p/cm^2



MAPS for the future

- Radiation hardness needs to be addressed
  - Present design uses diffusion so is slow and prone to carrier lifetime degradation (trapping)
  - Applying a detector bias should be possible to speed collection and minimize trapping



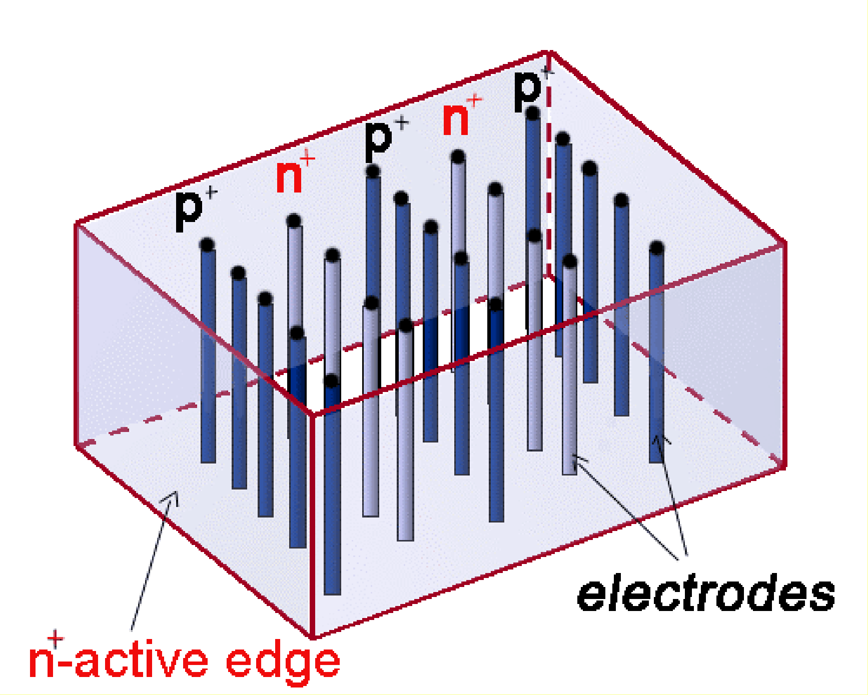
potential

Biasing structure

'3D' detectors

- Using MEMS (micro electro mechanical systems) techniques, vertical junctions are made (MBC, Brunel, Hawaii)

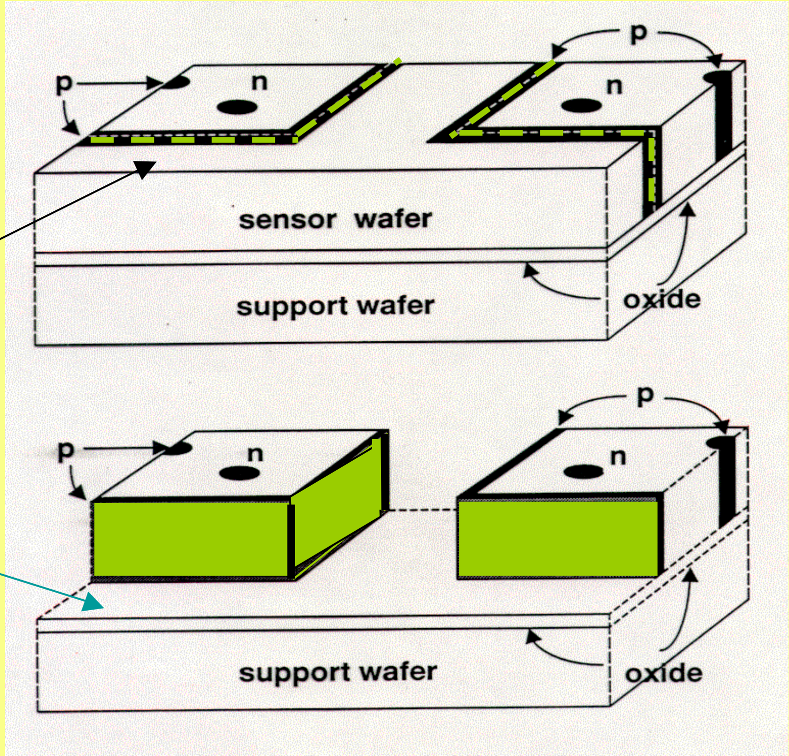
❖ **NIMA 395 (1997) 328**
❖ **IEEE Trans Nucl Sci 46 4 (1999) 1224**
❖ **IEEE Trans Nucl Sci 48 2 (2001) 189**
❖ **IEEE Trans Nucl Sci 48 6 (2001) 2405**
❖ **IEEE Trans Nucl Sci 48 5 (2001) 1629**
❖ **CERN Courier, Vol 43, Number 1, Jan 2003**



With thanks to: Cinzia daVia

3D-processing

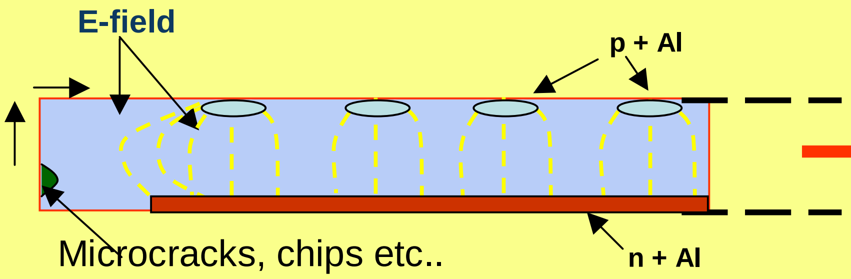
- Undergoing tests for TOTEM: edgeless operation is important

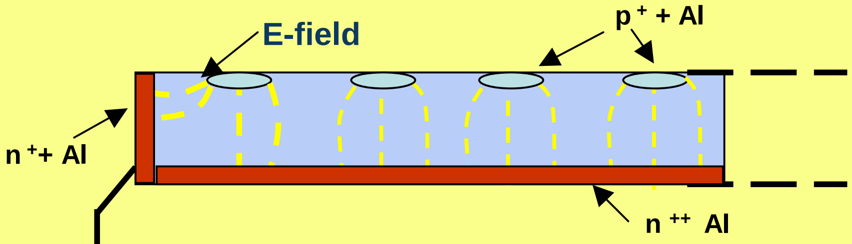


A trench is etched and doped to make a contact

After the first steps, the material around the detectors is etched away and the support removed: no sawing is required

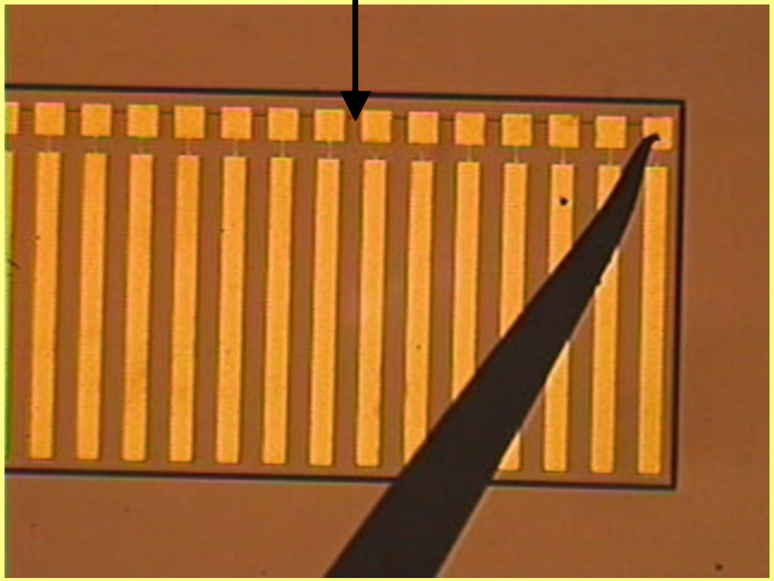
3D: 'Edgeless' detectors





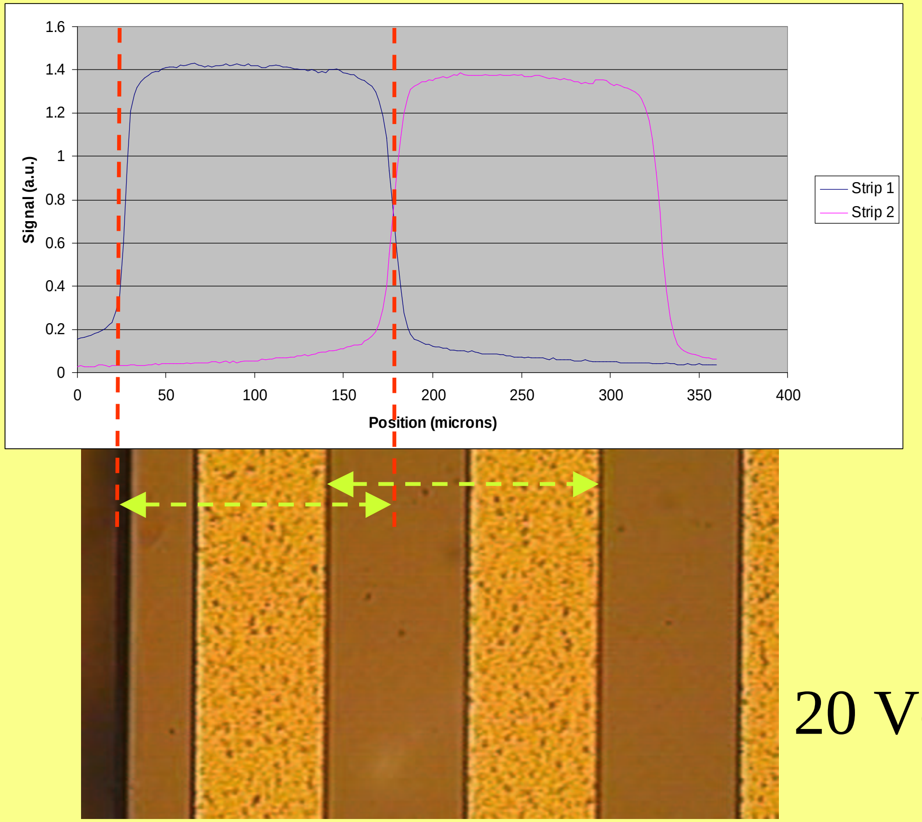
GUARD RING
Sinks surface leakage current

Planar 3D
Sinks surface leakage current



- 30 μm pitch strips
- 240 μm thick
- n-type silicon
- ρ=10 kΩcm
- 3 x 4 mm^2

3D: 'Edgeless' detectors

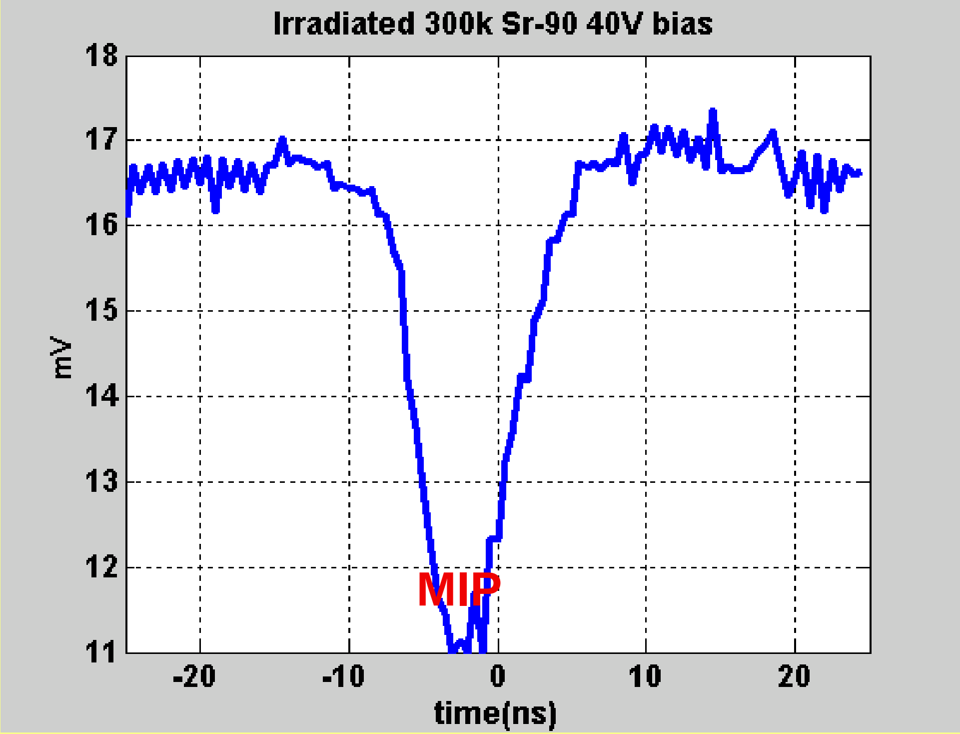


20 Volts Bias

- X ray microbeam scanned across the detector
- Measured 'dead' region is only 5μm at the edge of the detector

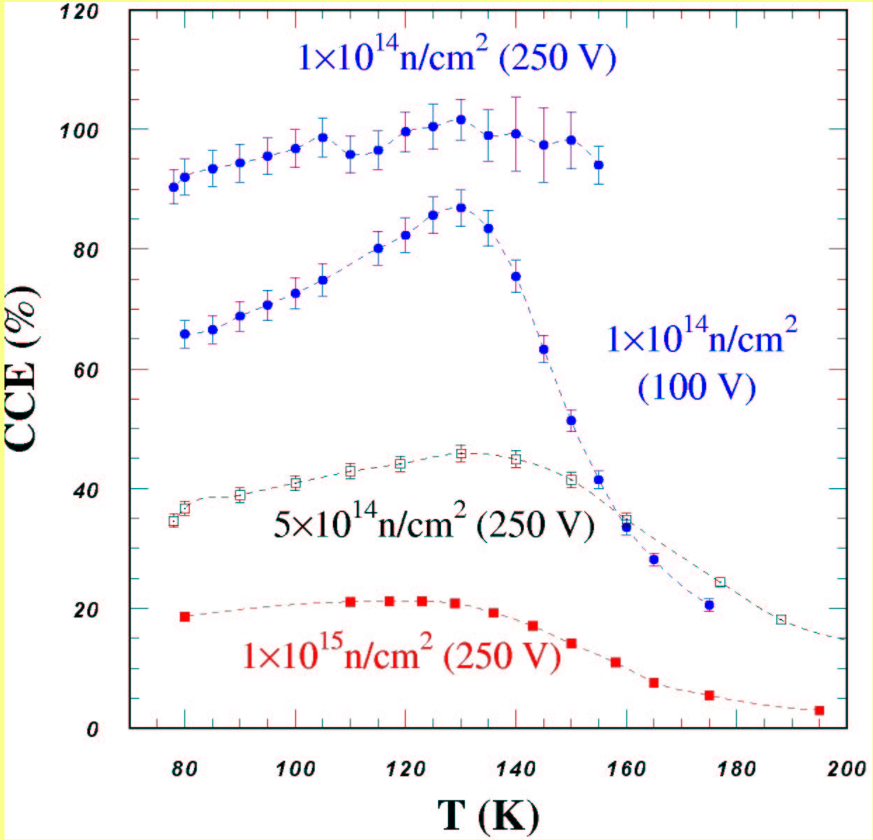
3D: Radiation hardness

- Irradiated to 10^{15} p/cm^2
  - Bias voltage 40V (max beneficial annealing)
  - Risetime 3.5ns, <10ns width
  - CCE 60%
  - Irradiated, stored, measured at 20°C
- Results also exist for 2×10^{15} p/cm^2
  - Different storage conditions



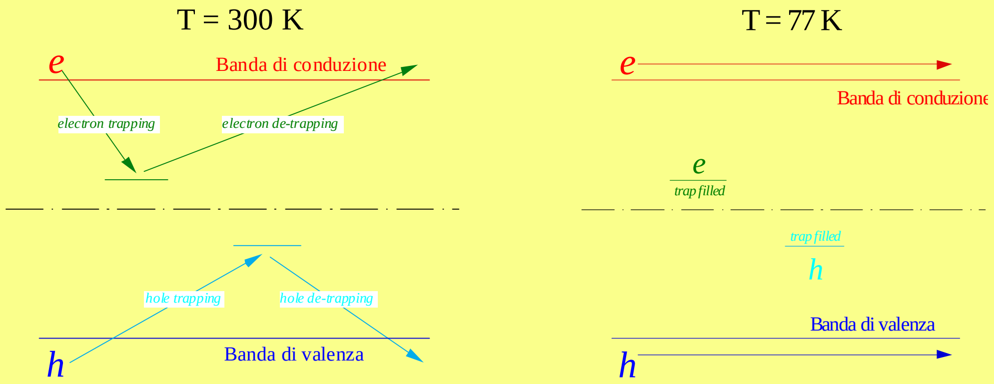
Cold Silicon

- Relies on freezing of the contributing traps
  - Requires 140K or below
  - Addresses both operating voltage and charge trapping problem



Thanks to: Gennaro Ruggiero

Cold silicon: Lazarus effect



T = 300 K

e

Banda di conduzione

electron trapping

electron de-trapping

hole trapping

hole de-trapping

Banda di valenza

h

T = 77 K

e

Banda di conduzione

e

trap filled

trap filled

h

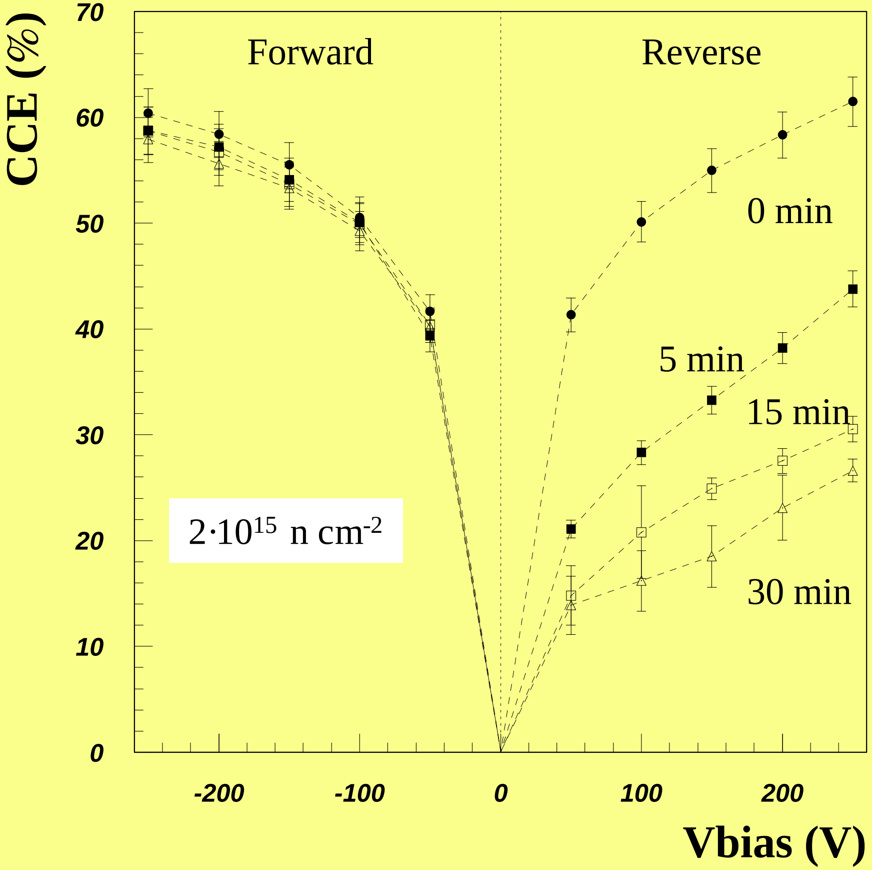
Banda di valenza

h

$$CCE \propto \left(\frac{d}{D}\right)^2 \exp\left(-\frac{t_{drift}}{\tau_{trap}}\right)$$

- Trap emission time becomes very long
  - Traps fill up and no longer contribute to electrical behaviour

Cold silicon



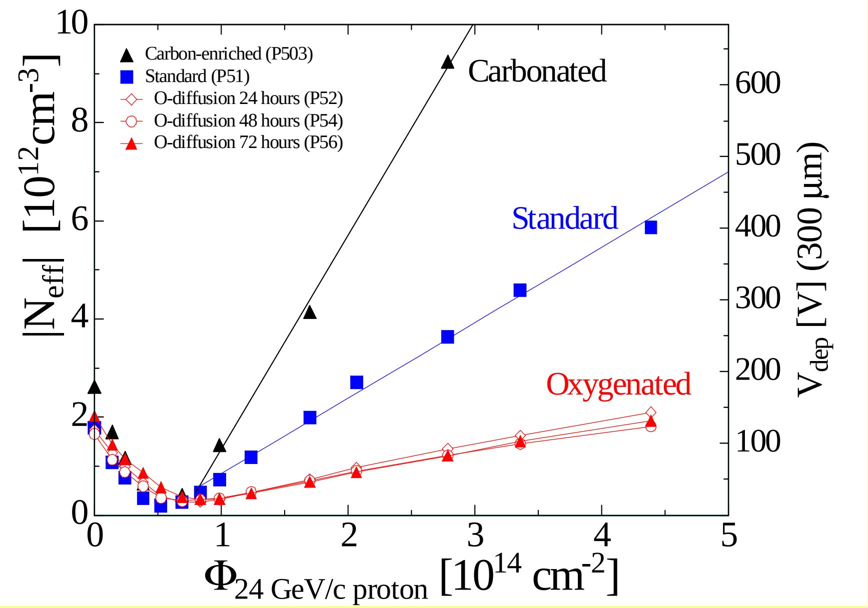
- Both forward and reverse biasing is possible
- Edgeless operation is being investigated

Cut edge at
0, strips
25µm

QuickTime™ and a TIFF (LZW) decompressor are needed to see this picture.

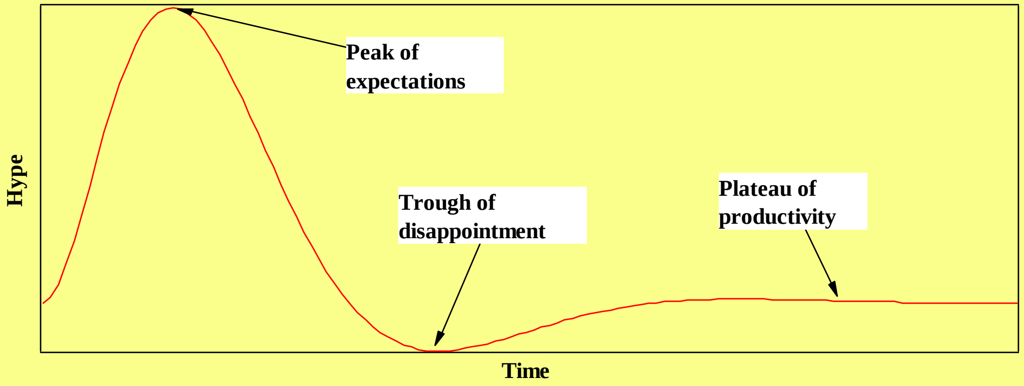
Oxygenated silicon

- Defect kinetics approach
  - Attempts to understand the microscopic causes of radiation damage
  - First studies implicated oxygen and carbon in the defect creation process
  - Diffusion oxygenated float zone silicon (DOFZ) investigated



Thanks to: Michael Moll

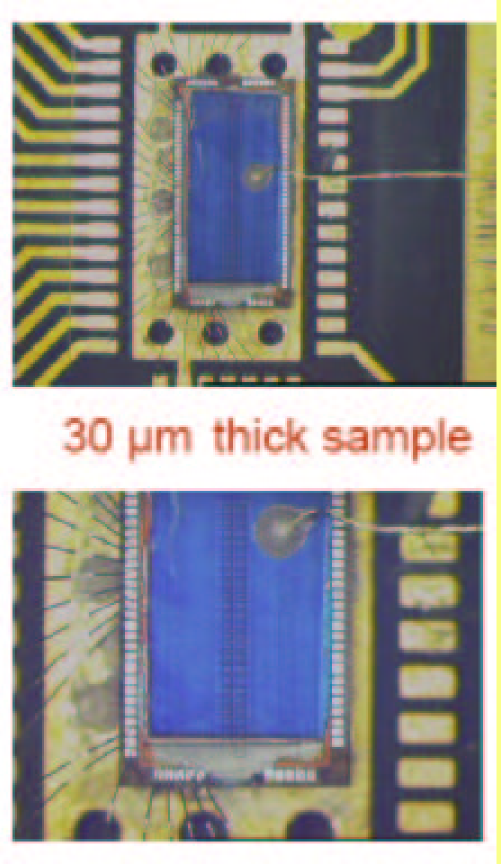
New materials



- ‘New material syndrome’
  - Other materials not as commercially important as silicon, tend to be technologically less mature
  - Typical problems are trapping and obtaining uniform material (and money)

Amorphous silicon

- Hydrogenated amorphous silicon
  - Initial work (1985-1995) produced only small signals
  - MAPS approach now being tried
    - Layers of 10-30μm can be deposited
    - Aim is to fully deplete and achieve charge transition of 10ns or less


30 μm thick sample

Thanks To: Pierre Jarron

S. Roe, Erice 28 September-4 October 2003

Amorphous silicon: technology

- Plasma Enhanced Chemical Vapour Deposition (PECVD)
  - Low temperature (220°C)
  - 6 hours for a 30µm layer
  - Silane decomposition

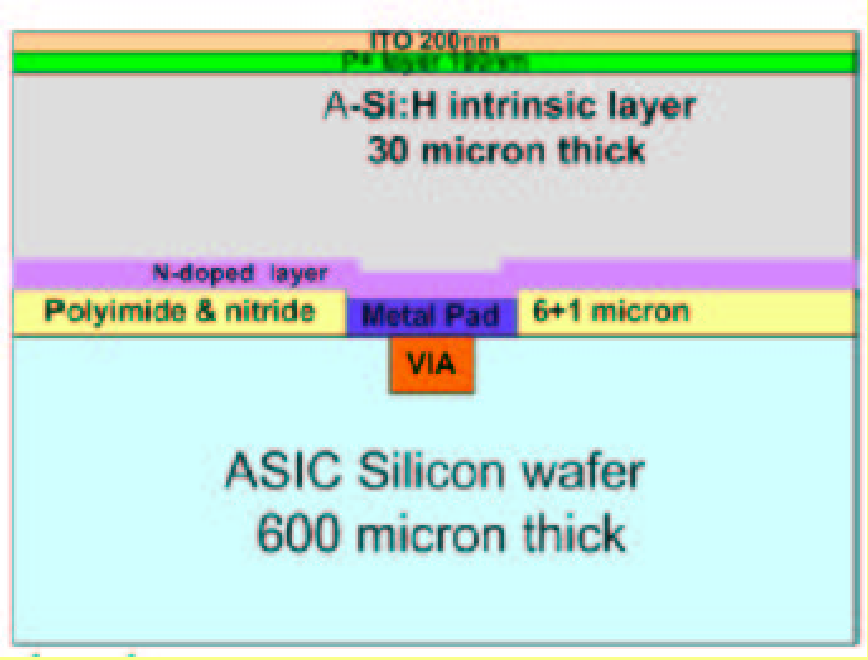
Amorphous silicon: properties

	c-Si	A-Si:H
Density [g/cm^3]	2.3	2.25
Hole mobility [cm^2/Vs]	1350	2-5
Electron mobility[cm^2/Vs]	480	0.005
Bandgap [eV]	1.12	1.7-1.8
W [eV]	3.6	4-4.8

- Band structure is complex
- Defect density is ~10^{15}/cm^3, charge lifetime depends strongly on this
- Trapping sites (incl. Radiation produced) are compensated by highly mobile H

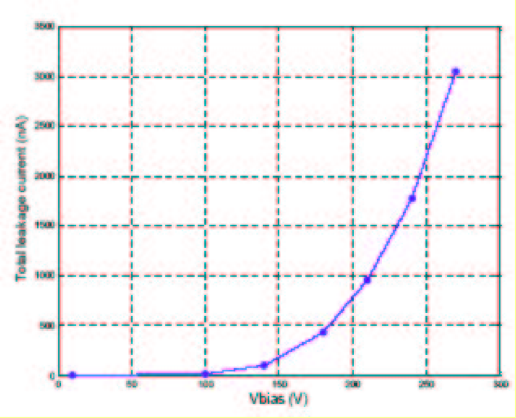
Amorphous silicon: devices

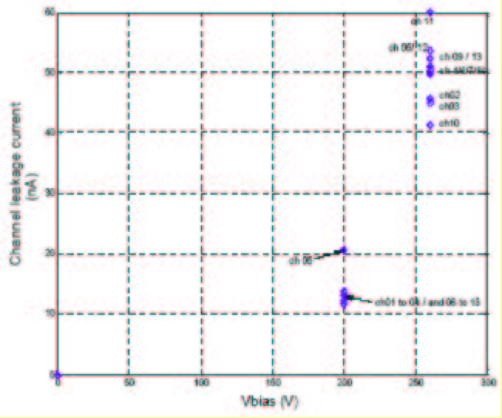
- Multilayer composition
  - Bottom thin n-doped layer (20nm)
  - Middle thick i-layer (5-30μm)
  - Top thin p-doped layer (40nm)
  - Indium Tin Oxide (100nm)
  - 13μm and 30μm thick layer devices have been made with 94 x 68μm pixels



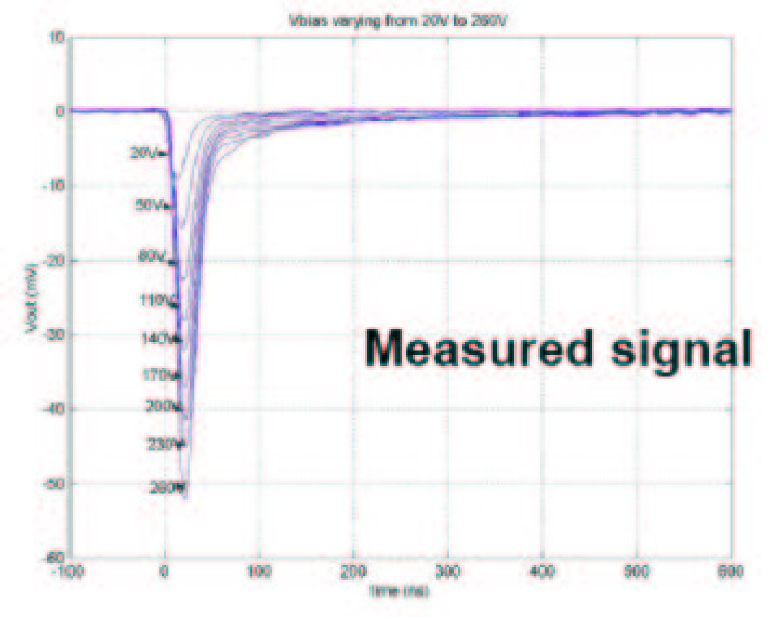
Amorphous Silicon: DC characteristic

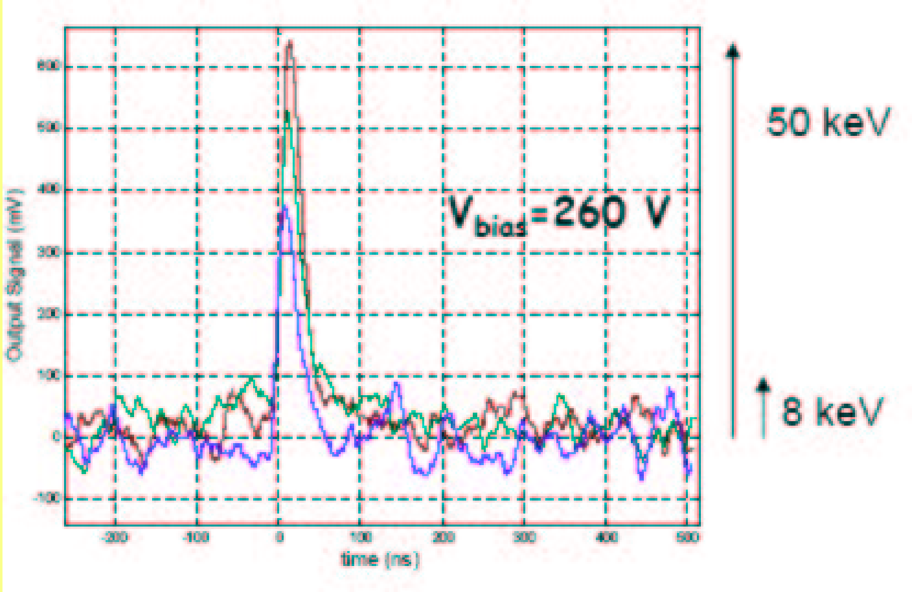
- Leakage current
  - Pixel leakage 10nA at 200V, 40nA at 250V
  - 'soft' breakdown characteristic
- Depletion
  - Full depletion ~400V for 30μm





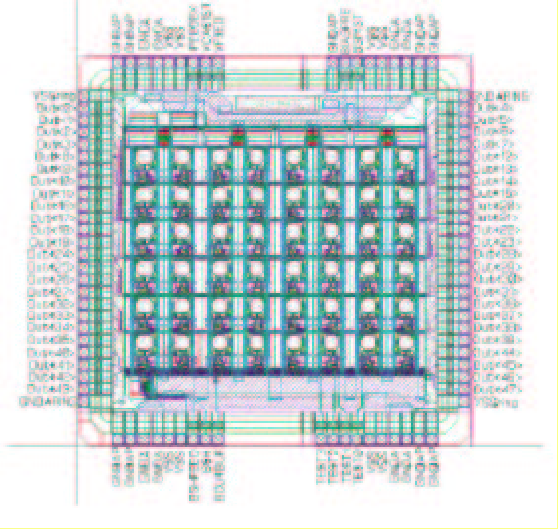
Amorphous silicon:signal response

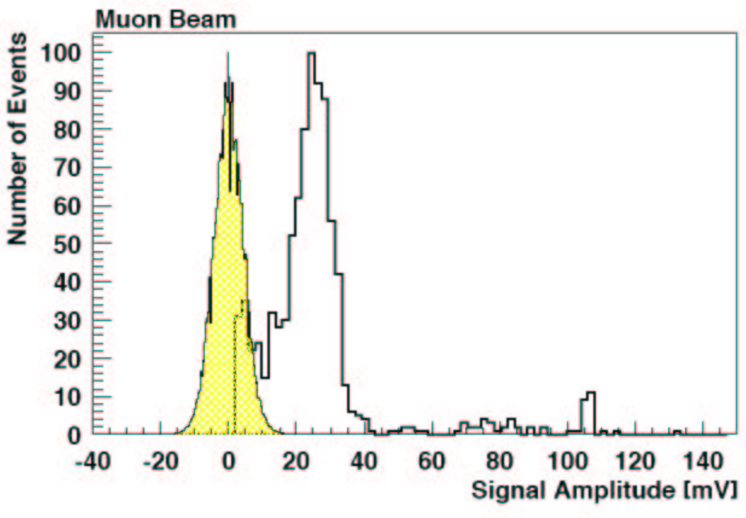




- Results shown for 30μm thick layer
  - Signal of 2400 e-/30μm (not fully depleted!)

Amorphous silicon: in beam

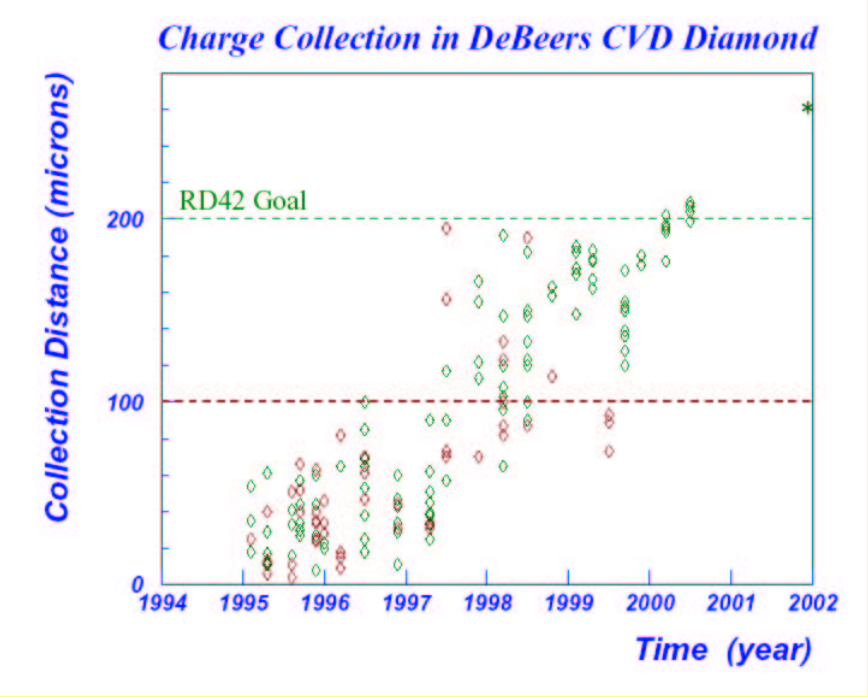




- Macropad chip used
  - 6 x 8 pixels, 380μm pitch, 20 e- ENC, 130ns peaking time
  - Still very preliminary!

Diamond

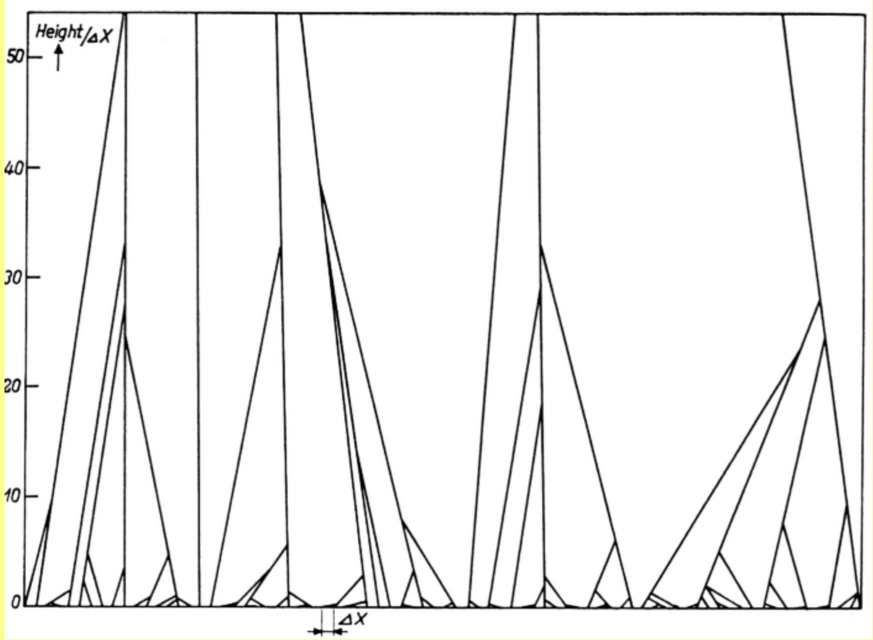
- RD42 leads the way..
  - Working with Element Six to improve properties
  - Polycrystalline silicon characterized in terms of ‘collection distance’ (measure of charge lifetime/trapping)
  - 5″ wafers possible



Thanks to: Alexander Oh

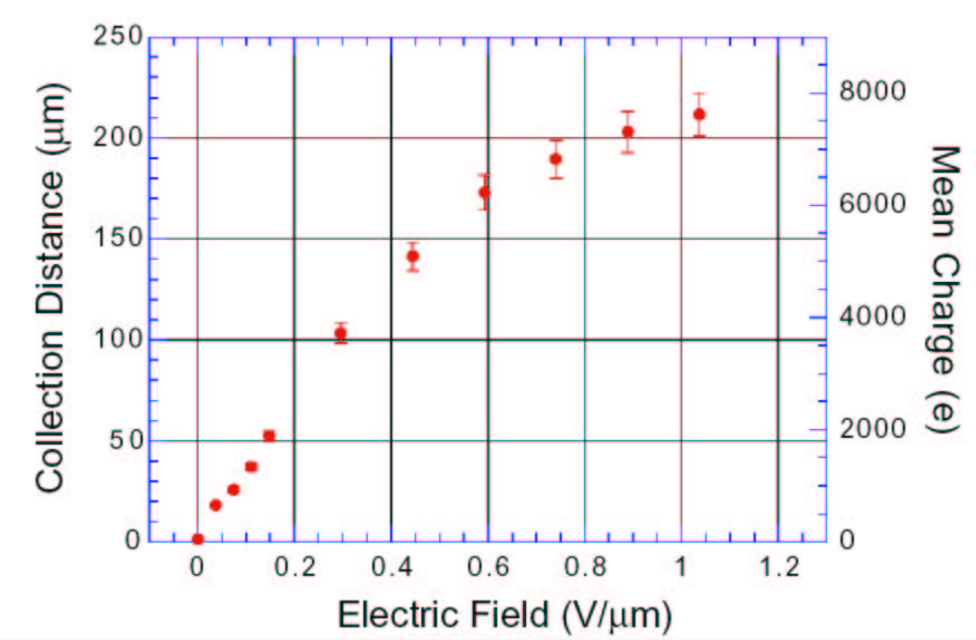
Diamond properties

- Polycrystalline diamond
  - Produced by CVD
  - Bandgap 5.47
  - Ionization energy 13eV
    - Smaller signal
    - Better radiation performance
    - Low leakage current
  - High mobility
  - Charge collection< 100%
- MIP signal 1.9 smaller than Si for same X_0



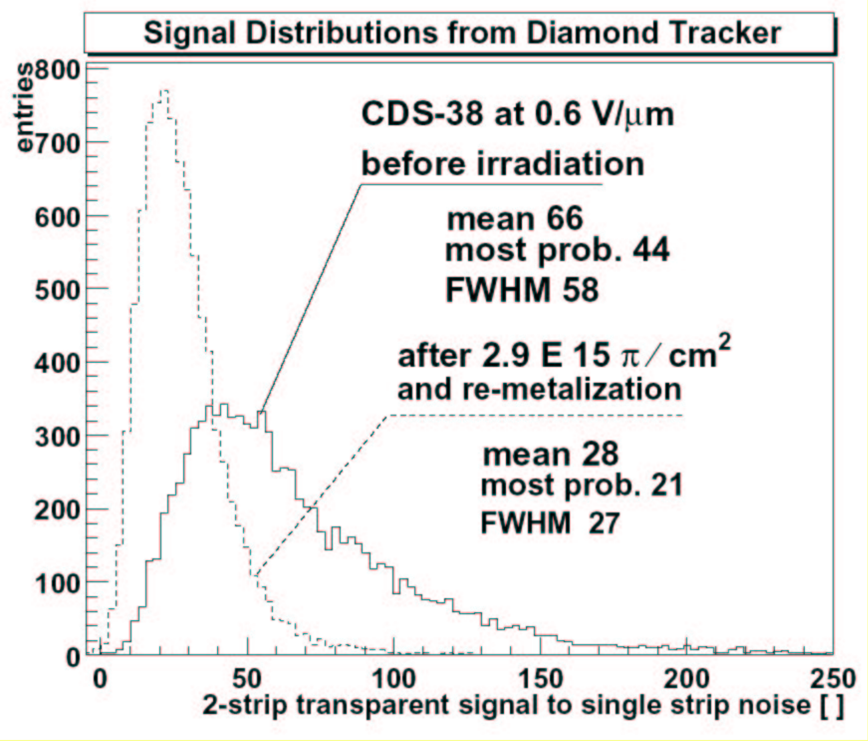
Diamond properties

- Sensitive to metallization process
  - E.g Cr/Au, Ti/Au, Ti/W…
- For full collection need ~1V/μm
  - Polycrystalline structure still influences resolution (lateral field)



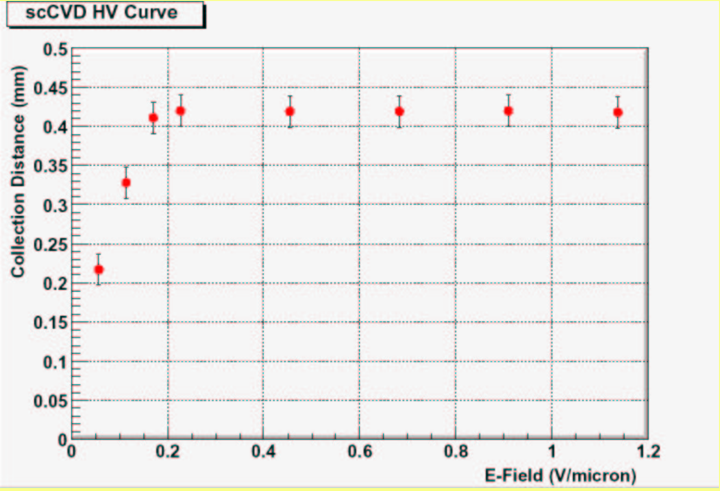
Diamond: radiation hardness

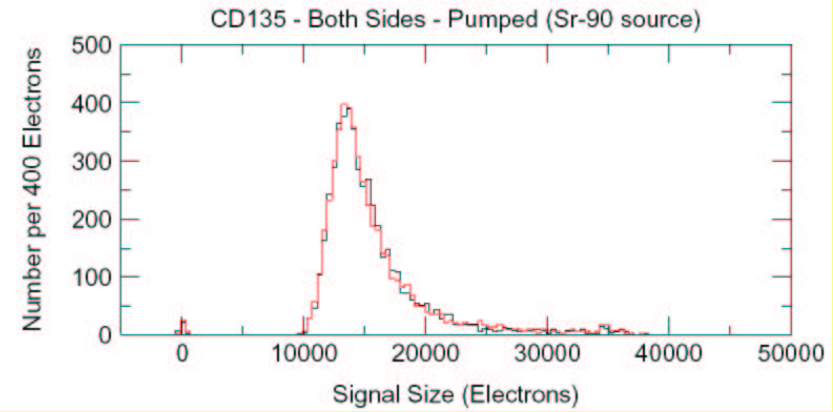
- Studied with various particles
  - More rad-hard to charged hadrons than neutrons
    - Survives 2.9×10^{15} /cm^2 pions
    - This gives 50% of charge



New: monocrystalline diamond

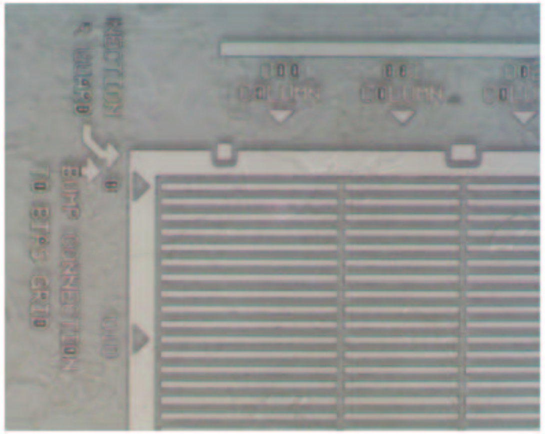
- Less defects
  - No grain boundary problem
  - Collection saturates at 0.2V/μm
  - 100% efficient



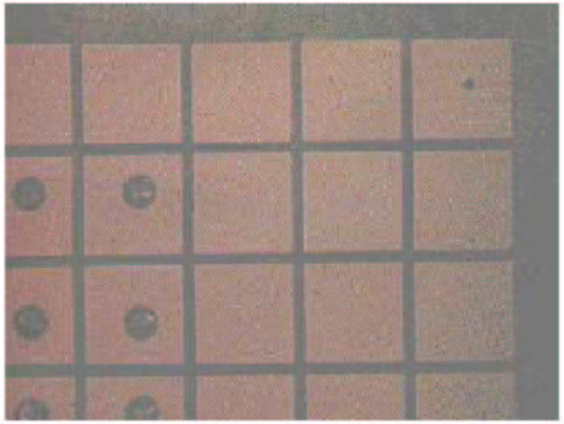


Diamond: pixel detectors

ATLAS FE/I Pixels (Al)



CMS Pixels (Ti-W)



- Atlas pixel pitch 50μm × 400μm
- Over Metalisation: Al
- Lead-tin solder bumping at IZM in Berlin

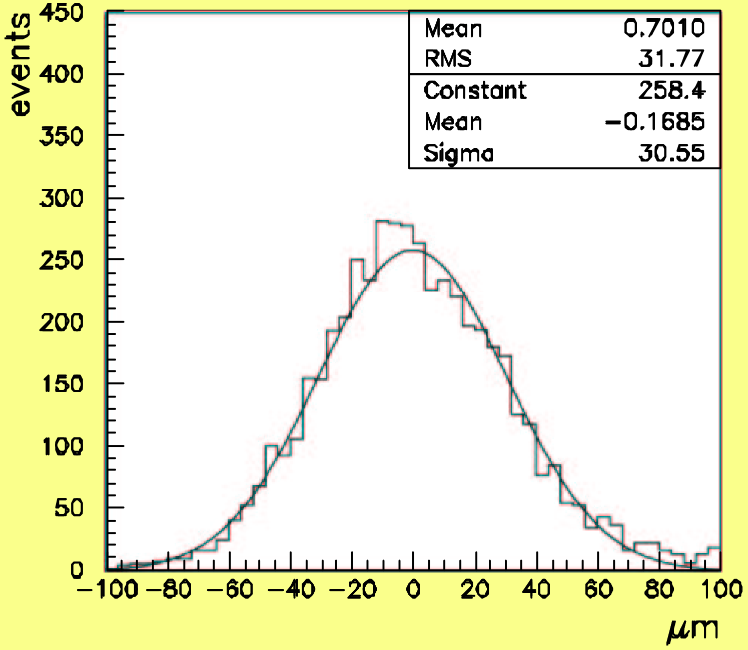
- CMS pixel pitch 125μm × 125μm
- Metalization: Ti/W
- Indium bumping at UC Davis

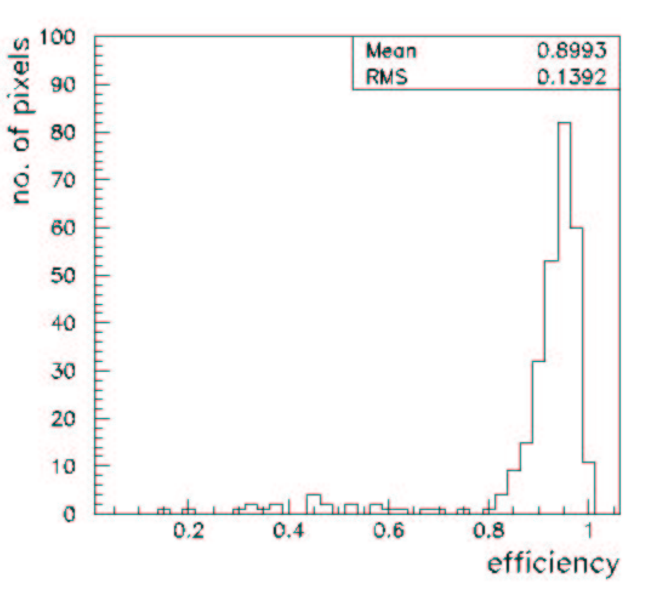
→ Bump bonding yield ≈ 100 % for both ATLAS and CMS devices

New radiation hard chips produced this year.

polycrystalline

Diamond detectors





- CMS results: 31μm resolution, 90% efficiency

Silicon Carbide

- Great promise
  - Greater displacement energy, should be radiation hard
  - More charge than diamond, less than silicon

Property	**Diamond**	**4H SiC**	**Si**
E_g [eV]	**5.5**	**3.3**	**1.12**
$E_{breakdown}$ [V/cm]	10^7	$4 \cdot 10^6$	$3 \cdot 10^5$
μ_e [cm^2/Vs]	1800	800	1450
μ_h [cm^2/Vs]	1200	115	450
v_{sat} [cm/s]	$2.2 \cdot 10^7$	$2 \cdot 10^7$	$0.8 \cdot 10^7$
Z	6	14/6	14
ε_r	5.7	9.7	11.9
e-h energy [eV]	**13**	**8.4**	**3.6**
τ_h [s]	10^{-9}	$5 \cdot 10^{-7}$	$2.5 \cdot 10^{-3}$
Wigner En.[eV]	**43**	**25**	**13-20**

Thanks to: Camilla Ronnqvist,
Michael Moll

Silicon Carbide

- Technology still immature
  - Defects seen in growth include step bunching, carrots and micropipes
  - Pipes may be mobile
  - Epitaxial is better, but expensive

QuickTime™ and a TIFF (LZW) decompressor are needed to see this picture.

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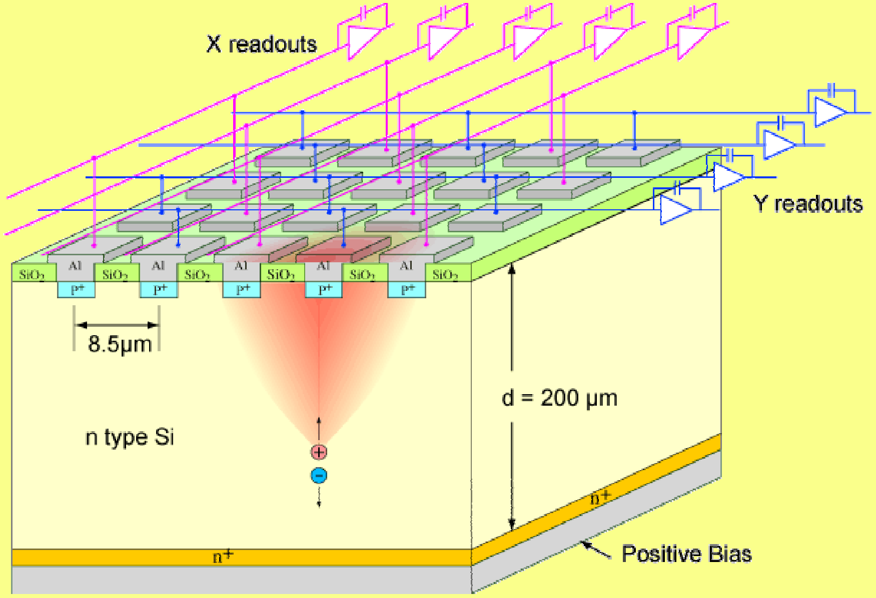
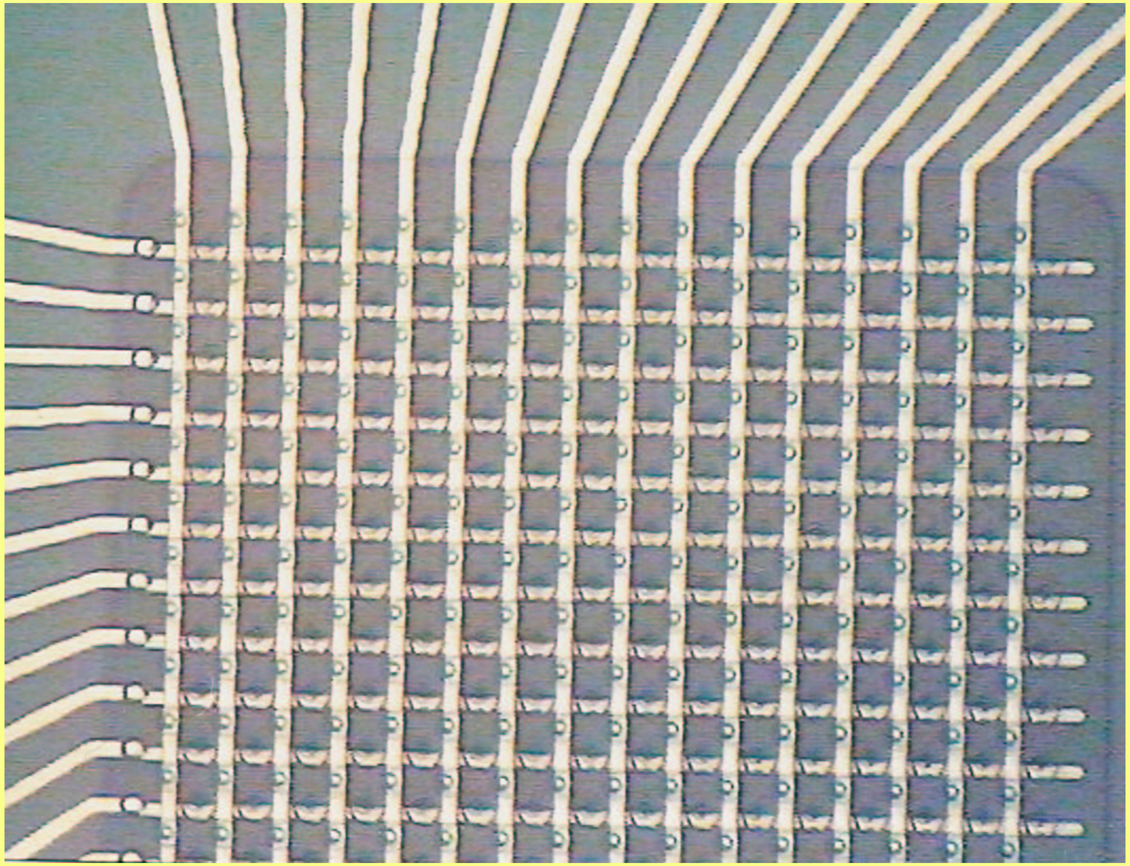
ASD

- Alternating stripixel detectors
  - Pixels are alternately connected to X/Y readout
  - Charge sharing allows the X/Y position to be determined
  - Small pitch allows interpolation to get <1μm resolution



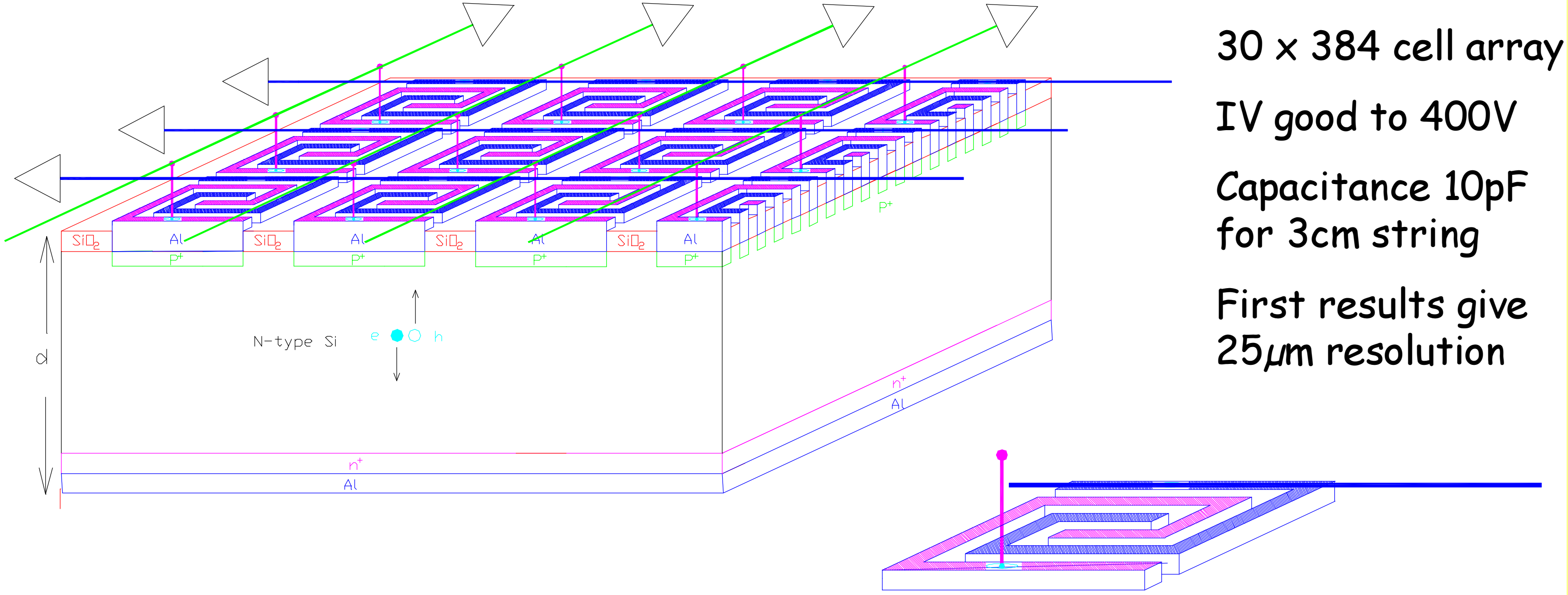
Thanks to: V.Radeka, Z. Li

ASD



- XY readout with single-sided processing
  - Double metal process
  - 8.5μm pitch
  - 2μm lines
  - 4 x 4 mm chip

Interleaved stripixel detector



Cells 1000 x 80 μm

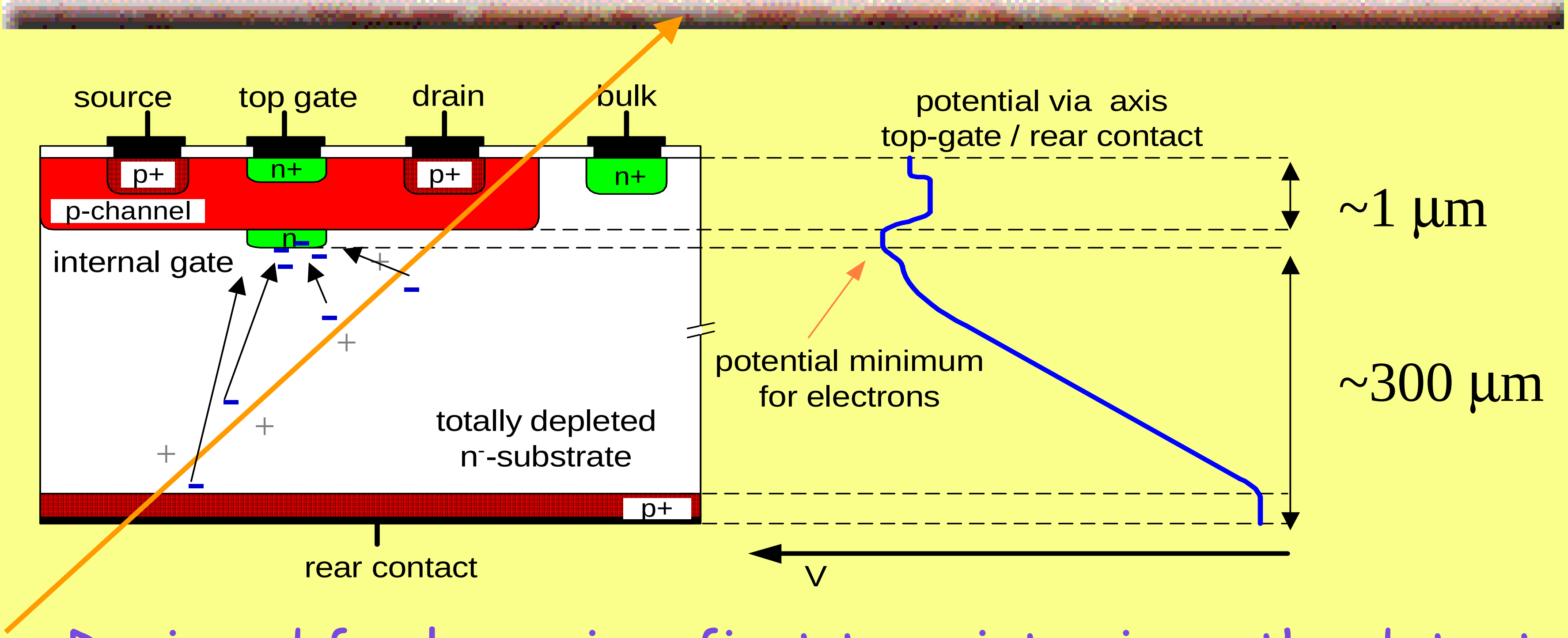
30 x 384 cell array

IV good to 400V

Capacitance 10pF for 3cm string

First results give 25μm resolution

DEPFET

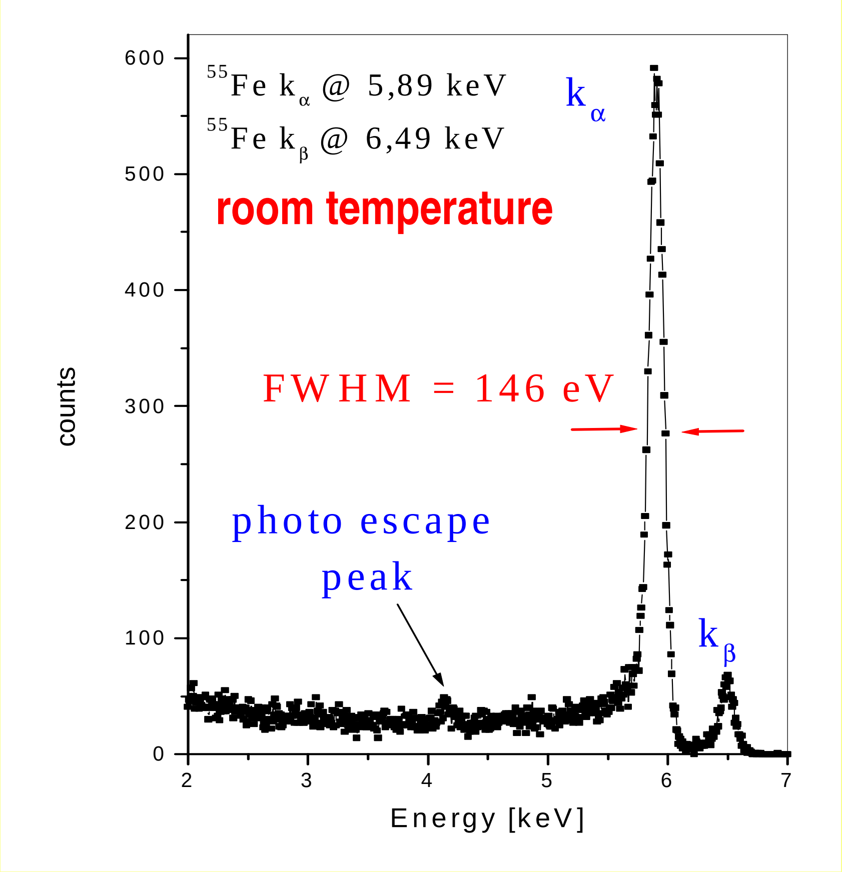


Designed for low noise; first transistor is on the detector
Substrate is sideways depleted (cf. drift detectors)

J. Kemmer und G. Lutz, NIM A253 (1987) 365

Thanks to: Norbert Wermes

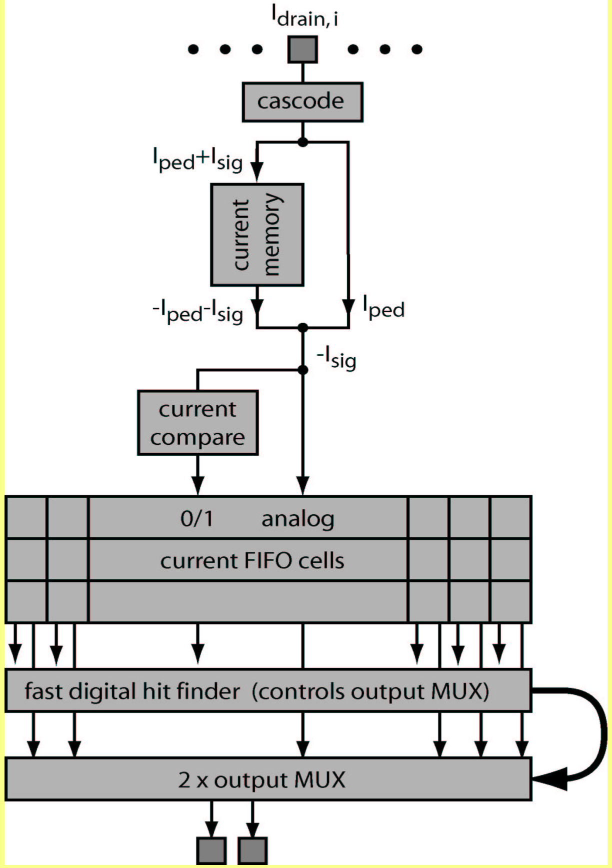
DEPFET resolution



- Noise of single pixel (50μm x 50μm) measured as 4.9 e- at room temperature.
  - Peak resolution limited by Fano factor
  - Matrices made with 69 e- noise at 35 C

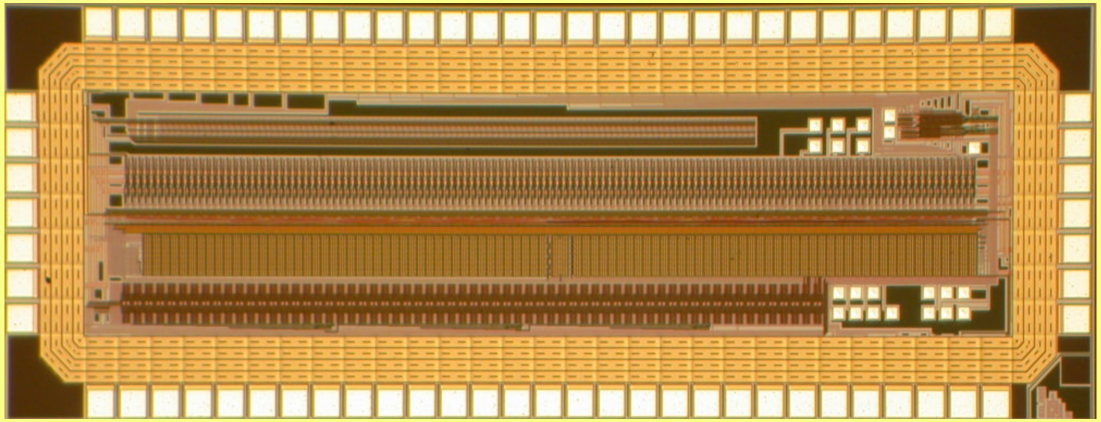
DEPFET: possibilities

- Was proposed for TESLA
  - Signal & pedestal in fast memory cell (20ns)
  - Hit decision with fast comparator
  - Decision and analogue value stored in FIFO
  - Fast digital scanner finds and reads hits; empty FIFO cells are skipped.



Marcel Trimpl, Peter Fischer

Future DEPFET



- Testchip 1.5 x 4 mm contains all basic blocks
  - Designed in rad tolerant 0.25μmTSMC
  - Works roughly as advertised

Summary

- Material and geometrical solutions are not exclusive
  - E.g. cold 3d
- Diamond looks mature enough for hybrid pixel detector
- Silicon has a habit of keeping up
- R&D on trapping still rather primitive
- Power will be an increasing problem
- New solutions are still costly, may remain so?