Highlights from the VTX session

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+
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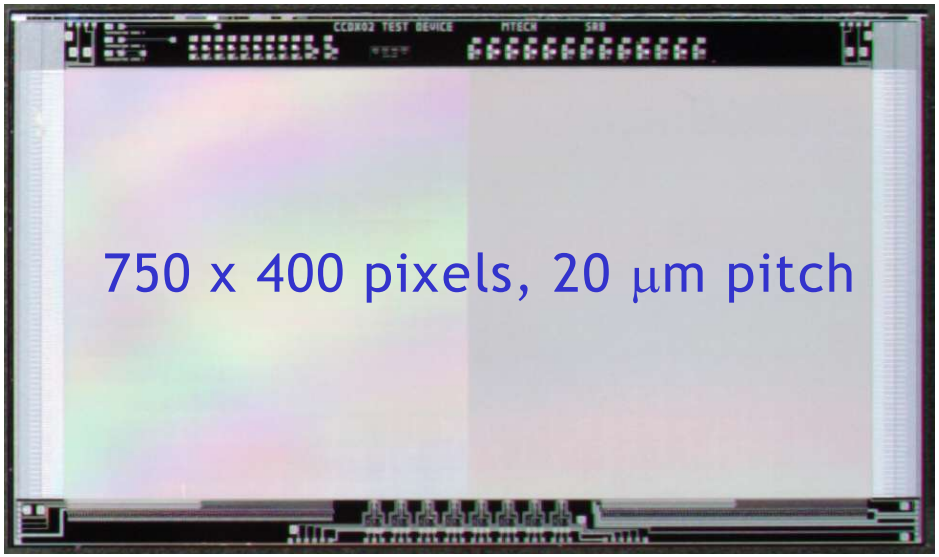
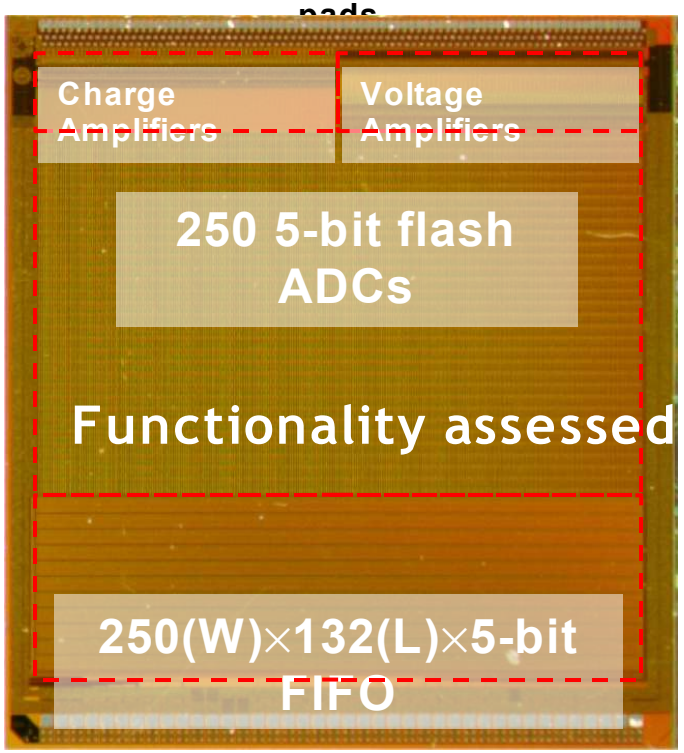
- R&D reports; four technologies:
  - CCD
  - CMOS
  - DEPFET
  - SOI
- physics studies:
  - impact parameter as a geometry & material figure of merit
  - stop production & Higgs BR as physics benchmarks

CCD highlights

First Column Parallel readout architecture + read out chip up & runnin



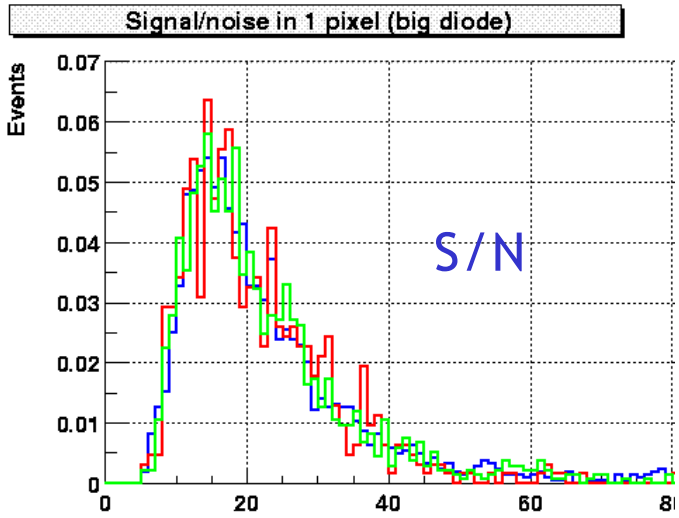


- clocked @10 MHz (TESLA specs: 50 MHz)
- clock amplitude ~ 2 V (spec: < 3 V)
- noise: 60 e- (signal > 1000 e-/pixel)
- response to ^{55}Fe 5.9 keV X-rays observed

Integration & test foreseen on a short time scale

CMOS hot news

Uniformity of real scale sensors

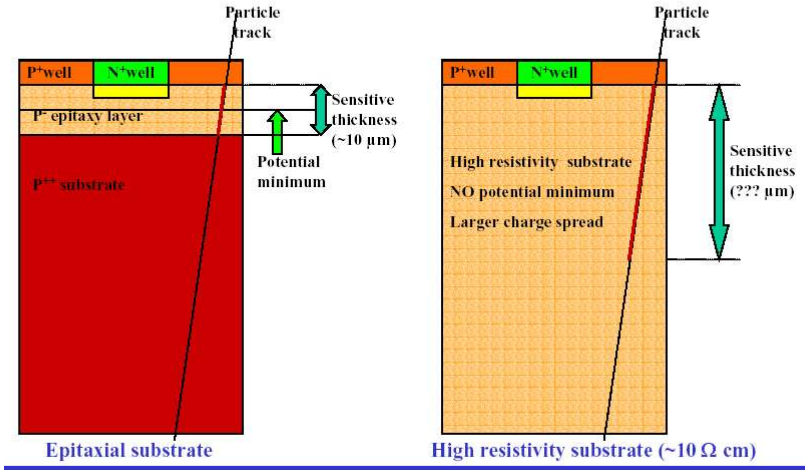


- 19.4 x 17.4 mm^2, ~ 1 Mpixels, 120 μm thick
- efficiency ~ 99%; σ ~ 2.5 μm
- baseline for the **STAR** VD upgrade (2006);

important items for the LC applications:

- 100 MHz clock; 0.25 μm technology
- large system integration & test in a real experimental conditions

No-epitaxial layer techn. assesse

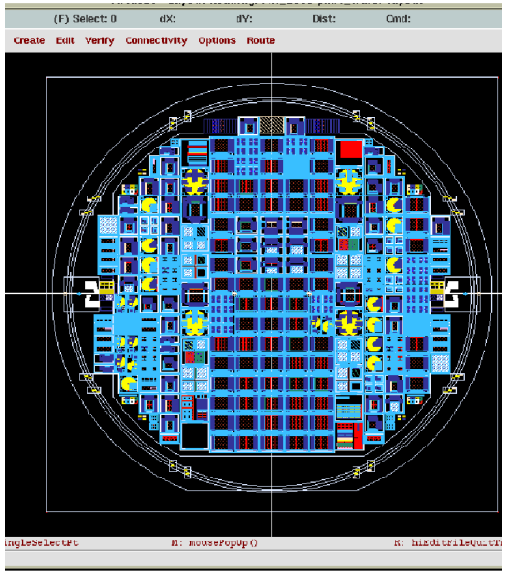


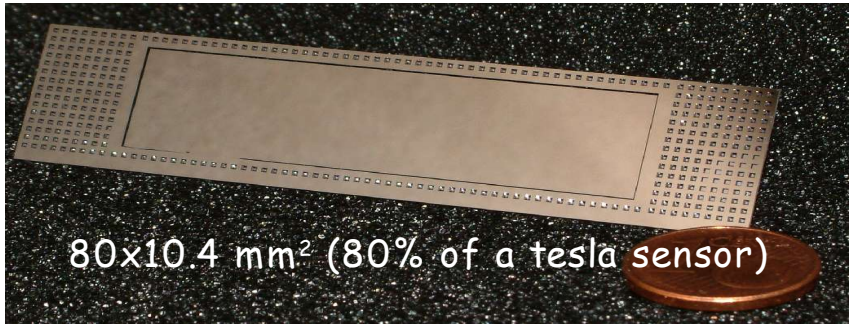
- two ≠ prototypes tested (20 & 40 μm pitch)
- S/N > 20 @ 10 °C
- efficiency > 99.5%; σ ~ 2.5 μm
- radiation tolerant at 200 krad & 10^{11} n/cm^2

First test on 15 μm backthinned chips expected in November

DEPFET advances

First prototypes for charged particles produced & dummies backthinn





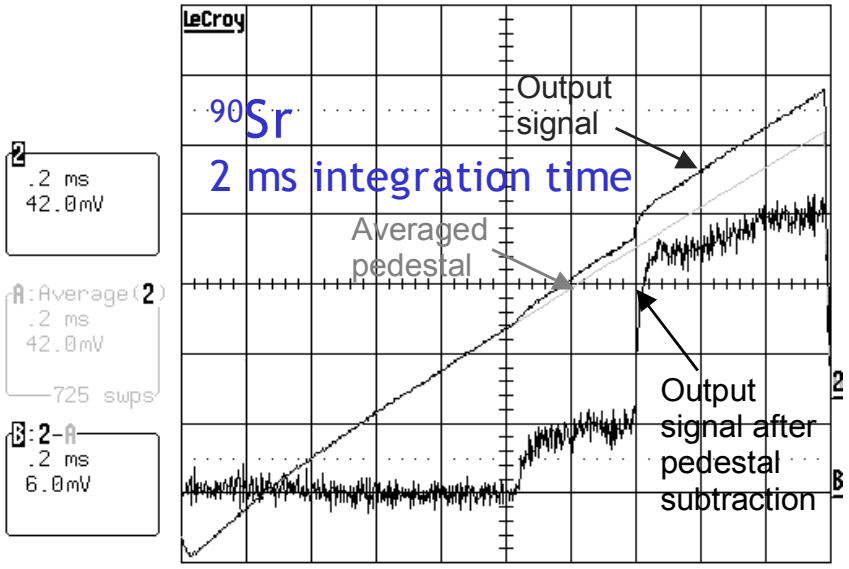
- Circular and linear DEPFETS
  up to 64 x 128 pixels
  minimum pixel size about 25 x 25 μm²
- technology assessed
- Line control chip ready (switcher)
- Readout Chip back from the foundry soon

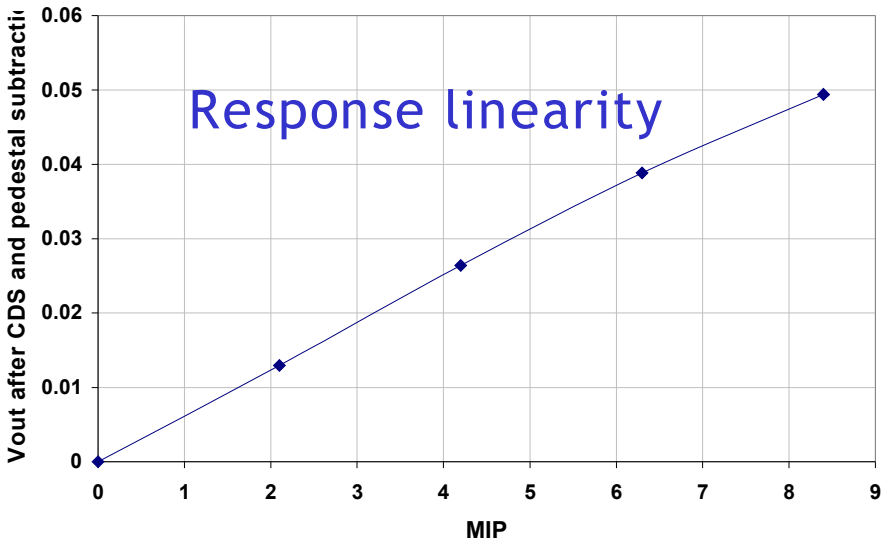
- dedicated thinning technology assessed
- 50 μm thickness + reinforcing rims
- Handling of etched wafers and diced thin chips is safe and easy

Full chain integration & Large pixel array production in 2004

SOI hot news

First prototype on high-resistivity substrate produced!
Sensitivity to m.i.p. assessed





- SOI on high resistivity FULLY DEPLETED substrate; nmos + pmos in the front e
- 8 x 8 pixel matrix; pitch: 140 x 122 μm
- simple front-end architecture inherited from the 3-T CMOS imager
- dynamic range up to 300 m.i.p./pixel

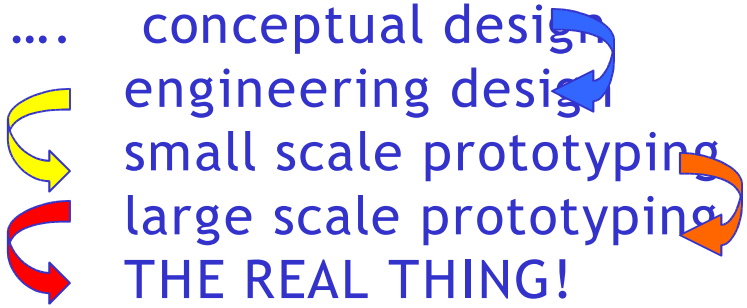
Processing of an imaging ladder 72 x 24 mm², 160 μm pitch planned for 2004

Physics benchmarks

Goals: estimate the effect of

- material budget
- layer geometry & alignment
- pixel pitch
- readout characteristics

as time goes by ….



Tools:

- basic impact parameter analysis
- performance of tagging algorithms
- selected “VD sensitive” channels ⇔ interaction with the physics teams