Status of the CALICE ECAL

CALICE collaboration


• Introduction
• The proposed calorimeter
• The ECAL prototype
• R&D for next generation
• Schedule

• Silicon wafer
• PCB
• VFE Chip
• Gluing
• DAQ
• First measurements

• New chip
• Thermal studies
• AC coupling (silicon)
• PCB
It is not R&D in the back yard!!
Start from physics
See what design/technique could fit
List the R&D to do to validate the choice
Study potential performance with simul.

Optimise EFLOW performances lead to optimize close showers separability so, like digital camera

\[\textbf{\textit{number of pixel !!!}}\]
Ultra granular/segmented – stable – compact
example ECAL, a sampling tungsten – silicon
example HCAL, a sampling Fe – RPC’s, gem, scint. tiles

Well adapted for the physics programme at TeV LC
i.e. to fully reconstruct multi-jets events
to have a good channel id. in the $\tau$ decays

Perspective view of the ECAL

$e^+e^- \rightarrow ZH, \ Z \rightarrow \mu\mu$ at $\sqrt{s}=500$ GeV

GEOMETRY*: No way to escape

[*] The calorimeter 8-fold way of Henri Videau
- No large dead zone
- All modules are identical
- Detector slab tested before mounting

Based on mechanical study,

The full scale detector can be realised with the same pattern:

“Tungsten wrapped in CFi”
The ECAL prototype

Note the density

Structure 1

Structure 2

Structure 3

Metal inserts (interface)

Detector slab

ACTIVE ZONE (18×18 cm²)

360 mm

200 mm

360 mm

Silicon wafers with 6×6 pads (10×10 mm²)

3 structures W-CFi (1,2,3 x1.4 mm)

15 « detector slabs »

Dimension 200x360x360 mm

9720 channels in the proto.
Prototypes for the test beam

Simulation GEANT4

10 GeV pion
Detector slab

- Shielding
- Tungsten
- Carbon Fiber
- Silicon wafer
- Front End electronics zone
- PCB
- SCSI connector
- Carbone Fiber
- tungsten
- 8.5 mm
## Silicon Wafers for the prototype

<table>
<thead>
<tr>
<th>Parameter</th>
<th>Details</th>
</tr>
</thead>
<tbody>
<tr>
<td>4” High resistive wafer</td>
<td>5 kΩ/cm</td>
</tr>
<tr>
<td>Thickness</td>
<td>525 microns ± 3 %</td>
</tr>
<tr>
<td>Tile side</td>
<td>62.0 + 0.0 - 0.1 mm</td>
</tr>
<tr>
<td>Guard ring</td>
<td></td>
</tr>
<tr>
<td>In Silicone ~80 e-h pairs / micron</td>
<td>42000 e−/MIP</td>
</tr>
<tr>
<td>Capacitance</td>
<td>~21 pF</td>
</tr>
<tr>
<td>Leakage current</td>
<td>5 – 15 nA</td>
</tr>
<tr>
<td>Full depletion bias</td>
<td>~150 V</td>
</tr>
<tr>
<td>Nominal operating bias</td>
<td>200 V</td>
</tr>
</tbody>
</table>

One wafer is a Matrix of 6 x 6 pixel of 1 cm².

**Important point:** manufacturing must be as simple as possible to be near of what could be the real production for full scale detector in order to:

- Keep lower price (a minimum of step during processing)
- Low rate of rejected processed wafer
- Good reliability and large robustness
Silicon Wafers for the prototype

Number of active Wafer needed for the physic prototype: **270**.

- **150** produce by Institute of Nuclear Physics - Moscow State University (M. Merkin, A. Savin, A. Voronin)
  - First test production: February 2003
  - Today: **~130 matrices**

- **150** produce by Institute of Physics, Academy of Sciences of the Czech Republic – Prague (V. Vrba)
  - *First test production: March 2004* (6 good wafers)
  - Full prod for end of May.
Silicon Wafers for the prototype

Institute of Nuclear Physics
Moscow State University

Capacitance: ~25 pF
Leakage current: 1 – 5 nA
Full depletion bias: ~110 V
Nominal operating bias: 200 V

Institute of Physics, Academy of Sciences of the Czech Republic

One process gives results which fit the spec.
PCB for the prototype

Class 6 PCB
design in LAL-Orsay
made in Korea (KNU)

NO WAFER
(MONEY !!!)

Prototype: 60 PCB → middle of July
**FLC-PHY3**

**Chip VFE**

- Processed channels: 18 (two possible gains)
- Noise: ENC = 3300 + 30 e⁻ μF
- Linearity: ± 0.2 %
- Dynamic: 600 MIPS @ Cf = 1.6 μF

**VFE electronics**

- Overall noise, including DAQ, is around 700 μV (0.14 MIP) ➔ S/B ~ 7σ
- The talk by Julien Fleury (LAL)
Mounting/Gluing the wafers

A automatic device is use to deposit the conductive glue:
EPO-TEK® EE129-4

Gluing and placement (± 0.1 mm) of 270 wafers with 6×6 pads
About 10 000 points of glue.

Using a frame of tungsten wires

X-Y-Z table (400×400×150 mm³) with glue dispensing tool (conductive glue)
Full Prototype DAQ (FPD) based on VME 9U board developed for CMS, modified by UK groups. No zero suppress, 96 VFE/board, 16 bits ADC's, 20 Kbytes/s possible for Test Beam. First test on April 2004 validate the full chain from wafer to DAQ and “tape”.

The talk by Paul Dauncey (Imp. Coll. London)
**Single Slab DAQ (SSD)**

- for calibration and test on Cosmic Test bench
- work only for a single detector slab
  (24 VFE chips/ 432 silicon pad channels)
- based on NI board (on-shell)
First test with a complete detector slab
First test with a complete detector slab

Si wafer - glue - PCB - VFE – DAQ (Single Slab DAQ) and ground with Al. EMC shield

“internal” signal

1 MIP injected in channel 10 with CALIB chip and measurement made on 100 points

- Theoretic result : 4.97mV 
(C_f=1.35pF)
- Measured : 5.05mV

“external” signal

Sr^{90} source → trigger → read 6 channels

Only ONE with signal

\[
\frac{MIP}{\text{Noise}} \approx 7.5
\]

Wafer from Moscow State University
First test with a complete detector slab

Si wafer - glue - PCB - VFE – DAQ (Full proto DAQ)
and ground with Al. EMC shield

Strontium Peak - New Wafers

Sr\textsuperscript{90} source \(\rightarrow\) trigger \(\rightarrow\) read 1 channel

<table>
<thead>
<tr>
<th>Strontium Peak - New Wafers</th>
<th>hist_event</th>
</tr>
</thead>
<tbody>
<tr>
<td>Entries</td>
<td>2000</td>
</tr>
<tr>
<td>Mean</td>
<td>66.58</td>
</tr>
<tr>
<td>RMS</td>
<td>27.77</td>
</tr>
</tbody>
</table>

Wafer from Academy of Sciences/Prague
Cosmic test bench

Si wafer - glue - PCB - VFE - PCB – DAQ (Single Slab DAQ)
First test with/without cooling (top Al. plate) and VFE inside

**SAMCEF Simulation**
Thermal dissipation with internal cooling at the border with liquid flow

**R&D**

**Thermal contact**

AC coupling elements?

- **Capacitance Si₃N₄ 2µm**
- **Resistance aSi 2µm**
- **Diode contact Chrome 1550A**
- **R and C external contact Chrome 1550A**
- **Diode contact Chrome 1550A**

**R and C for AC coupling using thin film technique**

- **Capacitance Si₃N₄ 2µm**

**PCB**

- **Aluminium**
- **Cooling tube**
- **VFE chip**
- **Cooling tube**

**Silicon wafer**

- **Power line**
- **Command line**
- **Signal out**

**LLR**

**KNU**

**Thermal contact gluing for electrical contact**
Assembling and testing on a cosmic test bench

**Intercalibration of the 10K channels** and overall debug!

**~December 2004 at DESY** (Low energy electrons E<6 GeV)
First test beam

**2005-2006 at FNAL/IHEP/SLAC ?** (electrons/pions/protons up to ~80 GeV)
Test beam with HCAL ...

**R&D in ECAL-CALICE**

**2004-2007**
Study of the new geometry \(\uparrow\) with the impact of HE e.m. shower in the chip

- Optimisation of the interaction VFE-chip / cooling
- ADC-DAQ board with low consumption, small dimension, >100 channels/board

\(\uparrow\) VFE inside detector