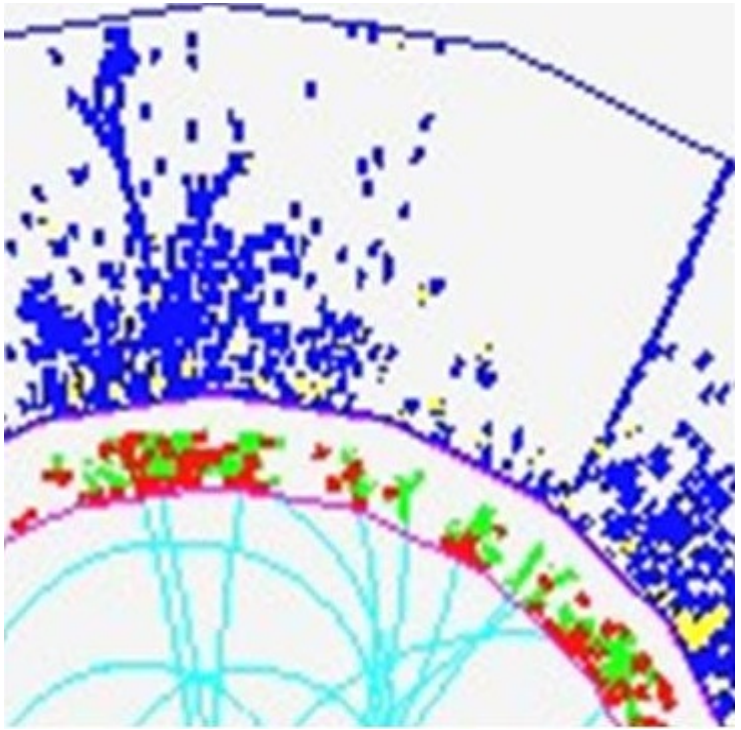
Silicon/Tungsten ECal for SiD – Status and Progress

Ray Frey
University of Oregon
ICLC Paris, April 22, 2004

- Overview (brief)
- Current R&D
  - detectors
  - electronics
  - timing
- Hybrid Status from K.U.
- Summary

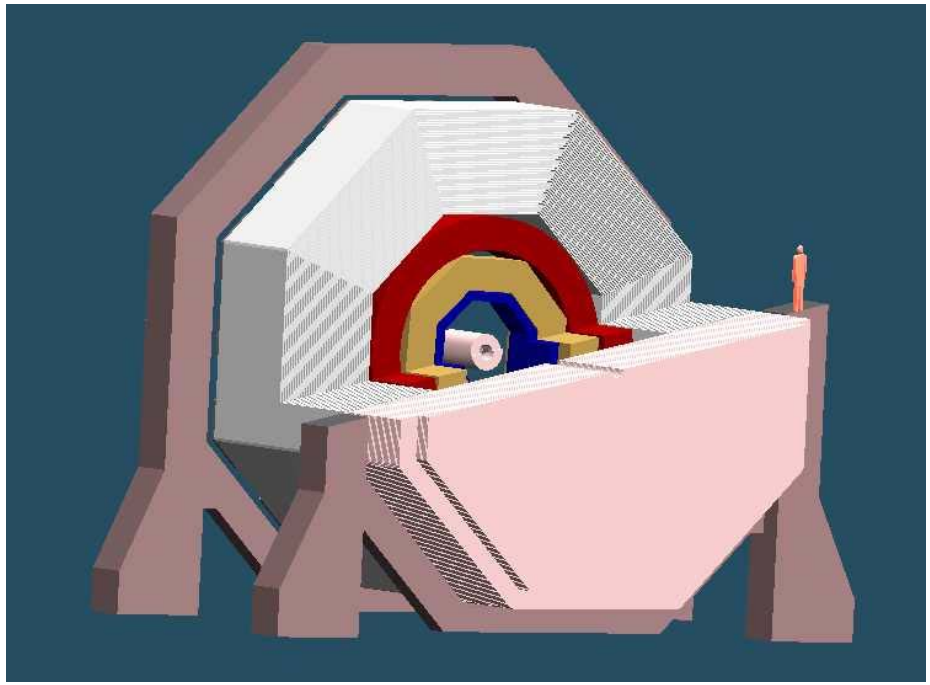


SD Si/W

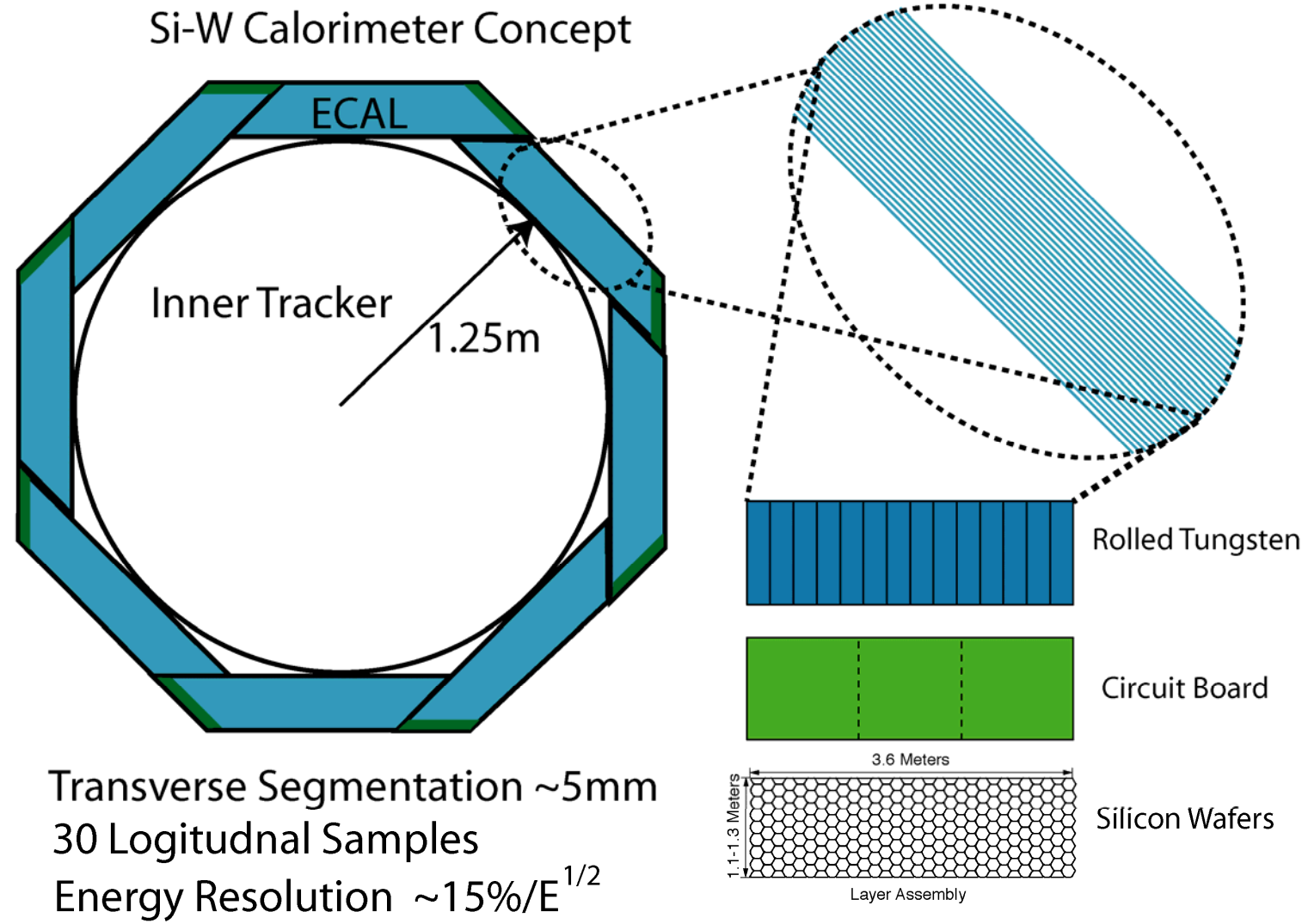
M. Breidenbach, D. Freytag, N. Graf,
G. Haller, O. Milgrome
Stanford Linear Accelerator Center

R. Frey, D. Strom
U. Oregon

V. Radeka
Brookhaven National Lab

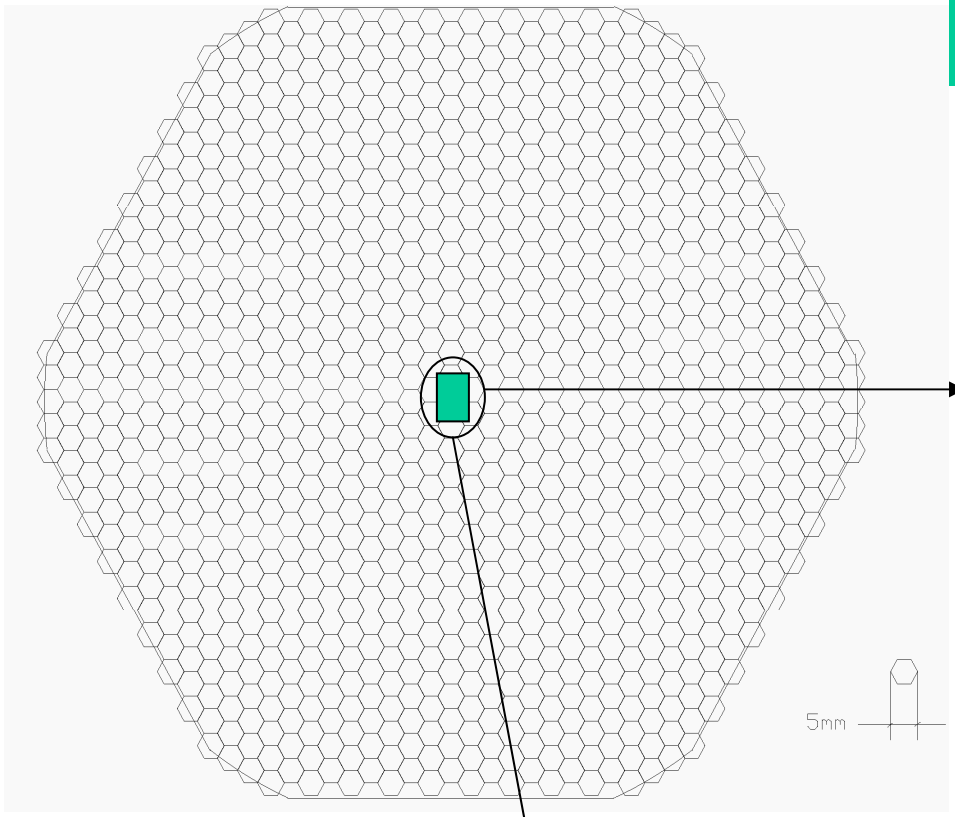


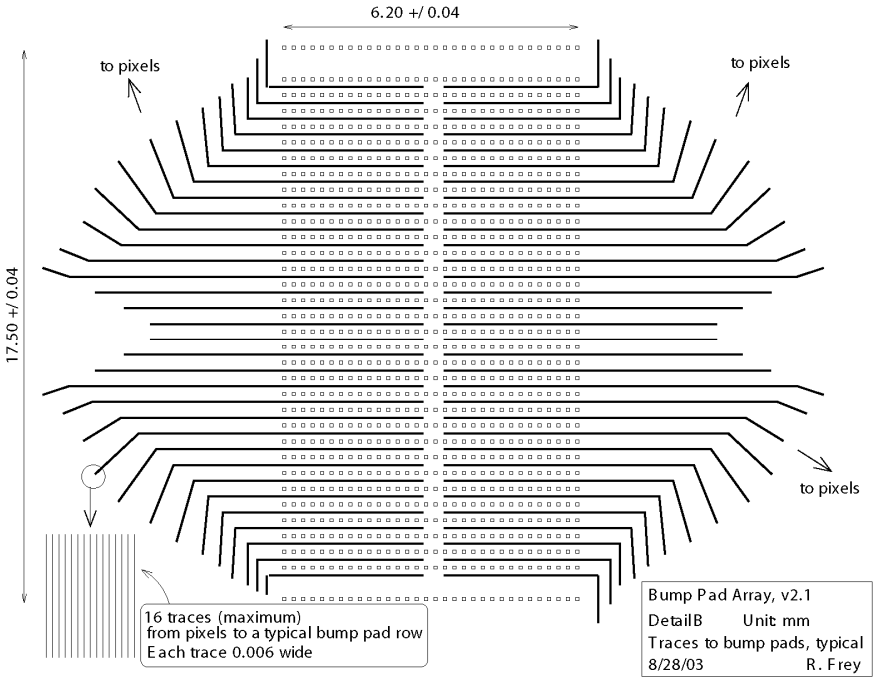
Concept

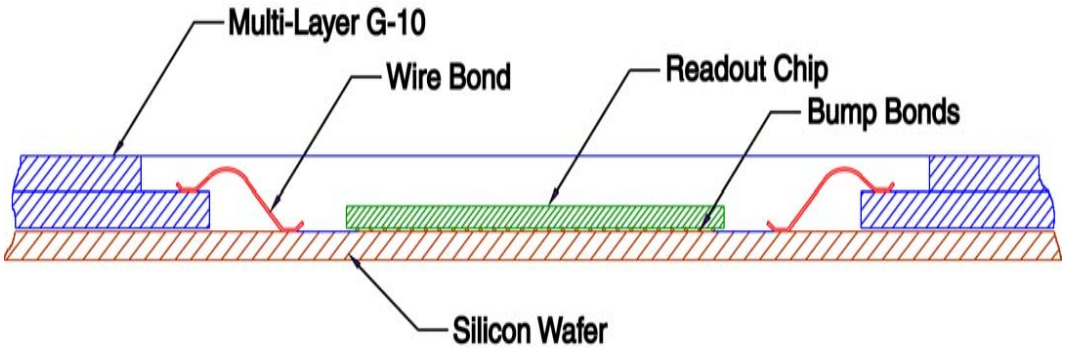


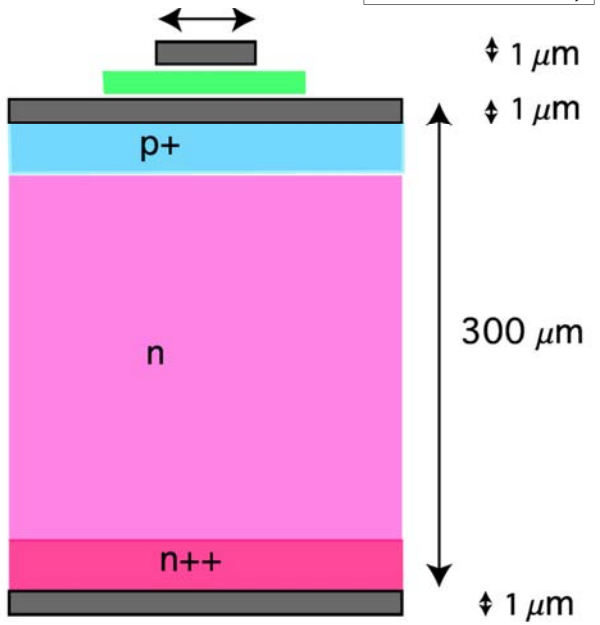
Transverse Segmentation ~5mm
30 Logitudnal Samples
Energy Resolution ~15%/$E^{1/2}$

Wafer and readout chip







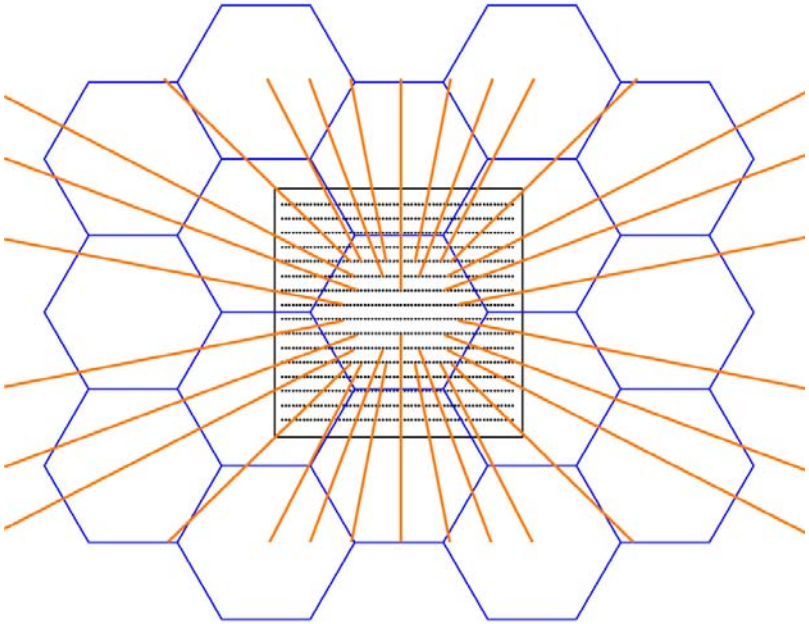


SiD Si/W Features

- "Channel count" reduced by factor of 10^3
- Compact – thin gap ~ 1mm
  - Moliere radius 9mm → 14 mm
- Cost nearly independent of transverse segmentation
- Power cycling – only passive cooling required
- Dynamic range OK
- Timing possible
  - Low capacitance
  - Good S/N
  - Correct for charge slewing/outliers

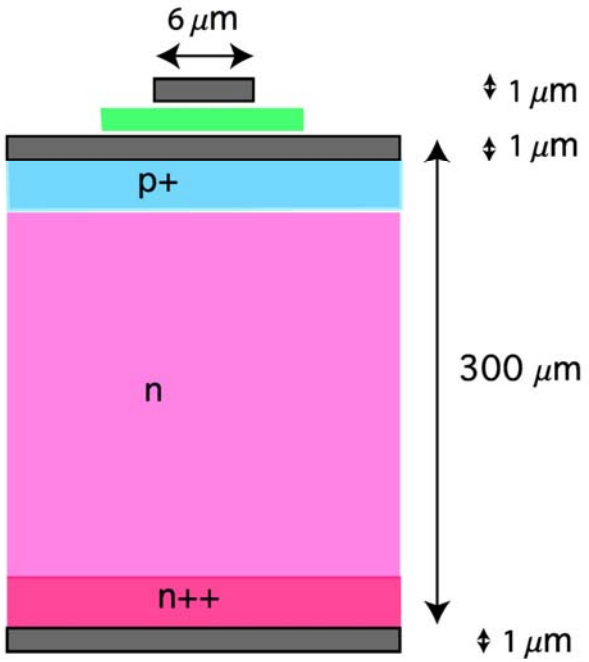
Current configuration:

- 5 mm pixels
- 30 layers:
  - 20 x 5/7 X0 +
  - 10 x 10/7 X0



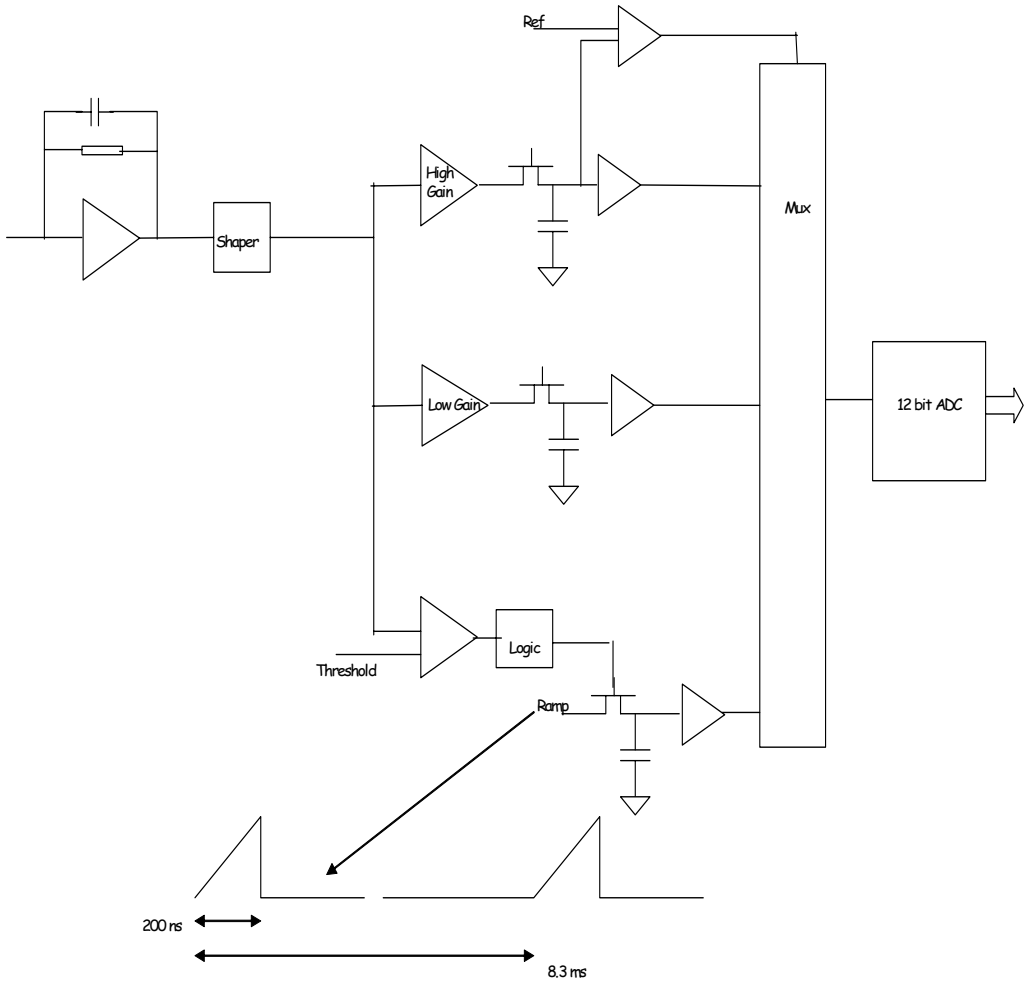
Electronics requirements

- Signals
  - <2000 e noise
  - Require MIPs with S/N > 7
  - Max. signal 2500 MIPs (5mm pixels)
- Capacitance
  - Pixels: 5.7 pF
  - Traces: ~0.8 pF per pixel crossing
  - Crosstalk: 0.8 pF/Gain x Cin < 1%
- Resistance
  - 300 ohm max
- Power
  - < 40 mW/wafer ⇒ power cycling
    (An important LC feature!)
- Provide fully digitized, zero suppressed outputs of charge and time on one ASIC for every wafer.



Electronics scheme – old (~1 year ago)

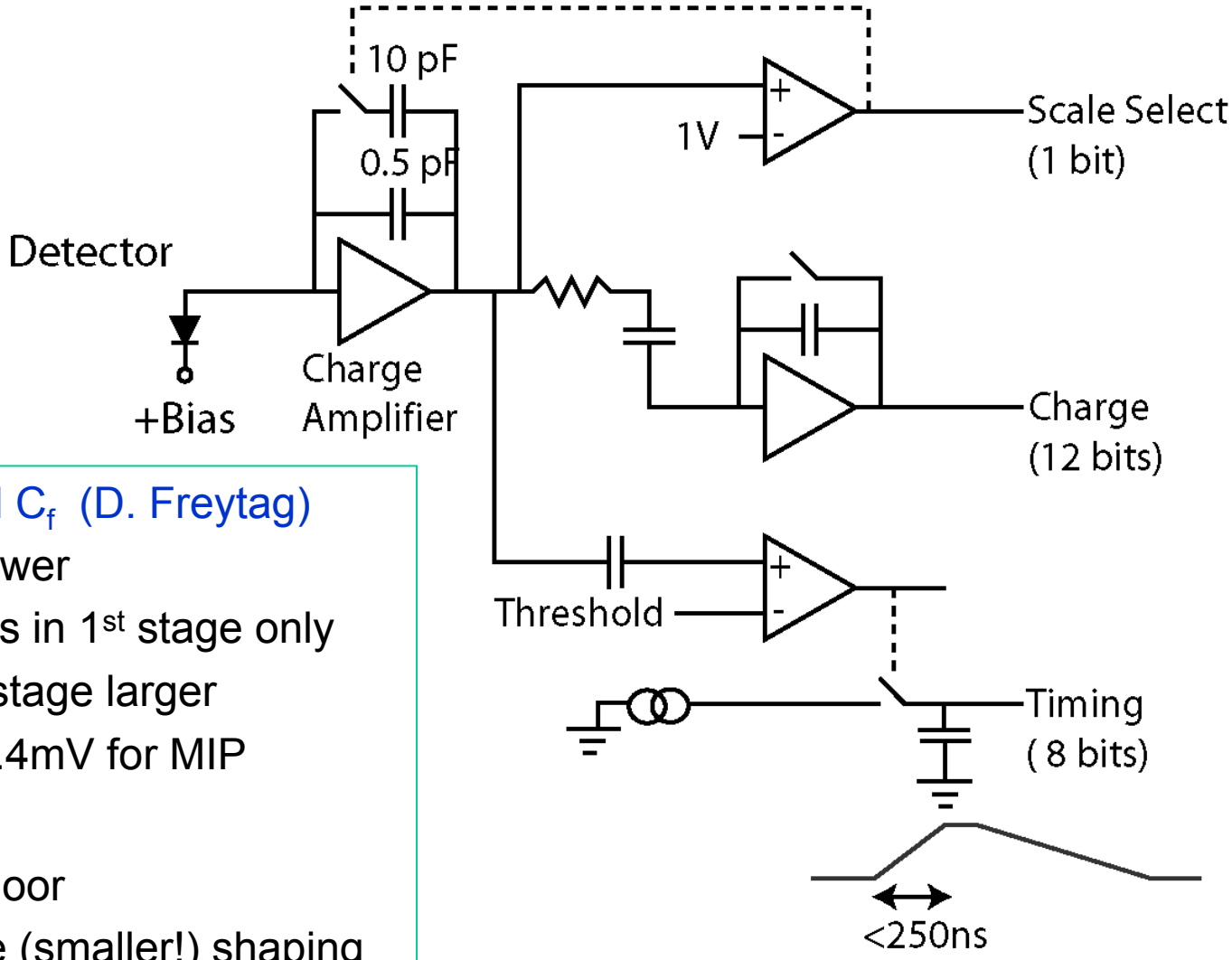
- Dynamic range
  - 0.1 to 2500 MIPs
  - Requires large Cf = 10 pF on input amplifier
  - Two ranges
  - Requires large currents in next stages
  - Requires small signals for ~MIPs after 1st stage
- Time
  - Pile-up background
  - Exotic physics
  - In this version, expect 10-20 ns



Electronics design – Present

Single-channel block diagram

Note: Common ~50 MHz clock



- Dynamically switched C_f (D. Freytag)
  - Much reduced power
    - Large currents in 1st stage only
  - Signals after 1st stage larger
    - ~0.1 mV → 6.4mV for MIP
- Time
  - No 4000e noise floor
  - Can use separate (smaller!) shaping time (~40 ns)
  - Readout zero-crossing discharge (time expansion)

Electronics design (contd)

- Present design gives:

  Noise = 20-30 e/pF

- C_{in} = pixel + traces + amplifier

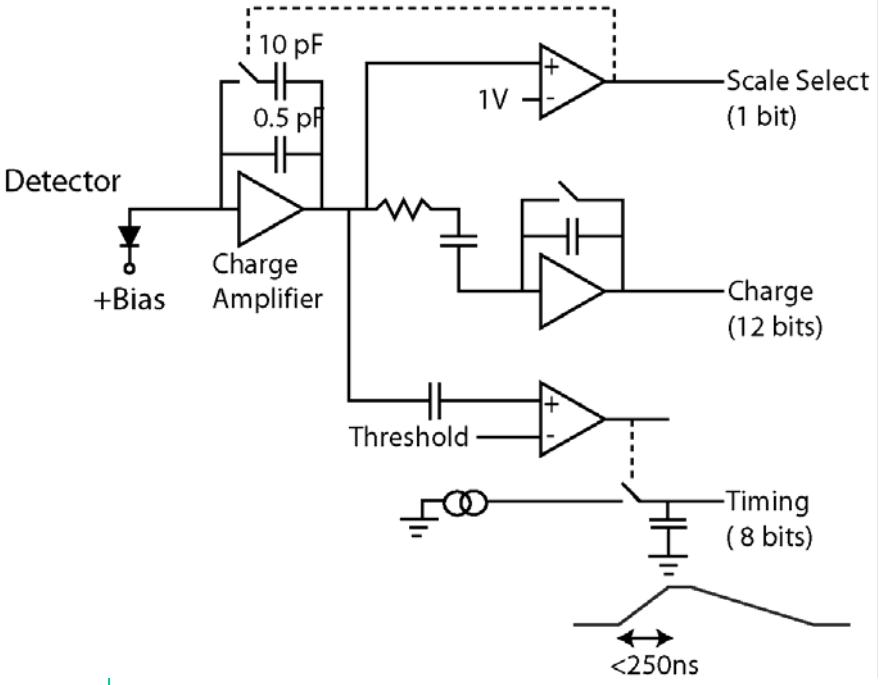
  5.7pF + 12pF + 10pF ≈ 30 pF

⇒ Noise ≈ 1000 e (MIP is 24000 e)

- Timing: ~ 5 ns per MIP per hit
  - D. Strom MC (next)
  - Simulation by D. Freytag
  - Check with V. Radeka:

    "Effective shaping time is 40ns;

    so σ ≈ 40/(S/N) ≈ 5 ns or better."



Timing MC

D. Strom, Calor2004

Toy Monte Carlo Studies of Timing Resolution for 30 Samples

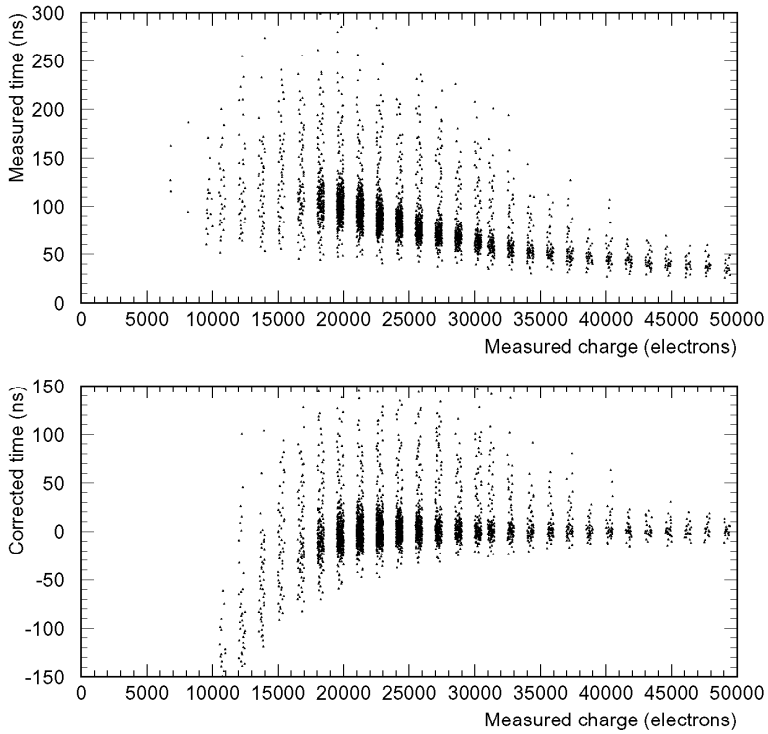
Assumptions – wild guesses – (waiting for real electronics model):

- Each MIP has 30 samples at random distances from the read-out chip
- Threshold for timing measurement is 8,000 electrons.
- Input FET has g_m = 1.5mS and the noise contribution from the rest of the amplifier is equal to input FET except for the "floor" noise.
- The charge measurement has a noise floor of either 0 or 4000 electrons
- Time constant for charge measurement is 200 ns.
- Time constant for the time measurement is 50 or 200 ns.
- The noise signals in the timing and charge circuits are uncorrelated
- Random 5% channel to channel variation in threshold
- Random 1% event-to-event variation in threshold
- Random 5% uncertainty in constants used for correction.
- Reject time measurements far from mean

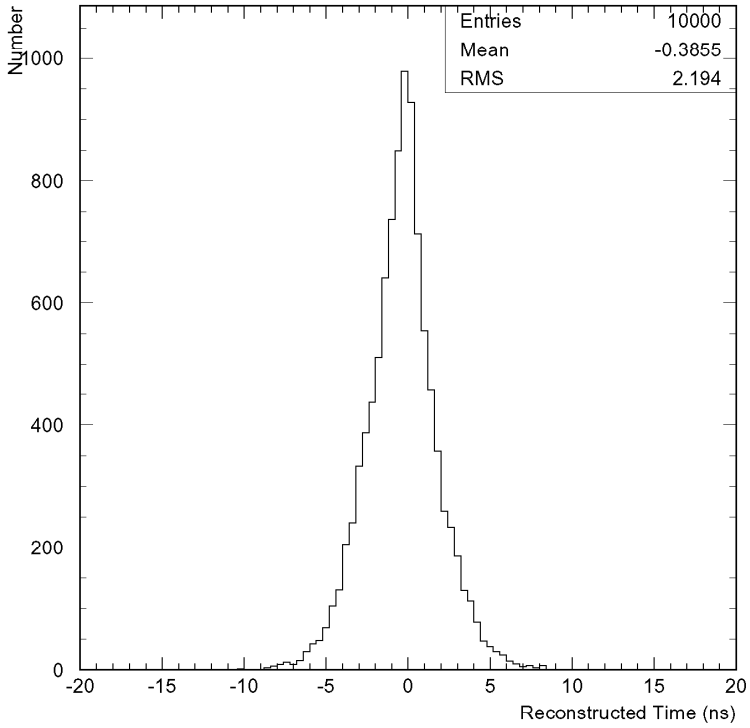
Timing MC (contd)

Sample Timing Results

200 ns time constant, no noise floor



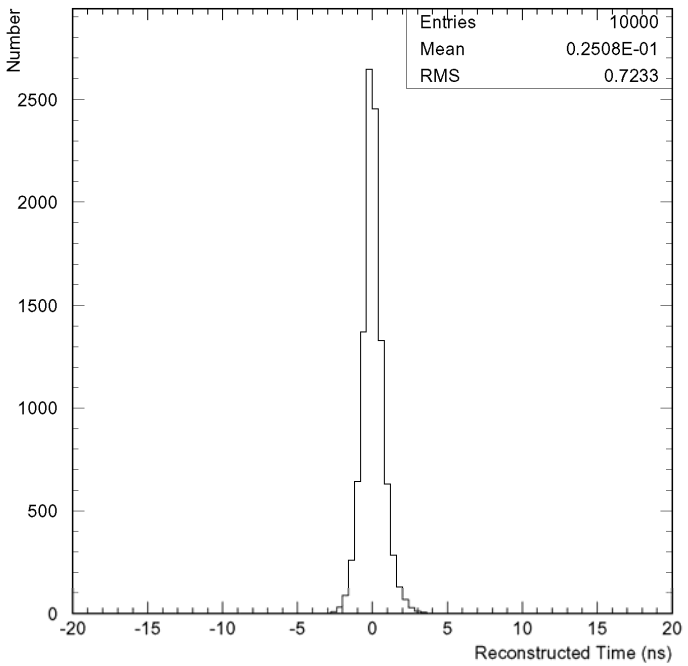
Time versus charge for mips



30 sample average time

Timing MC (contd)

50 ns time constant and
30-sample average



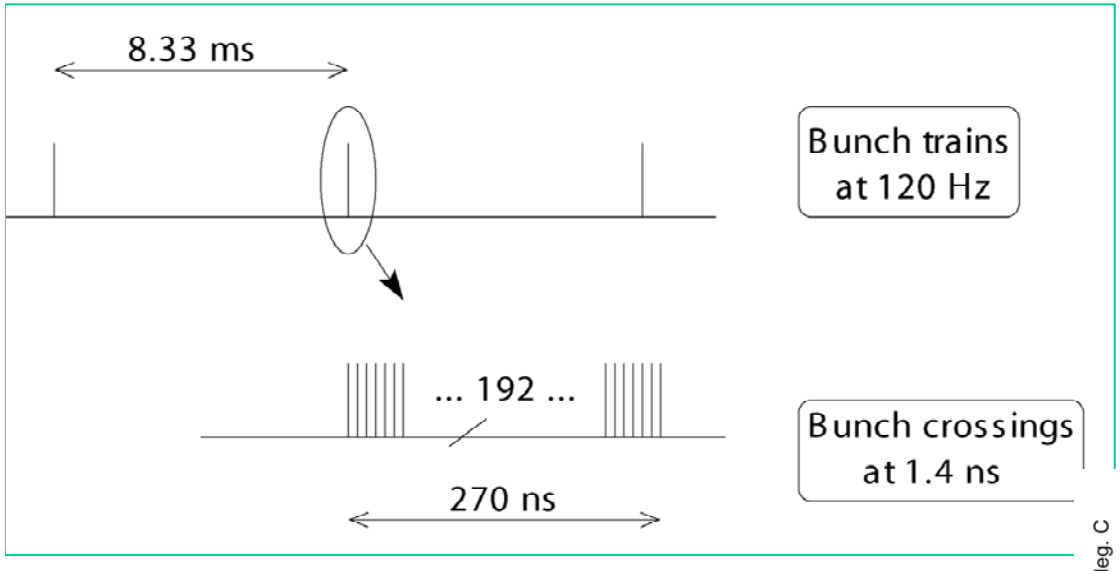
Needs to be demonstrated in a test beam!

Concerns & Issues:

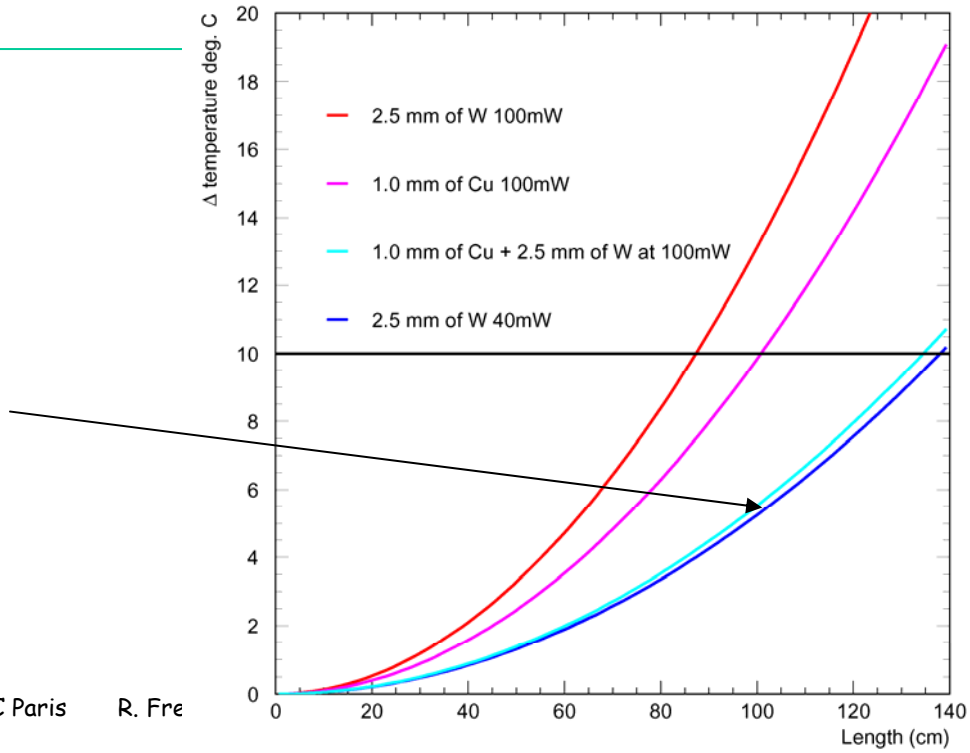
- Needs testing with real electronics and detectors
- verification in test beam
- synchronization of clocks (1 part in 20)
- physics crosstalk

- For now, assume pileup window is ~5 ns (3 bx)

Power



- Use power cycling (short LC live times) to keep average power in check
- 40 mW and no Cu look to be the realistic options



Power (contd.)

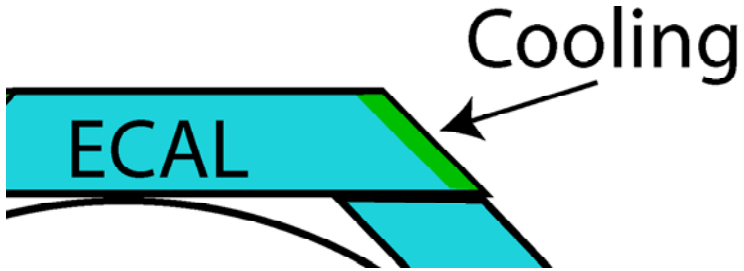
Phase	Current (mA)	Instantaneous Power (mW)	Time begin (us)	Time End (us)	Duty Factor	Average Power (mW)
All Analog "on"	370	930	0	9	0.00108	1.0
Hold "on", charge amp off	85	210	9	100	0.01092	2.3
Analog power down	4	10	100	8333	0.988	9.9
LVDS Receiver, etc		3	0	8333	1	3.0
Decode/Program		10	1	100	0.01188	0.1
ADC		100	10	500	0.0588	5.9
Readout		50	500	2500	0.24001	12.0
Total	459	1313				34.2

- < 40 mW per wafer ($\sim 10^3$ pixels)

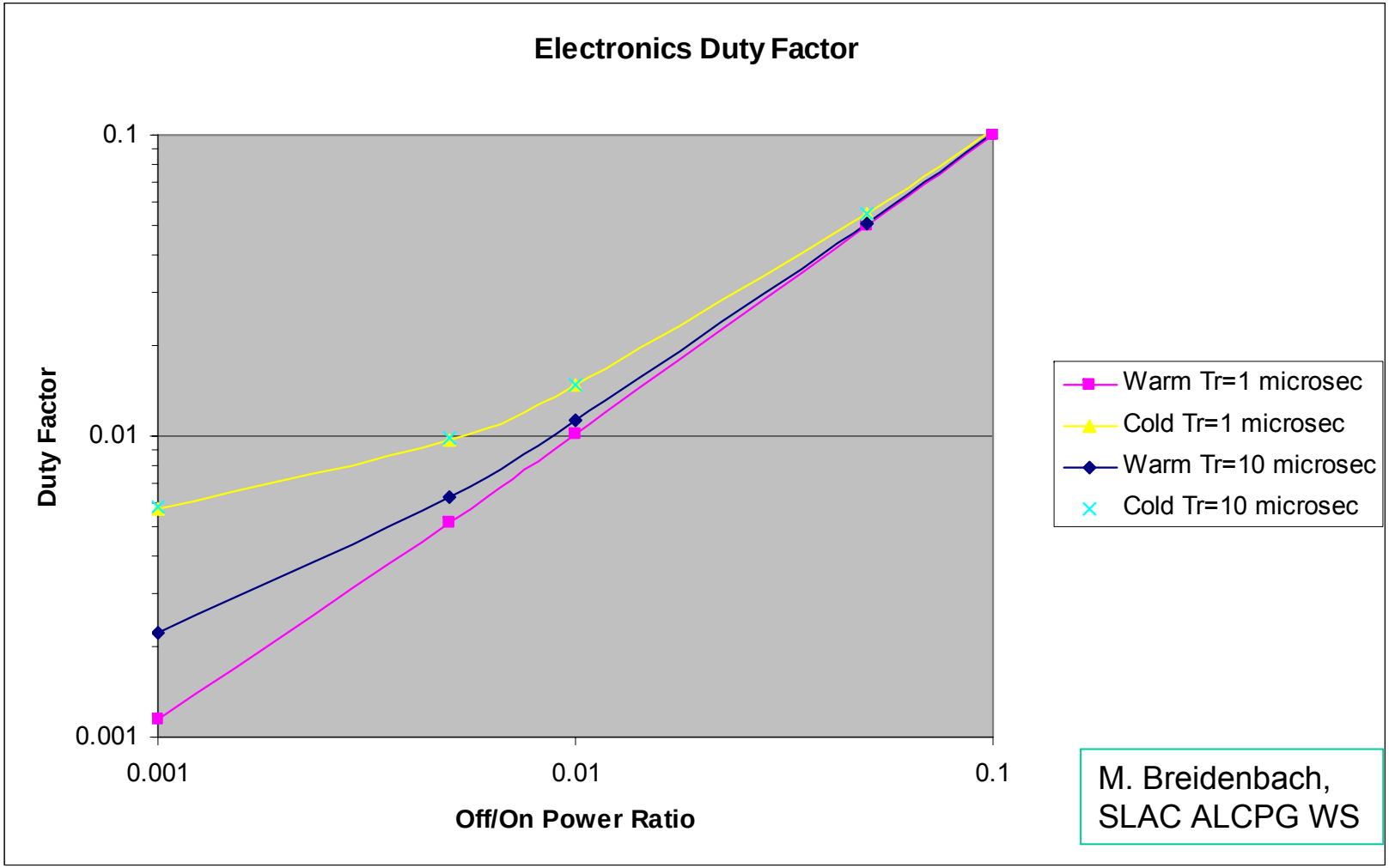
$\Rightarrow$ Passive cooling by conductance in W to module edges

  - $\Delta T \leq 5°$ from center to edge

$\Rightarrow$ Maintains small gap & Moliere radius

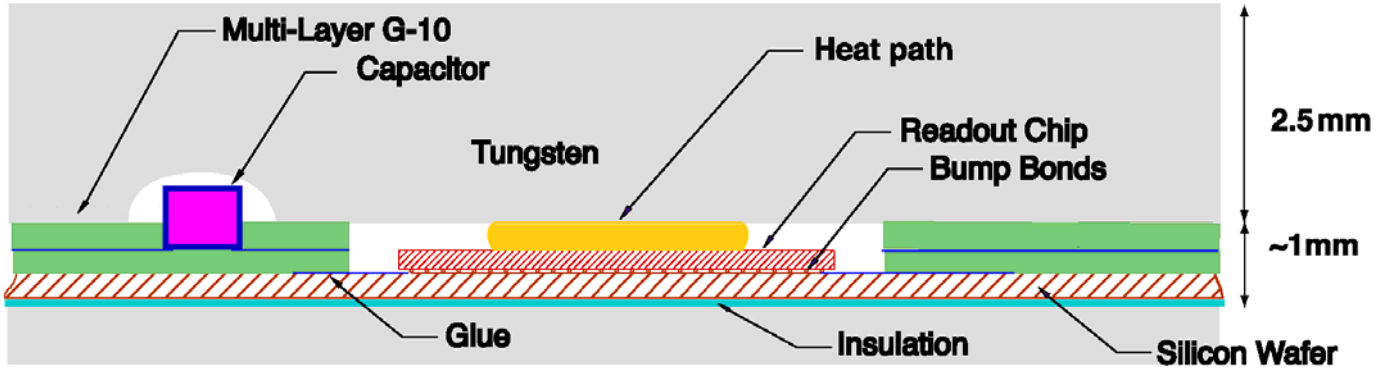


Power (contd.)

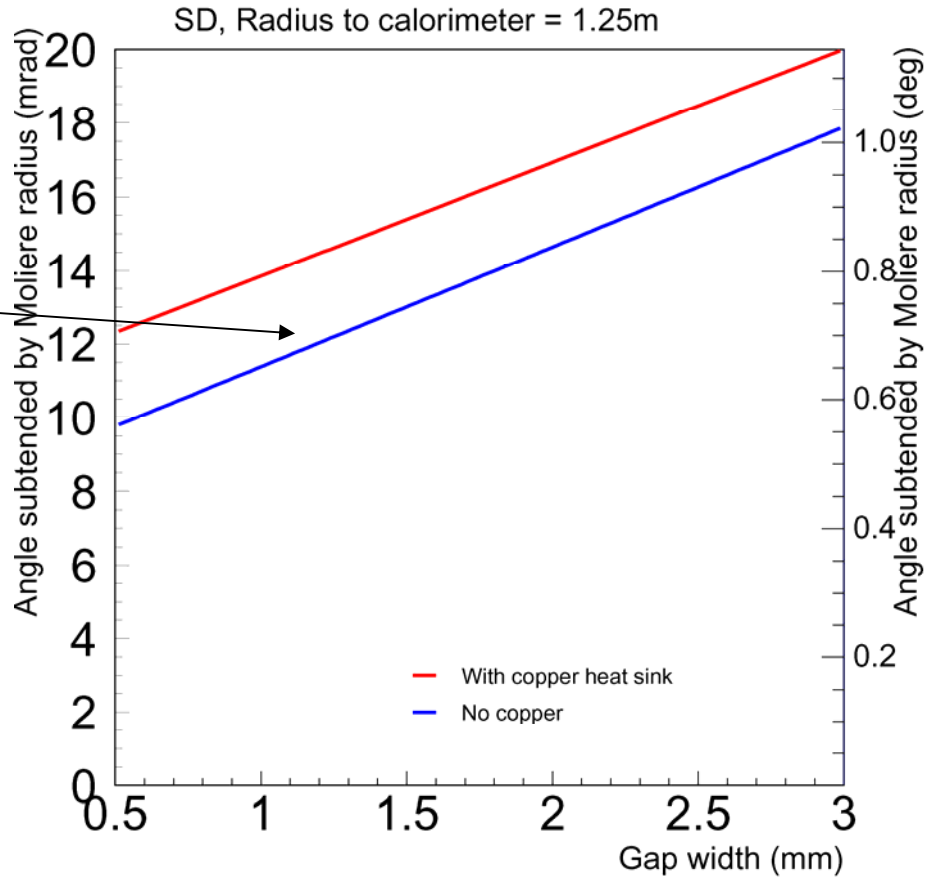


- Even though accelerator live fractions are 3×10^{-5} (warm) and 5×10^{-3} (cold), current electronics design parameters give small difference

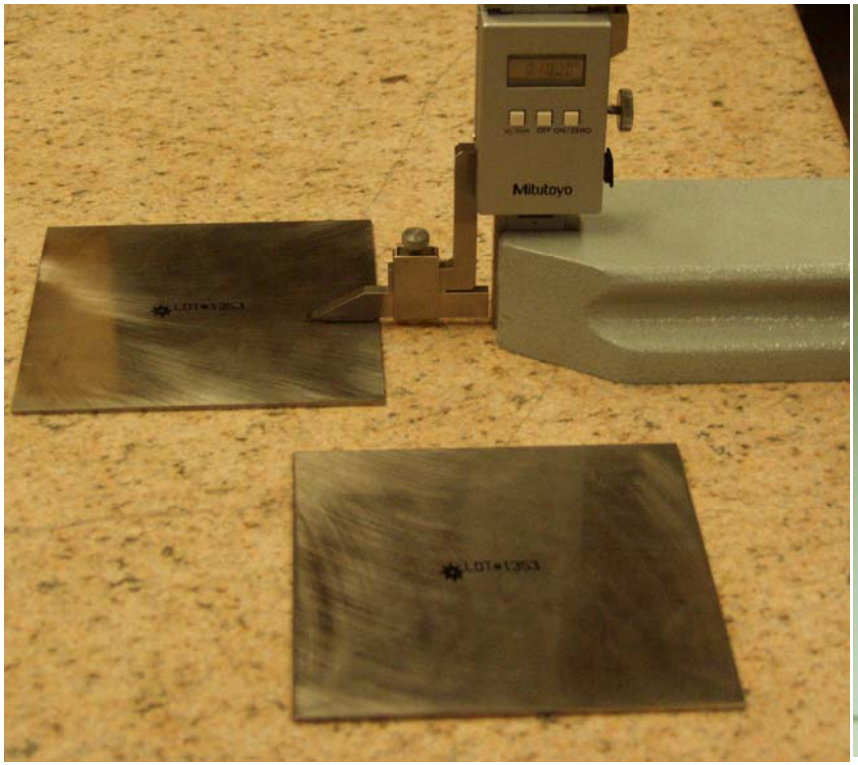
Maintaining Moliere Radius

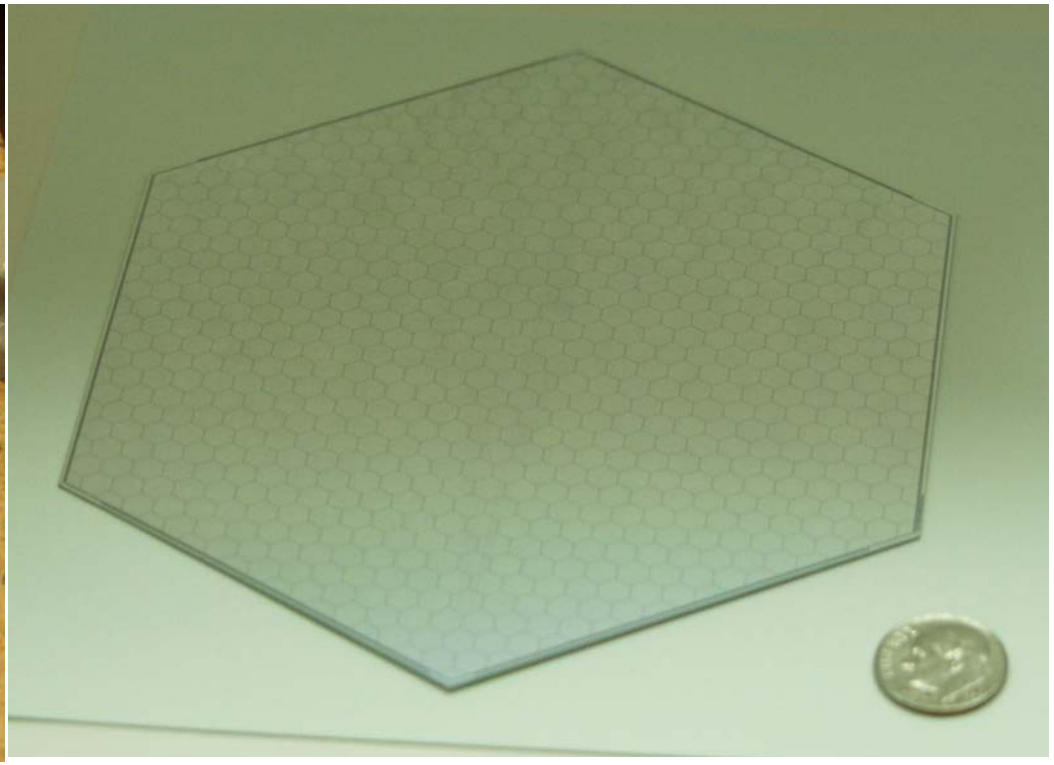


- Shouldn't need copper heat sink if present heat load estimates are correct (or close to correct).
  Angle = 11 mrad
- Compare with effective Moliere radius of 3mm at 1.7m (CALICE?):
  Angle = 13 mrad
- Capacitors may be biggest challenge



Components in hand





Tungsten

- Rolled 2.5mm
  - 1mm still OK
- Very good quality
  - < 30 μm variations
- 92.5% W alloy
- Pieces up to 1m long possible

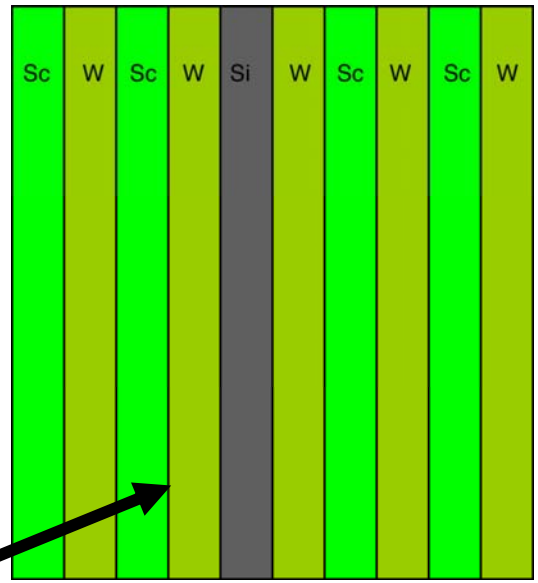
Silicon

- Hamamatsu detectors
- Should have first lab measurements soon
- (Practicing on old 1cm dets.)

Investigation & Design Optimization of a Compact Sampling ECAL with High Spatial, Timing and Energy Resolution

Contact Person : Graham Wilson, Univ. of Kansas

- **Objective: Develop a cost and performance optimized ECAL design which retains the performance advantages of the Si-W concept, but finer sampling, excellent time resolution and cost which permits placement at larger R.**
- **Investigating and comparing sampling geometries ranging from Si-W to Scintillator-W with particular emphasis on hybrid Scintillator-W-Si arrangements.**

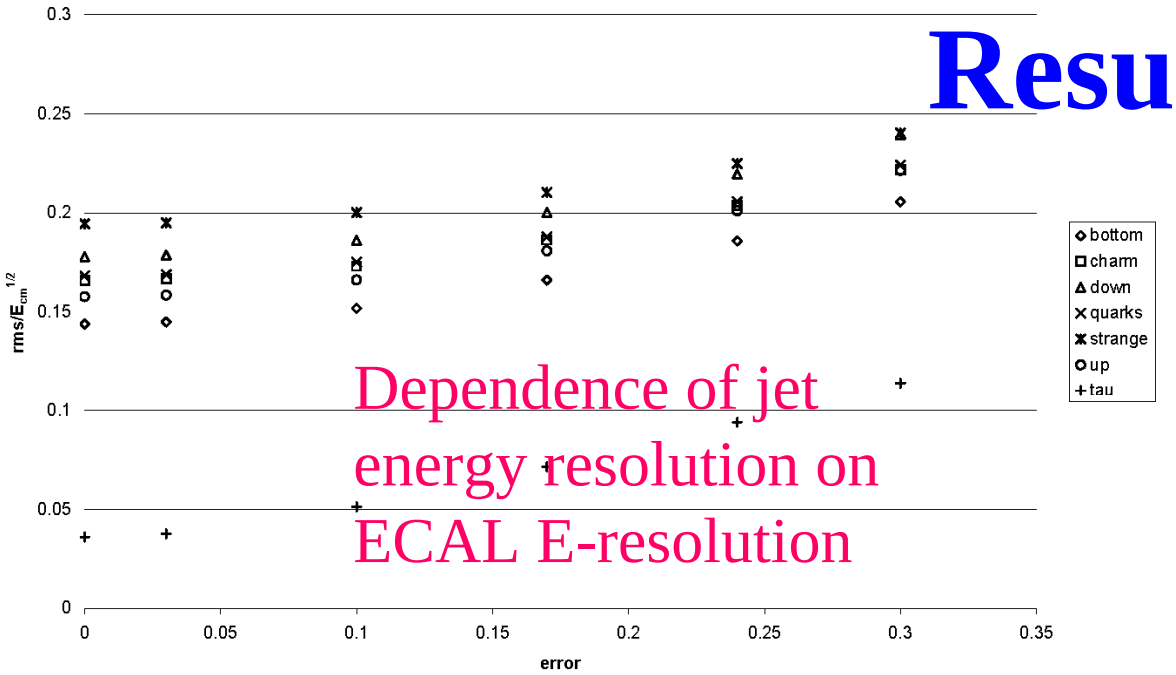


Tile-fiber considered main Scint. technology option

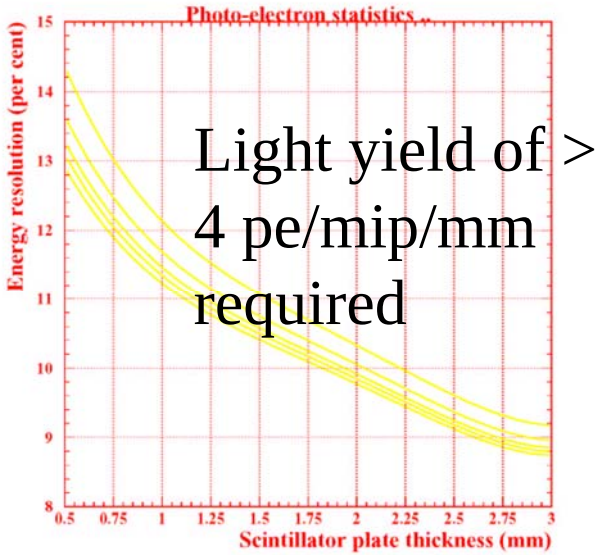
Relevance to detector design/physics performance

- Improvement in the ECAL performance in terms of :
  - i) energy resolution (15%/√E to 10%/√E) – better single particle measurements and jet energy resolution.
  - ii) timing resolution – can resolve NLC bunch crossings (1.4ns separation) and reduce $\gamma\gamma$ pile-up
  - iii) cost at fixed radius – allows placement at larger radius which improves angular resolution (and hence jet energy resolution) and allows gaseous tracking.
  - iv) position resolution – better angular resolution and jet energy measurement with particle flow algorithms

Results

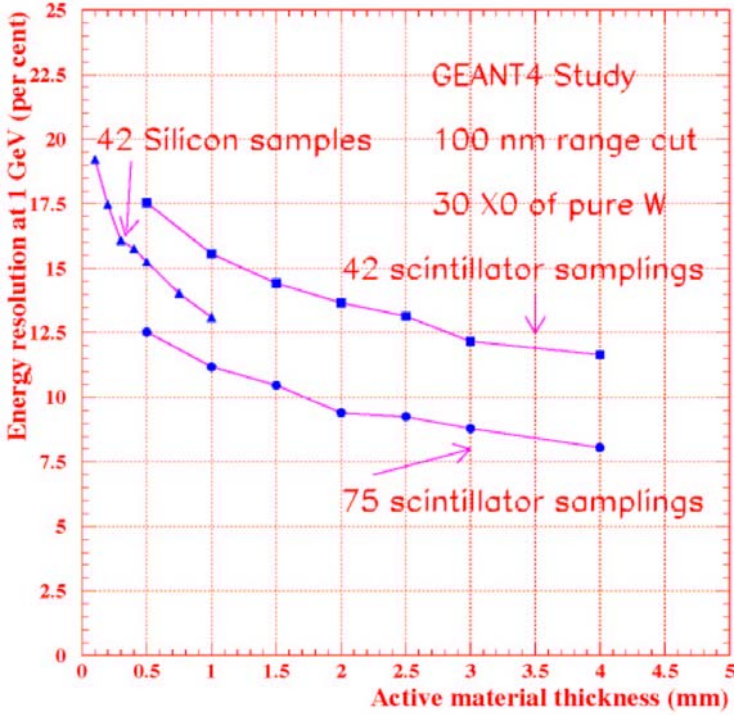


Dependence of jet energy resolution on ECAL E-resolution

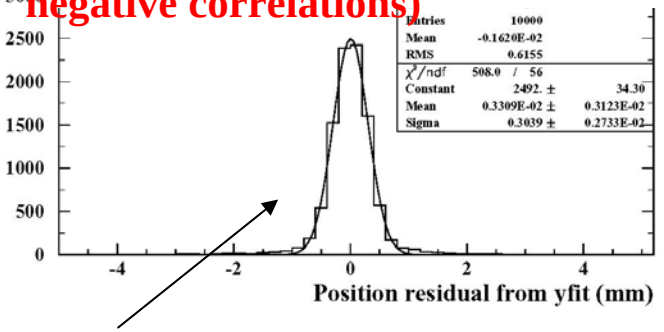


Light yield of > 4 pe/mip/mm required

Extensive study of EM energy resolution for various longitudinal configurations which retain small Moliere radius →



Hybrid sampling works :(even improves E-resolution due to negative correlations)



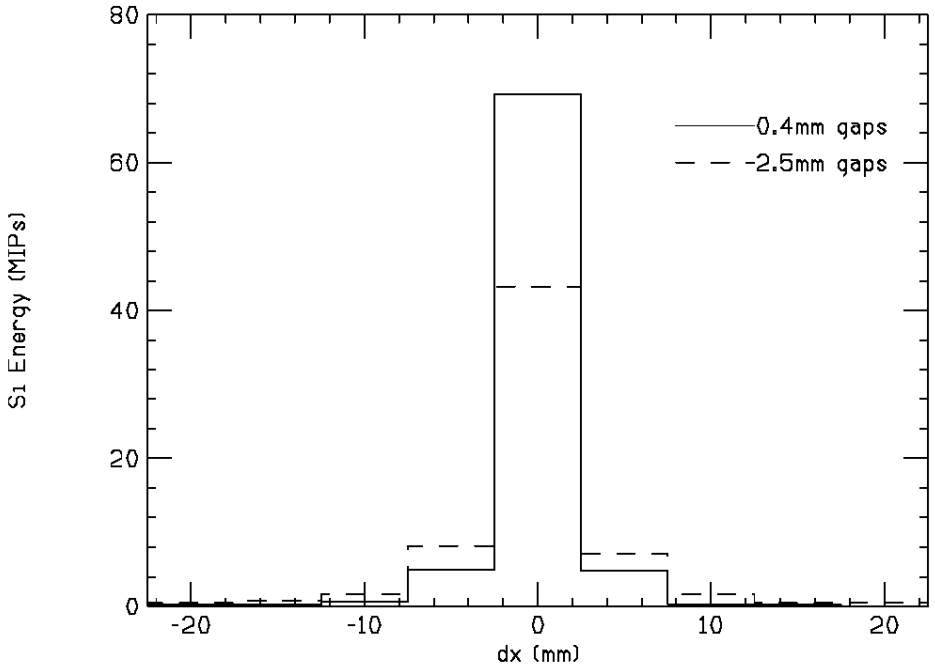
Position resolution for 1 GeV γ of 300 μm, with 1 mm Si strips at conversion point.

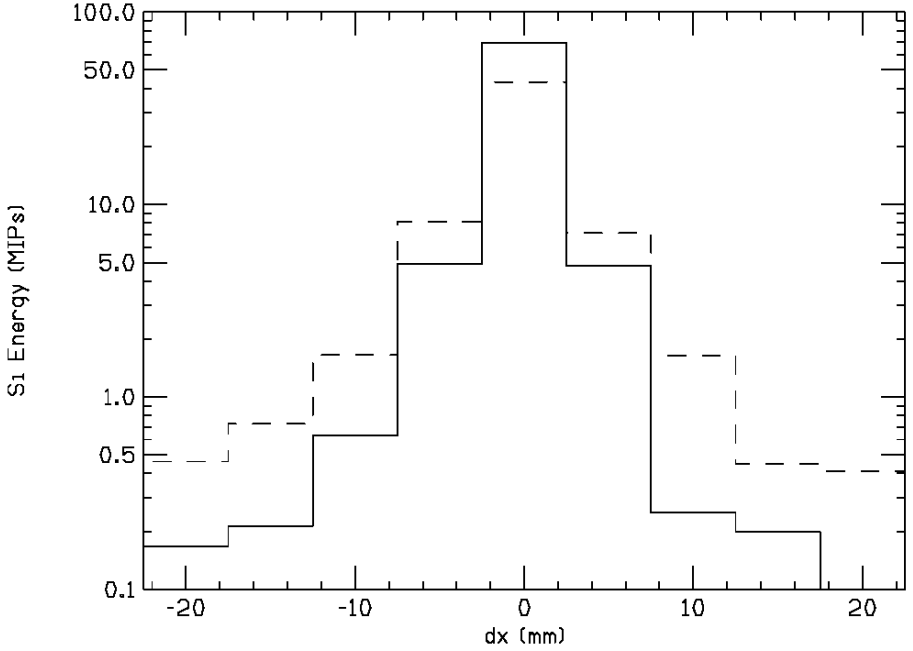
SiD Si/W Status and Plans

- Note that current design is optimized for warm, but could be optimized for cold
  - Would require digital pipeline
  - Still good to have timing?
- This year
  - Qualify detectors
  - Fabricate initial RO chip for technical prototype studies
    - Readout limited fraction of a wafer ($)
    - Bump bonding; finalize thermal plans
  - Consider technical beam test
    - Test readout, timing
  - Continue to evaluate configuration options
    - Layering, segmentation
- Next year (2005)
  - Order next round of detectors and RO chips
    - Might depend on ITRP decision
  - Design and begin fab. of prototype module for beam test
    - Full-depth, 1-2 wafer wide ECal module

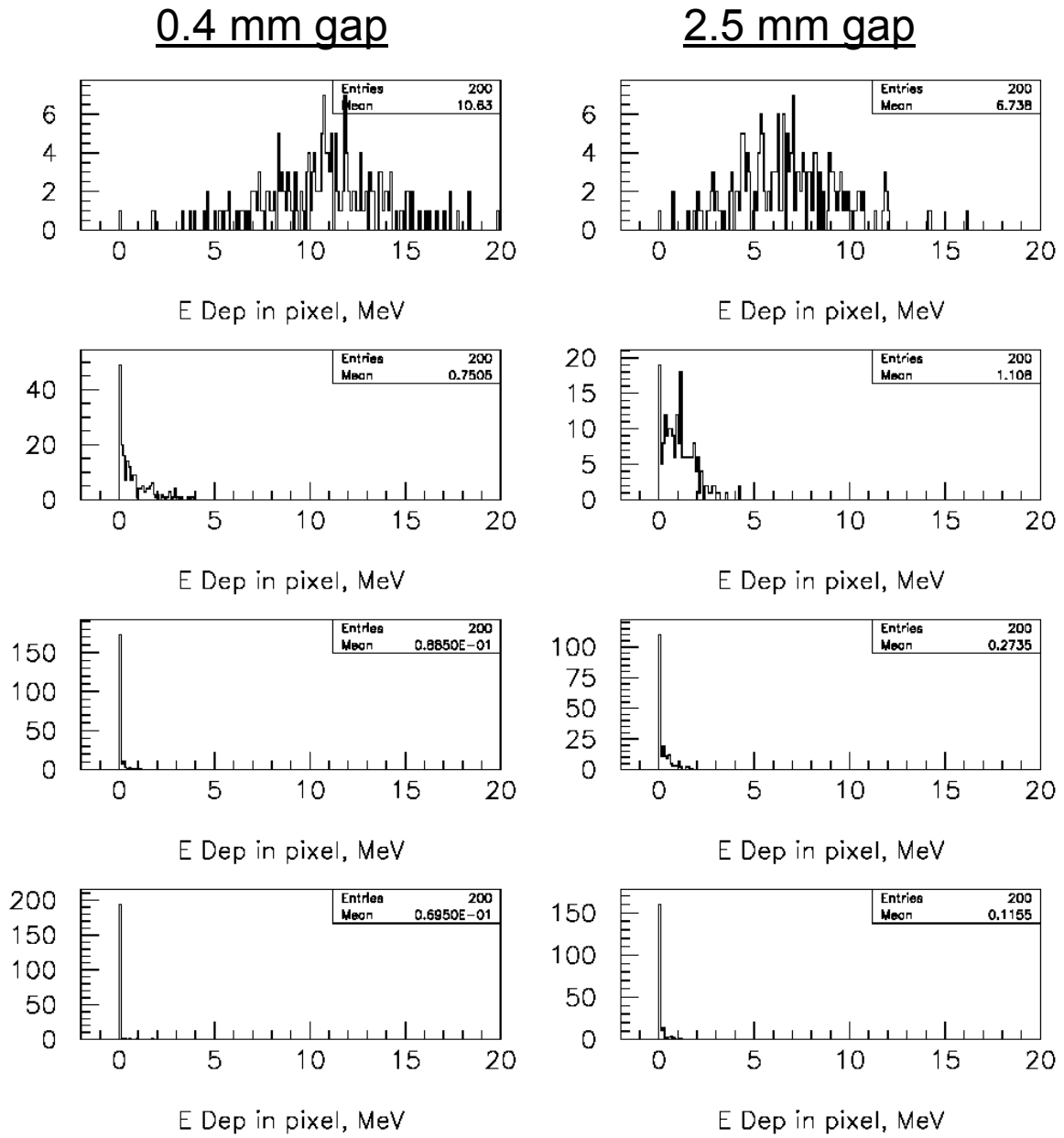
Effective Moliere radius

- Standard SD: 5x5 mm^2 pixels with (1) 0.4mm or (2) 2.5mm readout gaps.
- 10 GeV photons; look at layer 10

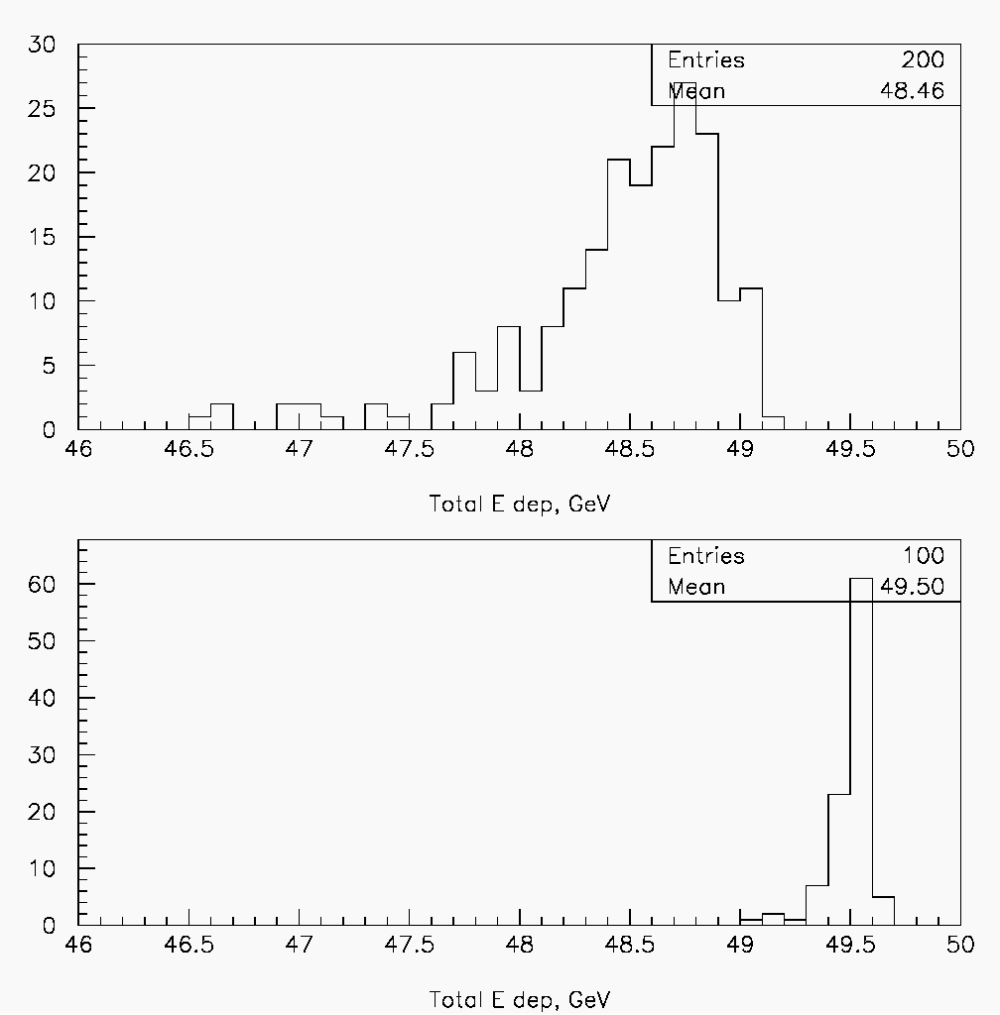




(contd)


0.4 mm gap
2.5 mm gap
dx = 0
+ 1 pixel
+ 2 pixels
+ 3 pixels
Entries 200
Mean 10.63
Mean 6.738
Mean 0.7505
Mean 1.108
Mean 0.8850E-01
Mean 0.2735
Mean 0.6950E-01
Mean 0.1155
E Dep in pixel, MeV

Alternative Sampling Configurations



50 GeV electrons

SD: 30 x 2/3 X_0

SD vB: 20 x 2/3 X_0 + 10 x 4/3 X_0

- better containment
- poorer sampling

Radiation

- EM radiation dominated by Bhabhas (in forward endcap)
  - $d\sigma/d\theta \approx 10\ pb/\theta^3$ for t-channel
  - Consider 1 ab^{-1}, 500 GeV, shower max., and θ=60 mrad (worst case)
    - Use measured damage constant (Lauber, et al., NIM A 396)

    $\Rightarrow$ ≈6 nA increase in leakage current per pixel
  - Comparable to initial leakage current
  - Completely negligible except at forward edge of endcap
- Evaluation of potential neutron damage in progress

- A 300 GeV electron shower into a readout chip?
  - "Linear Energy Threshold" (LET) is 70 MeV/mg/cm^2
  - 1 MIP in Si: 1.7 MeV/g/cm^2

  $\Rightarrow$ Expect no problems (check)