Status Report on the MAPS Detectors for the Warm and the Superconductor Options of the FLC

OUTLINE:

- Introduction of MAPS technology
- Where MAPS are, and plans for use at Vx
- How far to fulfil FLC requirements ($\tau$, $\sigma$, $\mathcal{W}$, ...)
- R Rout strategies for warm & cold FLC
- Development of fast rOut circuits
- Conclusions + future R&D

Grzegorz Deptuch, LEPSI, Strasbourg, France


and M6/M8 DAPNIA: Y.Degerli, N.Fourches, F.Ormizi, P.Lutz

depucht@lepsi.in2p3.fr
Monolithic Active Pixel Sensors (MAPS)

The detector is a standard VLSI chip. The active element is a thin moderately doped silicon layer, operated undepleted. The readout electronics is seat on top of this layer. The built-in potential, resulting from differences in doping, screens the detector from the electronics parts and confines the charge diffusing to the readout electrodes. The charge collectors are n-well/p-epi (substrate) diodes. Only NMOS transistors are used for in-pixel readout electronics, but full CMOS electronics is used on the detector periphery.

**MAPS advantages:**
- Decoupled charge sensing and signal transfer (improved radiation tolerance, random access, etc.), small pitch (high tracking precision), low amount of material, fast readout, moderate price, SoC, etc.
Introduction of MAPS technology

MAPS detectors are developed at IReS-LEPSI since 1999 for future vertex detectors (very high granularity + minimal material budget) and biomedical imaging.

First MAPS:
- ε~99%, S/N~20-40, σ~1.5-2.5 µm, σ_{2hit}~30 µm @ 20×20 µm²

The first prototypes, made of small arrays of a few thousands of pixels, demonstrated the viability of the technology and its high tracking performances. As a natural consequence, the first real scale prototype was fabricated and now tested. Following, the attention is focussed on readout strategies adapted to specific experimental conditions.
Where MAPS are, and plans for use at Vx

0.6 µm CMOS process with 14 µm epitaxial layer,
4 matrices of 510 × 512 pixels read-out in parallel; pixel: 17 × 17 µm², diodes: P1 - 9.6 pm², P2 - 24.0 pm², control logic and all pads aligned along one side,

Results:

- Noise mean ENC: 20.74 e⁻
- Single pixel S/N mean: 22.73
- Detection efficiency e: 99.3%
- Spatial resolution s: 1.7 µm
- Pixel-pixel gain nonuniformity: ~3%
- Macro-scale gain nonuniformity: ~0.2%
Design details and requirements:
small radius and thin: 2 pixel layers \(\sim 1000 \text{ cm}^2\),
25 ladders, \(\sim 100 \times 10^3\) pixels, \(R_{L1} \sim 1.5\) cm, \(R_{L2} \sim 4\) cm
silicon thickness \(\sim 50\ \mu\text{m}\), pitch \(20 \times 20\ \mu\text{m}^2\ - 30 \times 30\ \mu\text{m}^2\)
readout speed 10-20 ms thus 50 Hz – 100 Hz
**MIMOSA - STAR CHIP**

- subdivision in 10 groups of 64 × 640 pixels read-out in parallel with multiplexed outputs,
- each group splitted in 2 sub-groups of 32 columns *(to gain in speed)*,
- active area: 19.2 × 19.2 mm², readout part: 1.5-1.7 × 19.2 mm², chip dimensions: 19.2 × 19.2 mm²,
- clocks: pixel level - slow *(power + noise)*; chip processing level - fast *(small total integration time <5ms)*,
- continuous frame analogue readout option: single fast *(100 MHz multiplexed output)* or 10 slow parallel outputs,
- JTAG remote control *(bias + tests)*.

**CHIP UNDER DEVELOPMENT - SUBMISSION OF SMALL PROTOTYPE (2×64×128) IN TSMC 0.25 µm (8 µm EPI-LAYER) IN JULY 2004**
MIMOSA - STAR CHIP ARCHITECTURE

New STAR VxD is an interesting and important experience for both MAPS technology and engineered detector design.
How far to fulfil FLC requirements ($\gamma$, $\sigma$, $\omega$ ...)

Radiation Hardness

Neutron Irradiations

Tests up to $10^{13} n_{1MeVeq}/cm^2$ fluences up to $10^{12} n_{1MeVeq}/cm^2$ are still acceptable (2 orders of magnitude above FLC requirements=10$^9 n_{1MeVeq}/cm^2/year$).

Ionising Irradiations

doses up to this level acceptable above FLC requirements 50 krad/year, exact sources of performance losses under investigation (diode size and placements of transistors are important parameters).

Tracking Performances

Impact Point Spatial Resolution

$\sigma_{sp}=2-2.5$ $\mu$m for 3 bits encoding, $\epsilon_{tr}$ close to 100%, double hits distinguishable down to 30 $\mu$m distance.

Material Budget

The goal of $X/X_0=\sim0.1\%$/layer achievable in thinning to 50 $\mu$m, recent achievement: thinning to 15 $\mu$m for backside exposition for low energy $\beta$ detection.
How far to fulfil FLC requirements ($\gamma$, $\sigma$, $\mathcal{W}$, ...)

MIMOSA TECHNOLOGY OPTIONS

- Original MAPS implementations use the epitaxial layer as a sensitive volume. Alternatively, non-epitaxial, intrinsically lightly doped substrates, typical for RF CMOS, can also be used.

**MIMOSA IV no epi (summary):**

- SB design $\varepsilon \sim 99.5\%$, $\sigma \sim 2.5$ $\mu$m, @ 20x20 $\mu$m²

**SUCCESSOR II no epi (summary):**

- SB design $\varepsilon \sim 99.9\%$, $\sigma \sim 5$-6 $\mu$m (larger diodes) @ 40x40 $\mu$m²

Expanding market of commercial visible light imagers entails equal development of dedicated fabrication processes. Those become available for wide public - **MIMOSA IX** submitted for fabrication using such a dedicated process...

- mixed-signal polycide gate CMOS, 4 metal, 2 poly, high-resistive poly, 3.3V and 5V gates,
- optimized N-well diode leakage current $<45$ pA/mm² @ 27 °C - according to foundry documentation,
- $\sim20$ $\mu$m epitaxial lightly doped substrate, (samples on non-epi high resistivity substrate also available),
- availability in multiproject submissions in 2004 - reasonable pricing.
**DETERMINATION OF THE READOUT SPEED**

- **Beamstrahlung (TESLA):**
  
  according to simulations one may expect:

  \[ N|_{90°} \approx 5e^\pm/cm^2/BX @ 500 \text{ GeV and } R_{L1}=15\text{mm} \]

  deducing occupancy one finds \( \approx 3\text{-}5\% \) in 100 \( \mu \)s \( m_{\text{clus}} \approx 5 \)

  \( t_{L1-L2} \approx 25\text{-}50 \) \( \mu \)s (R&D running)

  \( t_{L3-L5} \approx 100 \text{ up to } 200 \) \( \mu \)s (achieveable with current state of MAPS development)

- **Machine time structure cold and warm LC**
  
  - multiple readout during beam-on *(train)* interval with on-line signal processing and result data transfer,
  
  - multiple sampling of signals during beam-on *(train)* time onto on-pixel capacitors and readout in between trains.

  - fast, column || on line data processing with hit/cluster selection.

  integration over single train and data transfer in between trains, possible data processing with hit/cluster selection for data reduction.
**Readout Strategies for Warm & Cold FLC**

**Readout of L3-L5 for Cold LC**

- **Train**: ~1 ms
- **Processing and Readout**: <199 ms
- **1 Cycle**

```
<table>
<thead>
<tr>
<th>BX's nBX's integrated</th>
<th>BX's nBX's integrated</th>
<th>BX's nBX's integrated</th>
</tr>
</thead>
<tbody>
<tr>
<td></td>
<td></td>
<td></td>
</tr>
</tbody>
</table>
```

```
<table>
<thead>
<tr>
<th>S/H cell 1</th>
<th>S/H cell 2</th>
</tr>
</thead>
<tbody>
<tr>
<td>time</td>
<td></td>
</tr>
</tbody>
</table>
```

"COLD LC":
- Rep. rate 4...5 Hz, BX/train 2820...4886, BX sep. 337...176 ns
- Dead time ~199 ms

On detector data sparsification is optional

- Multiple scans of the whole detector with sampling data on pixel at the required speed (~200 μs) during the beam-on interval and then read the samples out when the beam is off.

**For L1 & L2 development of fast parallely processing µcircuits is necessary!**

**Or more cells and faster scan?**
readout strategies for warm & cold FLC

**Readout for Warm LC**

- **TRAIN** ~267 ns
- PROCESSING and READOUT <10 ms
- 1 CYCLE

"WARM LC":
- rep. rate 100...150 Hz, BX/train 192, BX length 267 ns
- ⇒ dead time ~6.6...10 ms
- sparsified data on detector data sparsification is optional

- only two on pixel memory cells (for beginning and end of integration levels) are required,
- can be fitted with pixel designs MIMOSA VI, VII, VIII and IX,
- integration over 192 BX within one train,
Rdout strategies for warm & cold FLC

Readout of L3-L5 for cold LC

- use of auto reverse bias system for charge collecting diode,
- only NMOS AC-coupled amplifier,
- coupling of each memory cell to separate SF transistor, charge division and no gain loosing.

Similar to FAPS from RAL but...
Development of fast readout circuits

MIMOSA VI

MIMOSA VI - first tested device, integrating on-pixel voltage mode memory cells, column || readout, and discrimination stages.

Main features:
- Mixed 0.35 µm process with 4 µm epitaxial layer,
- Array of 128 rows × 30 columns read in || with CDS + signal discrimination (total 25 µs)
- AC coupled on-pixel voltage amplifier + CDS,
- Conversion gain ~6.5 nA/e−,

pixel + basic processing needs power typically 3-5 × 100 µW /col./rd cycle

MIMOSA VI pixel and discriminator tests summary

<table>
<thead>
<tr>
<th>MIMOSA VI</th>
<th>features</th>
</tr>
</thead>
<tbody>
<tr>
<td>performances of chip designed</td>
<td>noise ENC: ~20 e−, conversion gain: 6.5 nA/e−, pixel dispersions: ~120 e−</td>
</tr>
<tr>
<td>discriminator performances</td>
<td></td>
</tr>
<tr>
<td>τ1 ns</td>
<td>τ2 ns</td>
</tr>
<tr>
<td>90</td>
<td>15</td>
</tr>
<tr>
<td>75</td>
<td>12.5</td>
</tr>
<tr>
<td>60</td>
<td>15</td>
</tr>
</tbody>
</table>

LEPSI
iRes

MVI designed in coll. with CEA/DAPNIA.
**Development of Fast Readout Circuits**

**MIMOSA VII**

**MIMOSA VII - MAPS device** integrating pixel with charge sensitive element similar to DEPFET, but all processing electronics integrated on the same circuit!

- **Main Features:**
  - Mixed 0.35 µm process w/o epitaxial layer,
  - Array of 64 rows x 16 columns read in || with CDS (total 20 µs)
  - PhotoFET CSE,
  - Conversion gain ~500 pA/e-

**PhotoFET Possibility of Ganging Outputs for Preselection of Zones for Readout**

**Tests Under Preparation.**

---

**Notes:**

- Pitch 25 × 25 µm²
Development of fast readout circuits

MIMOSA VIII

- Main features:
  - Digital 0.25 µm process with 8 µm epitaxial layer,
  - Array of 128 rows × 32 columns read in || with CDS + signal discrimination (total 20 µs)
  - Only NMOS transistors + n-well/p-epi diodes,
  - DC and AC coupled on-pixel voltage amplifiers + CDS,
  - Conversion gain 30-60 µV/e⁻ and 150 µV/e⁺.

Tests under preparation.

MVIII designed in coll. with CEA/DAPNIA.
Conclusions + future R&D

›› MAPS technology proved for high performance charged particle tracking,

›› MAPS Know-How close to satisfy warm LC,

... and for external layers of cold LC,

›› STAR VxD pioneering the use of MAPS,

›› Tests of the second generation detectors M6/M7/M8/M9 will help to chose working-horse for future development - including fast and intelligent detector (more advanced pixel arch. than class. 3T),

›› R&D necessary for L1 & L2 of cold LC (prototyping and testing - but there are candidates),

›› Other experiments e.g. CBM @ GSI (rad. hardness + readout speed more agressive) are joining,

›› Be prepared to face surprises, e.g. beam pick-up noise, etc.