Silicon Strip Sensor R&D Activity in Korea

- Introduction
- Strip Sensor Design and Simulation
- Preliminary Measurement Results
- Readout Design
- Summary

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Generic Silicon R&D
- experiment high physics
- astroparticle physics
- nuclear physics
- medical physics

- Kyungpook National University (H.J. Kim, Y.J. Kim, H. Park, D. Shim)
- Ewha Womens University (I.H. Park, M.Y. Kim)
- Seoul National University (J. Lee)
- Yonsei University (Y. Kwon, S.P. Kim)
- Chonnam National University (B.G. Cheon)
- Sungkyunkwan University (Y.I. Choi, Y. Choi)
Introduction: Background

Design and Fabrication of Silicon Pixel Detector for CREAM (Cosmic Ray Energetics And Mass) experiment: a balloon experiment to measure energy spectrum from $10^{12}$ to $10^{15}$ eV over elemental range from proton to iron.
Introduction: Detector Configuration of GLC

- CDC, 50 wires
- Support Tube
- IT, 5 layers
- VTX, 4 layers
- Beam pipe

- 5 layers at r=9 to 37 cm
- Angular coverage: $|\cos \Theta| < 0.9$
- Spatial resolution: $\sigma = 40 \mu m$
- Thickness of a layer: 0.6% radiation length

- Improve linking efficiency of CDC track to corresponding VTX hits
- Reconstruction efficiency of low momentum tracks and of particles which decay between VTX and CDC
- Momentum resolution of tracks
Double-Side Silicon Strip Sensor Design

- double sided silicon strip
- tree metal process
- implant strips in ohmic side are orthogonal to those in junction side
- readout strips in junction side have the same direction as that of ohmic side

Front Side:
- brown: implanted n+
- blue: p-stop
- sky blue: SiO2
- gray: Al for readout

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Silicon Strip Sensor Simulation

N-type wafer (100um)

Pitch = 50um

N-type wafer (100um)

2.4pA @ 6V

IV Curve
MASK for n+ side

N-side 1st MASK
p+ implant

N-side 3rd MASK
Metal Contact

N-side 4th MASK
Metal

N-side 2nd MASK
Open
n+ implant

5th MASK
MASK for p+ side
Silicon Strip Sensor Types

allowance for handling in fab.

6 inch mask

5 inch wafer

1st sensor (base)

2nd sensor

3rd sensor

2nd sensor

3rd sensor
Silicon Strip Sensor Prototype

- n+ implanted
- p-stop in atoll
- readout pad in staggering
- guard ring
- p+ implanted
- via in hourglass
- readout strip

N+ side

P+ side
**N-side measurement**

- **p_stop pad**
- **n bulk pad**
- **n+ guard-ring pad**
- **ground**

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**Probe**

**n+ guardring/n+strip & p-stop.**

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**Graph:**
- **Capacitance (F)**
  - 4.50E-010
  - 4.00E-010
  - 3.50E-010
  - 3.00E-010
  - 2.50E-010
  - 2.00E-010
  - 1.50E-010
  - 1.00E-010

- **Bias voltage (V)**
  - 0
  - 2
  - 4
  - 6
  - 8
  - 10
P-side measurement

probe
n bulk pad(+) on n-side
&
p-guardring(ground) / p-strips

p+ guard-ring pad

n bulk pad

N-side

Silver paste
single p-strip IV (1st Run)

Leakage current (A) vs. Reverse bias voltage (V)

- Type1_IV_guard
- Type1_IV_single_1
- Type1_IV_single_101
- Type1_IV_single_120
- Type1_IV_single_13
- Type1_IV_single_141
- Type1_IV_single_160
- Type1_IV_single_17
- Type1_IV_single_181
- Type1_IV_single_21
- Type1_IV_single_25
- Type1_IV_single_29
- Type1_IV_single_33
- Type1_IV_single_37
- Type1_IV_single_41
- Type1_IV_single_44
- Type1_IV_single_5
- Type1_IV_single_61
- Type1_IV_single_80
- Type1_IV_single_9
Strip leakage current ~6nA (increased by ~ 5nA compared to 1st run) as expected due to deep drive-I n of n & p junctions
single p-strip CV (1st Run)

Need more statistics !!!

 Capacitance ($F$)

Reverse bias voltage (V)

[Graph showing a decreasing trend in capacitance with increasing reverse bias voltage.]
Schematics of Readout and DAQ for DSSD

- DSSD
- Flex cable
- RC chip
- HV
- VA1(-TA)
- FPGA
- FADC
- USB2 DAQ

Control Signal

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Status and Plan for Readout and DAQ

- Flex cable to be designed and produced (size and line definition to be determined)
- RC chips (8) in hand
- VA1 chips (10) and VA-CA test board purchased (VA1-CA test and VA1 chip wire bonding necessary, and VA-TA chip to be purchased)
- FADC (25 MHz)+USB2 board and DAQ ready (need a FPGA program to operate VA chip)
- Hybrid board (RC+VA+FADC+USB2) to be designed
### VA-CA test board

#### Pin Assignment Table

<table>
<thead>
<tr>
<th>Pin</th>
<th>Signal</th>
<th>Pin</th>
<th>Signal</th>
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<tbody>
<tr>
<td>1</td>
<td>gnd</td>
<td>2</td>
<td>gnd</td>
</tr>
<tr>
<td>3</td>
<td>n.c.</td>
<td>4</td>
<td>gnd</td>
</tr>
<tr>
<td>5</td>
<td>outm</td>
<td>6</td>
<td>gnd</td>
</tr>
<tr>
<td>7</td>
<td>gnd</td>
<td>8</td>
<td>outp</td>
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<tr>
<td>9</td>
<td>Avss</td>
<td>10</td>
<td>gnd</td>
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<td>11</td>
<td>Cal</td>
<td>12</td>
<td>Avss</td>
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<td>13</td>
<td>Vfs</td>
<td>14</td>
<td>Pre_bias</td>
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<tr>
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<td>Vfp</td>
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<td>Cal_r</td>
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<td>Vdd_r</td>
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<tr>
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<td>Vss_r</td>
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<tr>
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<td>Gnd_r</td>
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<td>Vfp_r</td>
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<td>31</td>
<td>Extra1</td>
<td>32</td>
<td>Extra2</td>
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<tr>
<td>33</td>
<td>Vdd</td>
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<tr>
<td>35</td>
<td>Holdb</td>
<td>36</td>
<td>Shift_out</td>
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<tr>
<td>37</td>
<td>Mon10/bi11</td>
<td>38</td>
<td>Ck</td>
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<tr>
<td>39</td>
<td>Dreseth</td>
<td>40</td>
<td>Dresethb</td>
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<td>41</td>
<td>Shift_inb</td>
<td>42</td>
<td>n.c.</td>
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<tr>
<td>43</td>
<td>Ckb</td>
<td>44</td>
<td>Hold</td>
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<td>45</td>
<td>Teston</td>
<td>46</td>
<td>Vss (del_on)</td>
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<tr>
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<td>Dvdd</td>
<td>48</td>
<td>Dvss</td>
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<tr>
<td>49</td>
<td>Dvdd</td>
<td>50</td>
<td>Dvss</td>
</tr>
</tbody>
</table>

This is the pin assignment list for the ‘Standard VA interface’ used by the VA2CA evaluation board.

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Summary and Plan for Silicon Strip R&D

• 1st & 2nd runs of prototype fabrication were done
  - manual measurement in progress (pain stacking!)
• 3rd run being splitted (April) with feedback from test measurements
  - 2 for same process as 1st & 2nd runs
  - 2 for spray implantation
  - 2 for double implantation

• automatic probe station & wirebonder purchased and installed
  - faster and more reliable measurement
• probe card design in progress
• design revision will be needed
• test patterns should be added
• simulation in progress
• readout & DAQ design and production in progress

Stay Tuned!