

Silicon Strip Sensor R&D Activity in Korea

- Introduction
- Strip Sensor Design and Simulation
- Preliminary Measurement Results
- Readout Design
- Summary

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Generic Silicon R&D

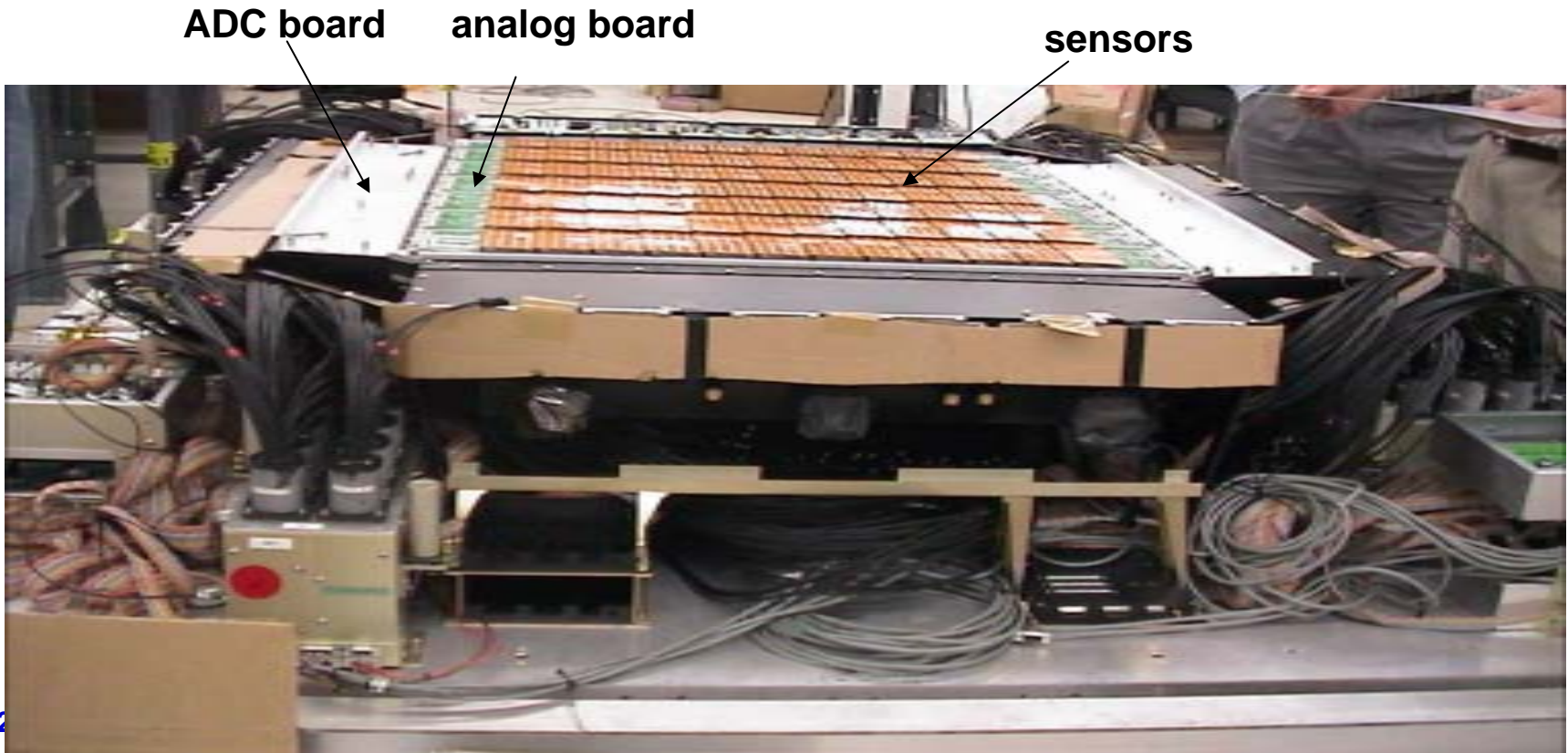
- experiment high physics
- astroparticle physics
- nuclear physics
- medical physics
- :



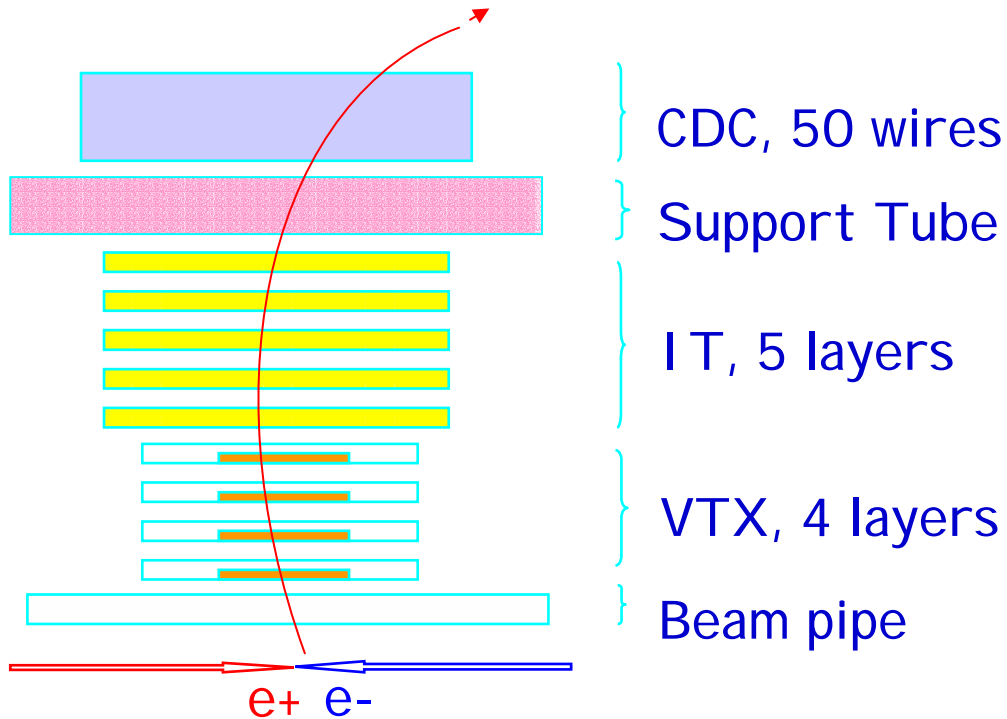
- Kyungpook National University (H.J. Kim, Y.J. Kim, H. Park, D. Shim)
- Ewha Womens University (I.H. Park, M.Y. Kim)
- Seoul National University (J. Lee)
- Yonsei University (Y. Kwon, S.P. Kim)
- Chonnam National University (B.G. Cheon)
- Sungkyunkwan University (Y.I. Choi, Y. Choi)

Introduction : Background

Design and Fabrication of Silicon Pixel Detector for CREAM (Cosmic Ray Energetics And Mass) experiment : a balloon experiment to measure energy spectrum from 10^{12} to 10^{15} eV over elemental range from proton to iron.



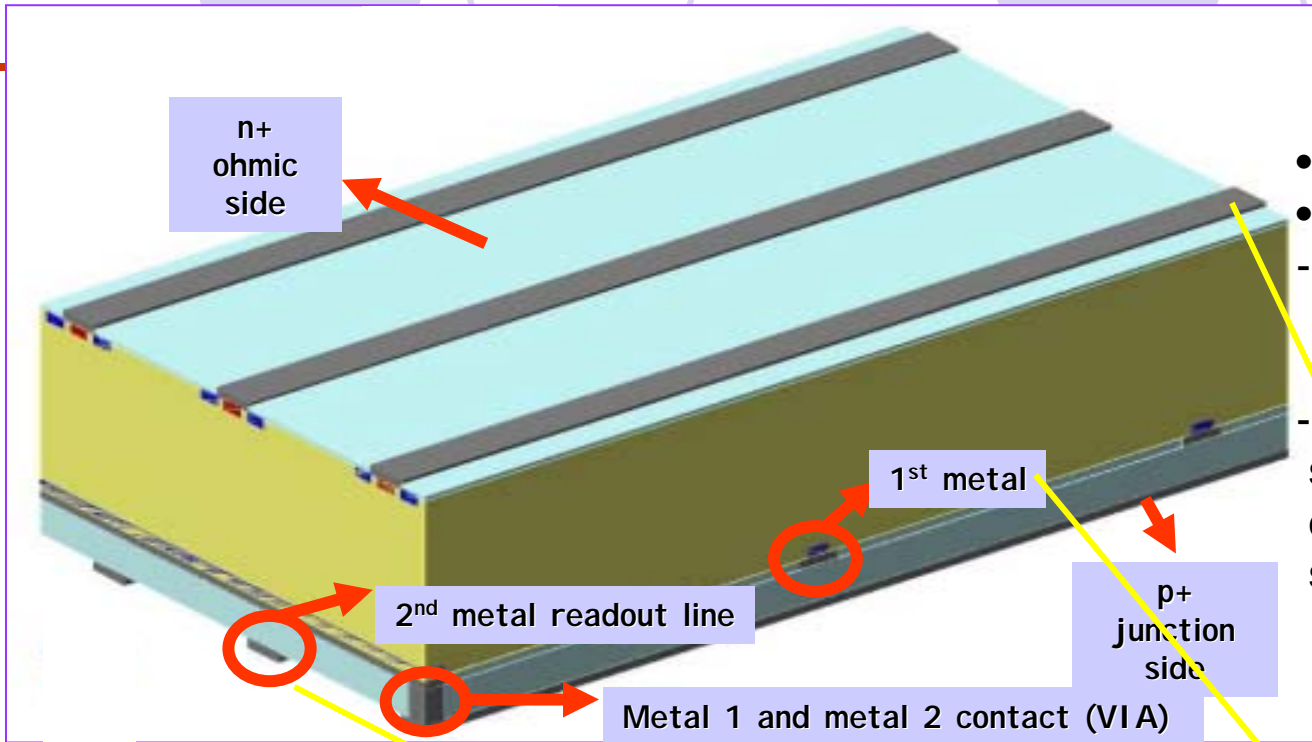
Introduction : Detector Configuration of GLC



- 5 layers at $r=9$ to 37 cm
- angular coverage:
 $|\cos\Theta| < 0.9$
- spatial resolution:
 $\sigma = 40\mu\text{m}$
- thickness of a layer:
0.6% radiation length

- improve linking efficiency of CDC track to corresponding VTX hits
- reconstruction efficiency of low momentum tracks and of particles which decay between VTX and CDC
- momentum resolution of tracks

Double-Side Silicon Strip Sensor Design



- double sided silicon strip
- tree metal process
- implant strips in ohmic side are orthogonal to those in junction side
- readout strips in junction side have the same direction as that of ohmic side

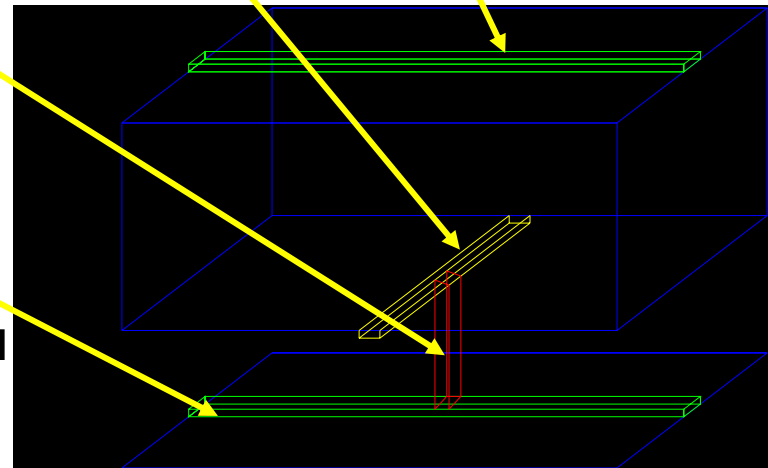
Front Side:

- brown: implanted n+
- blue: p-stop
- sky blue: SiO₂
- gray: Al for readout

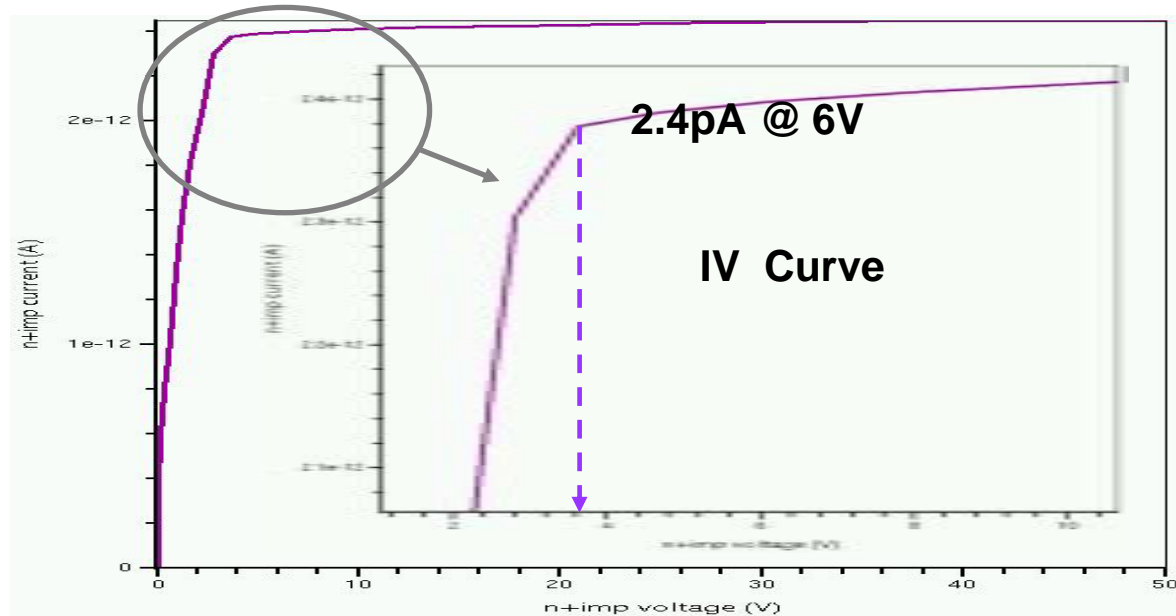
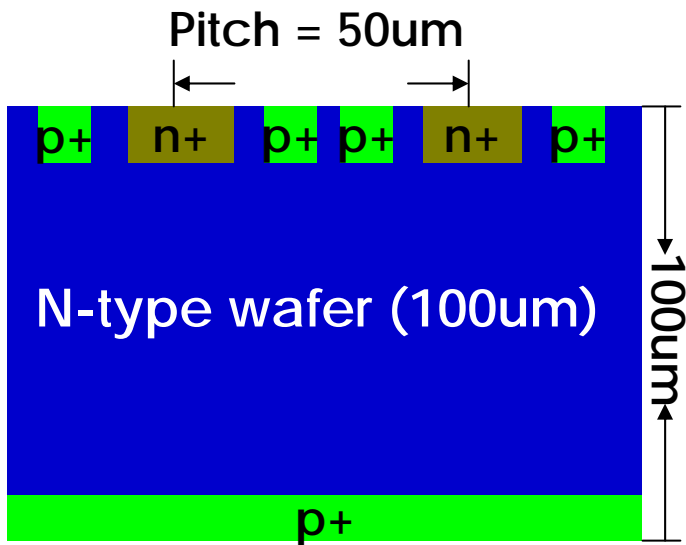
Back Side:

- blue: implanted p+
- first gray: 1st metal
- sky blue: SiO₂
- vertical gray: VIA
- second gray: 2nd metal

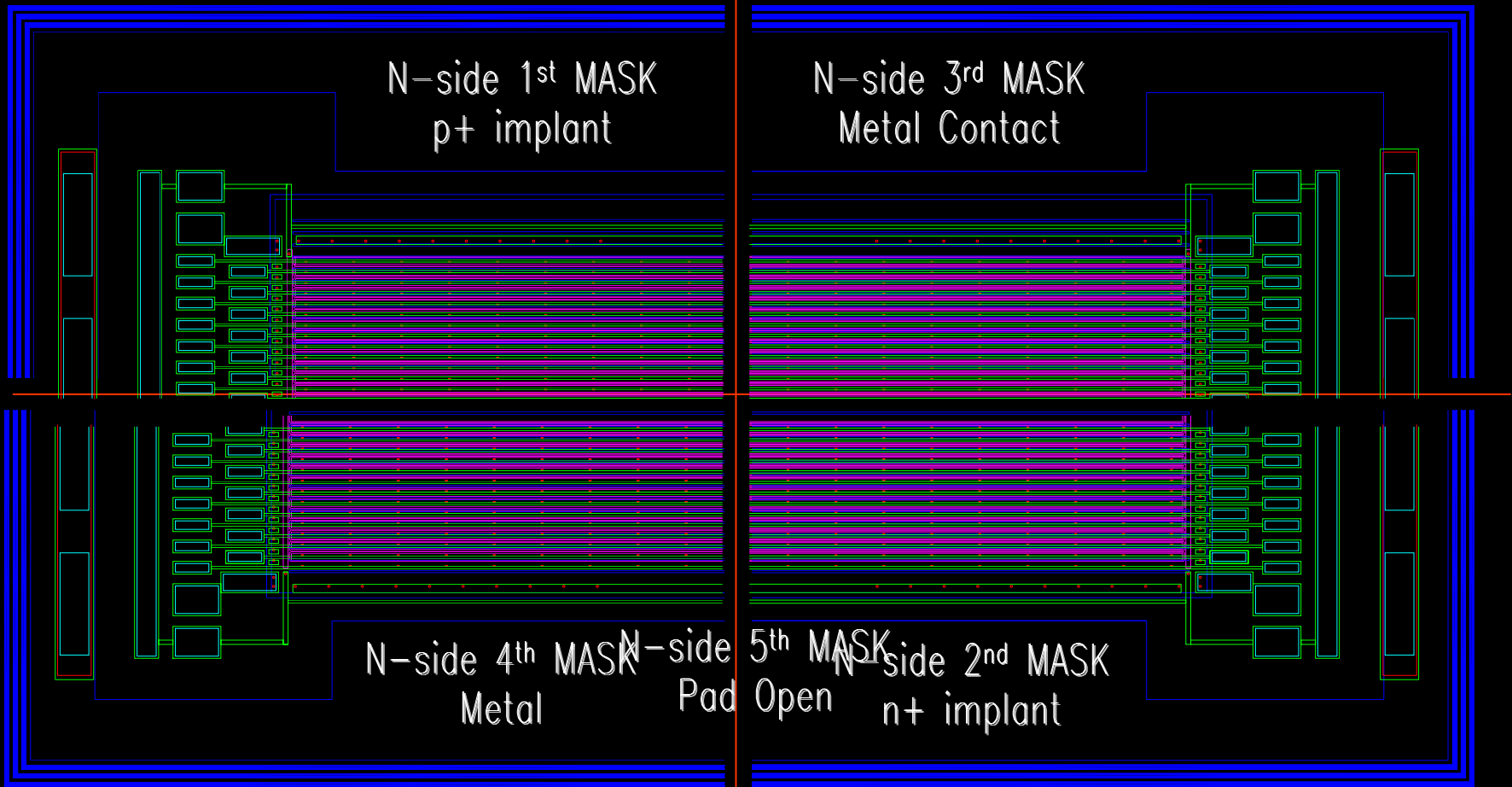
2004-04-20



Silicon Strip Sensor Simulation

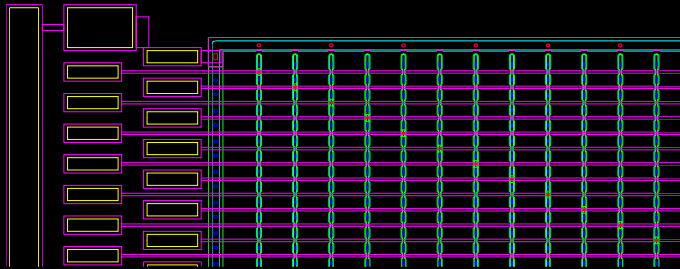


MASK for n+ side

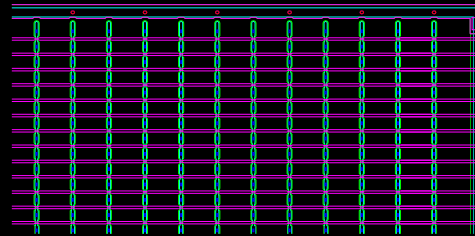


MASK for p+ side

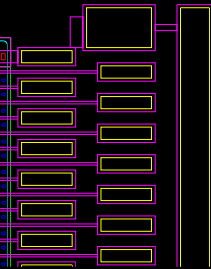
P-side 1st MASK
p+ implant



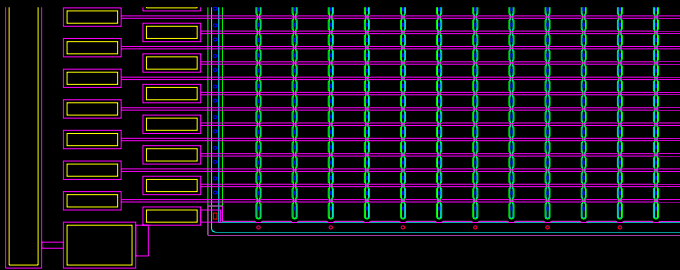
P-side 2nd MASK
Metal contact



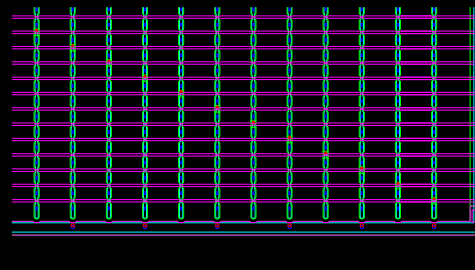
P-side 3rd MASK
1st Metal



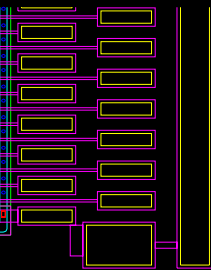
P-side 5th MASK
2nd Metal



P-side 4th MASK
VIA contact



P-side 6th MASK
Pad open

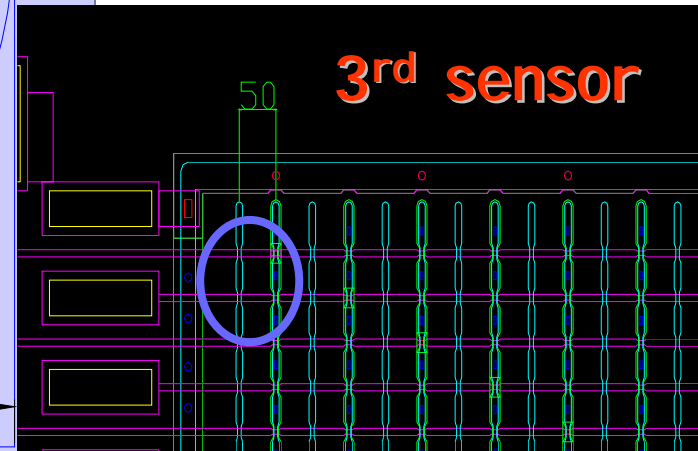
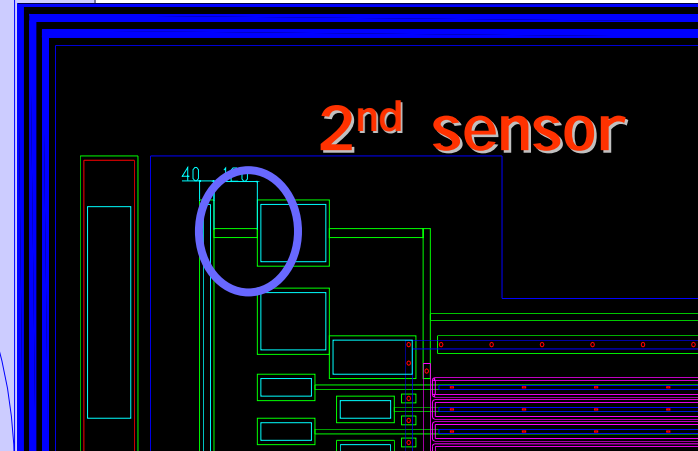
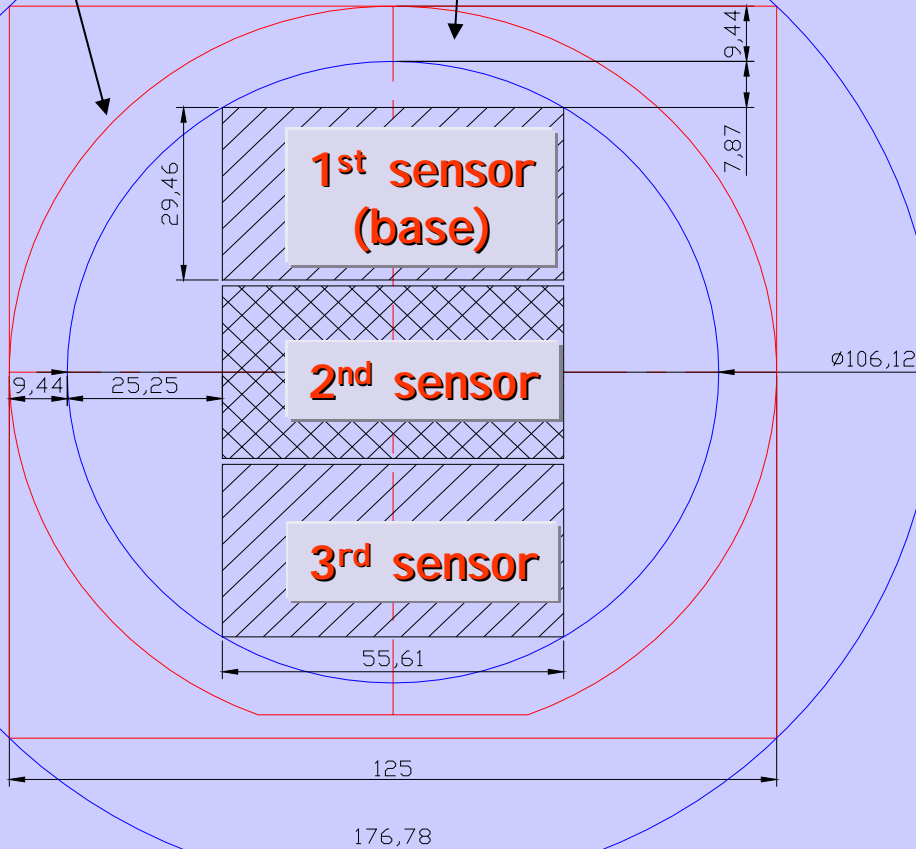


Silicon Strip Sensor Types

allowance for handling in fab.

6 inch mask

5 inch wafer



Silicon Strip Sensor Prototype

n+ implanted

p-stop in atoll

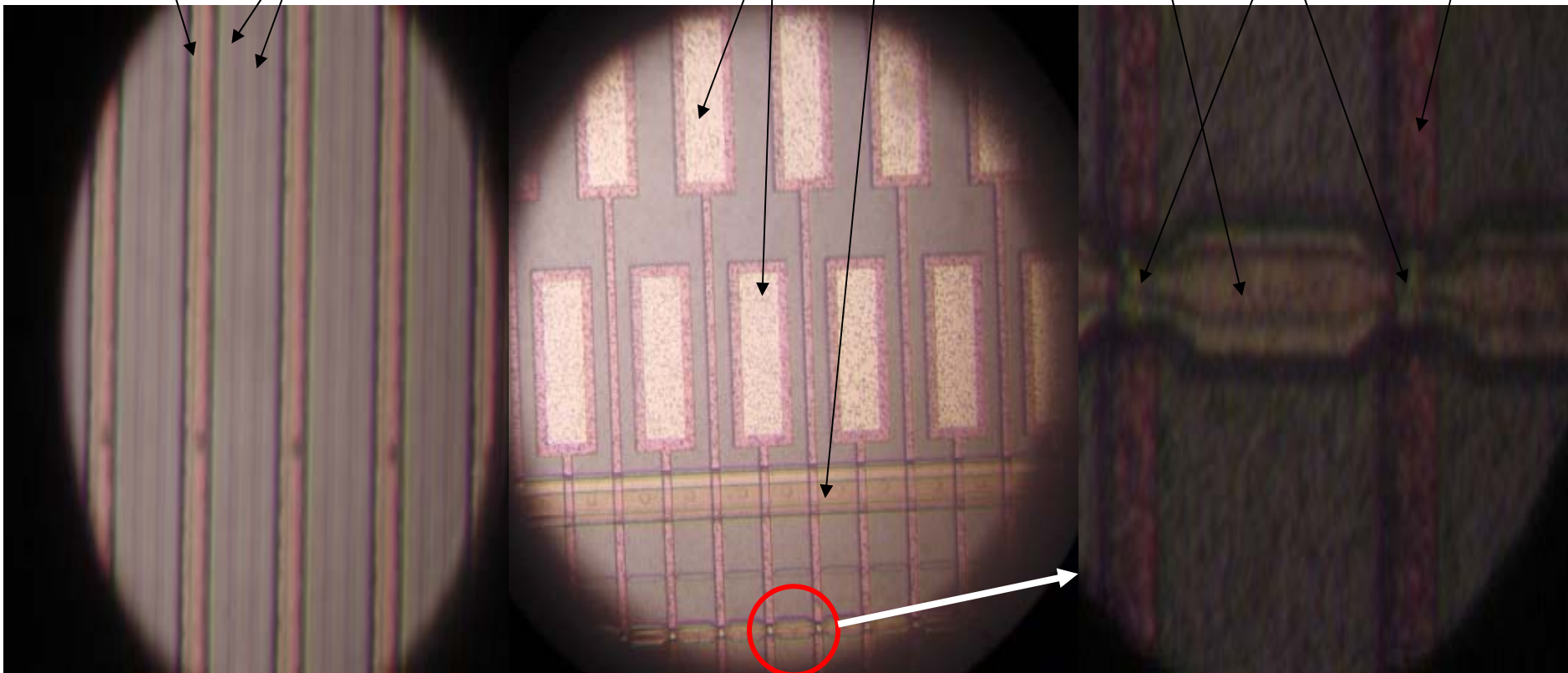
readout pad in staggering

guard ring

p+ implanted

readout strip

via in hourglass



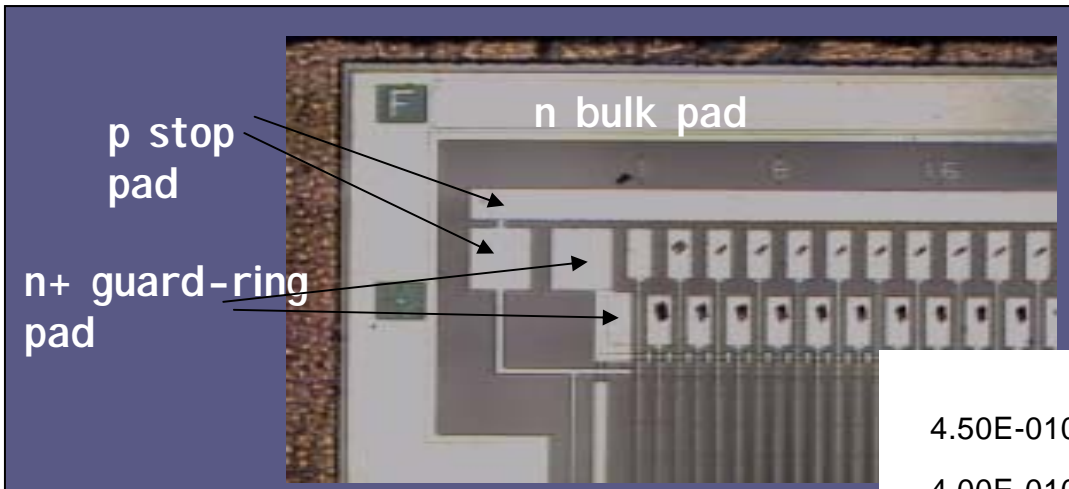
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N+ side

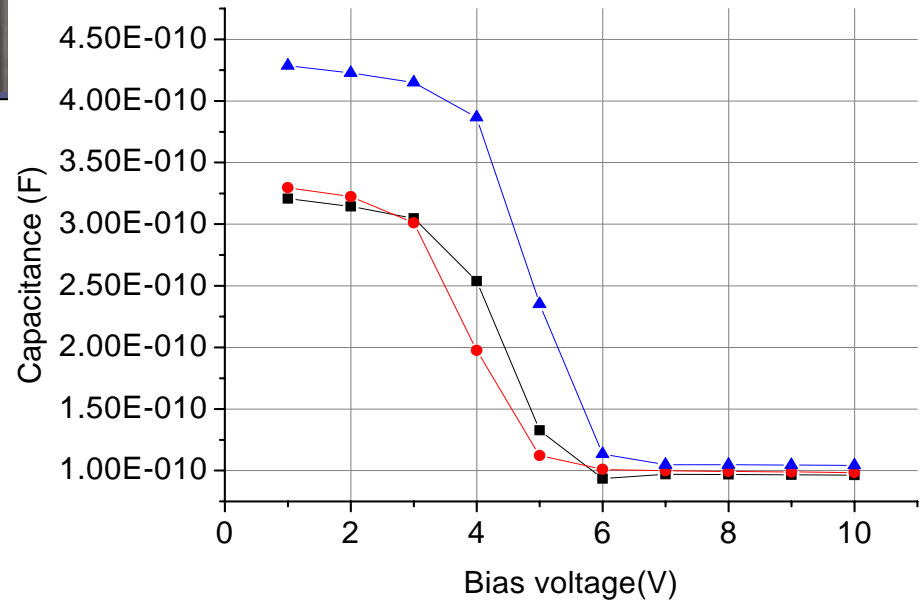
LCWS04

P+ side

N-side measurement

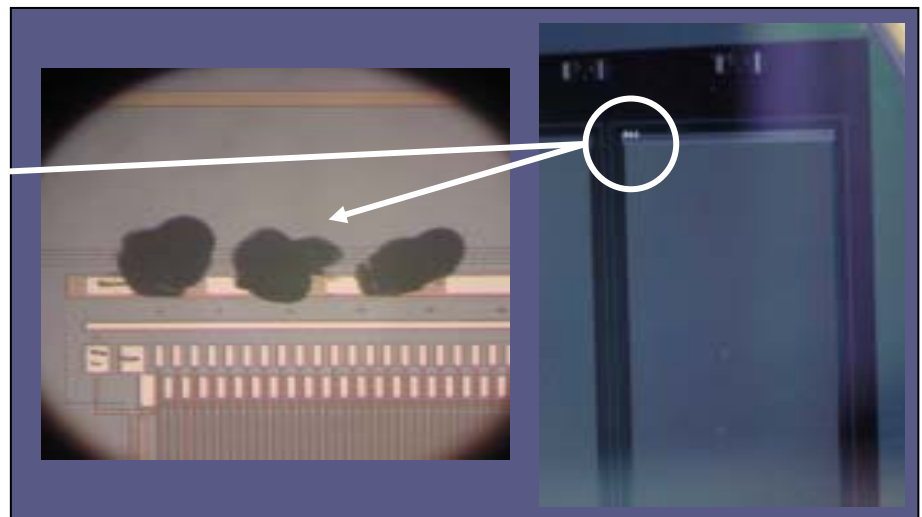
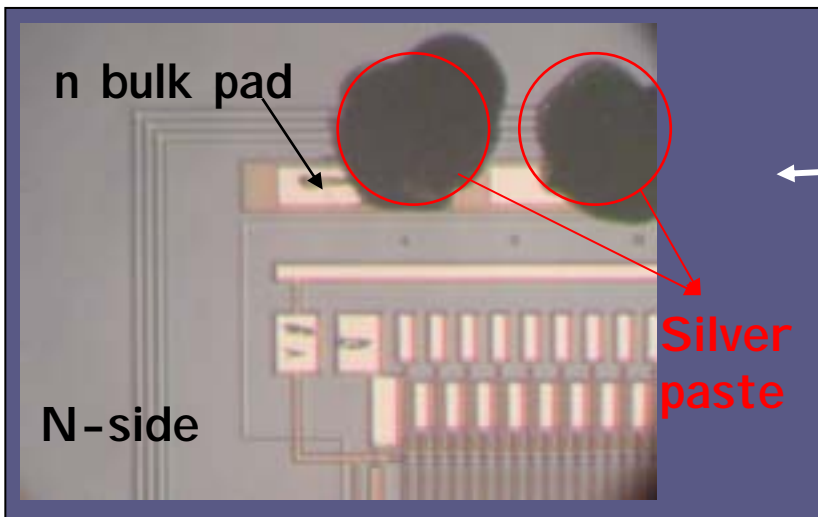
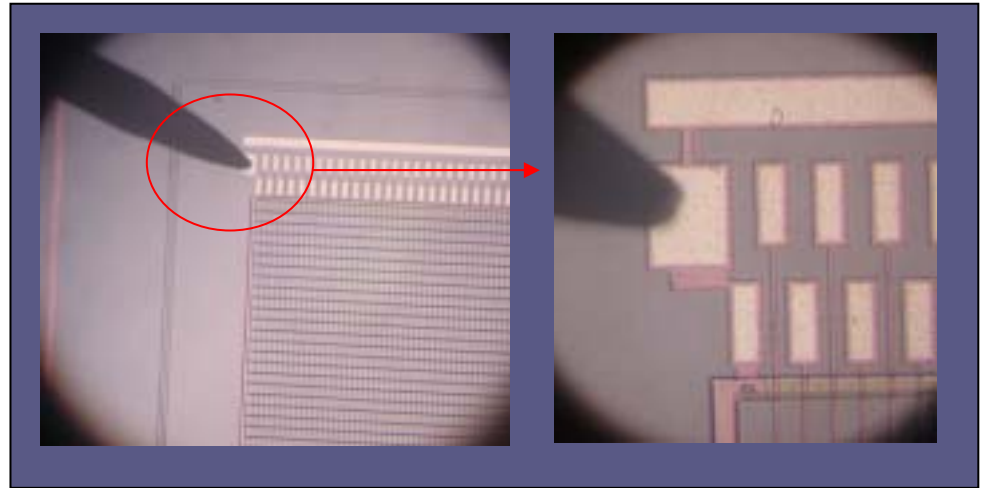
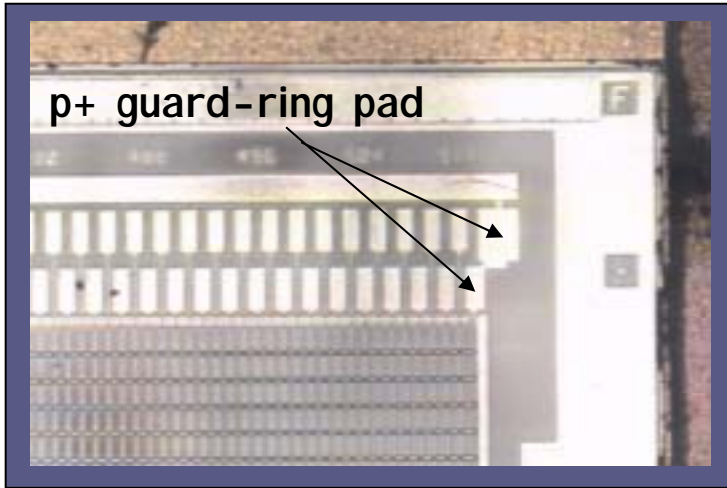


probe
n+ guardring/n+strip
&
p-stop.

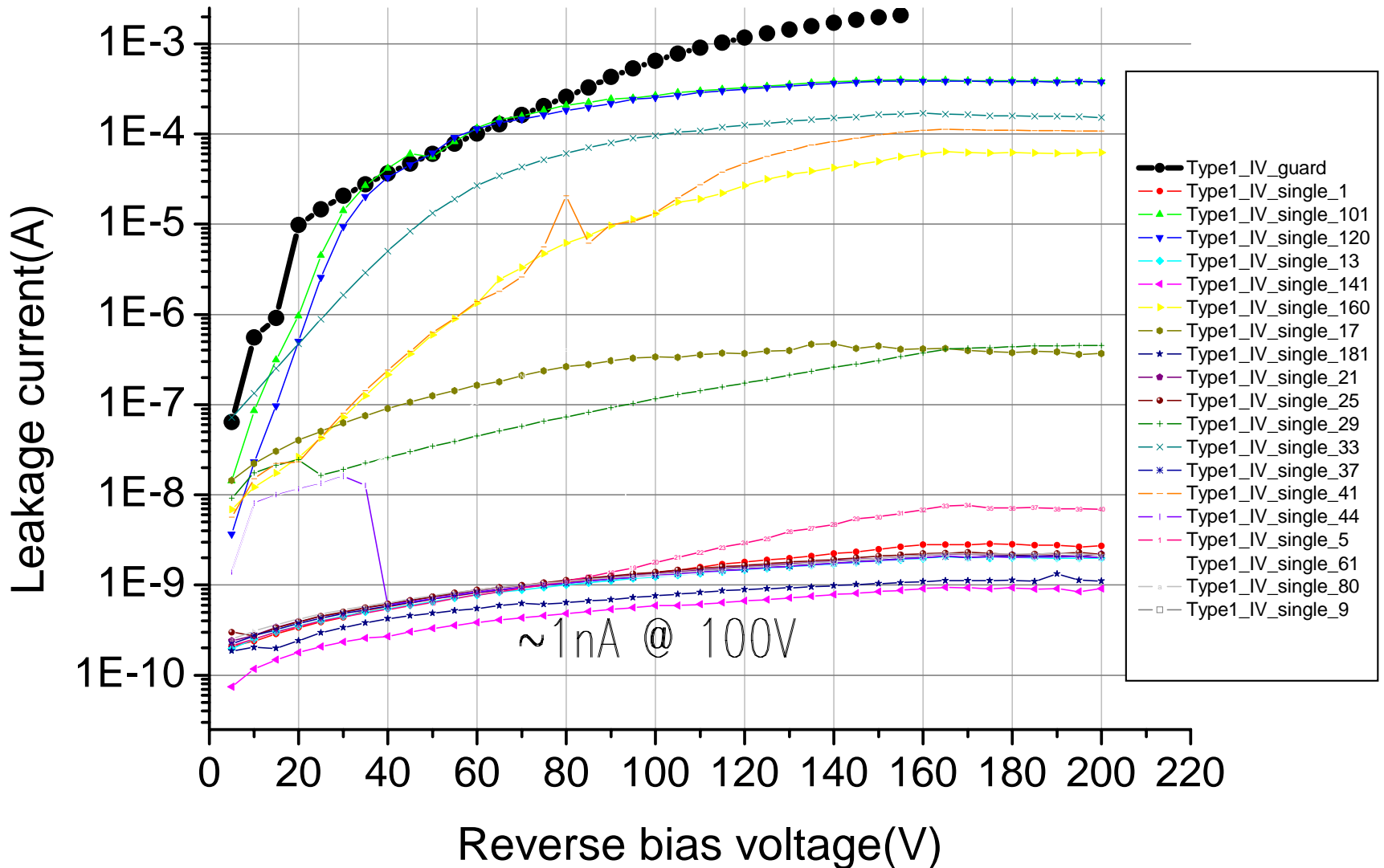


P-side measurement

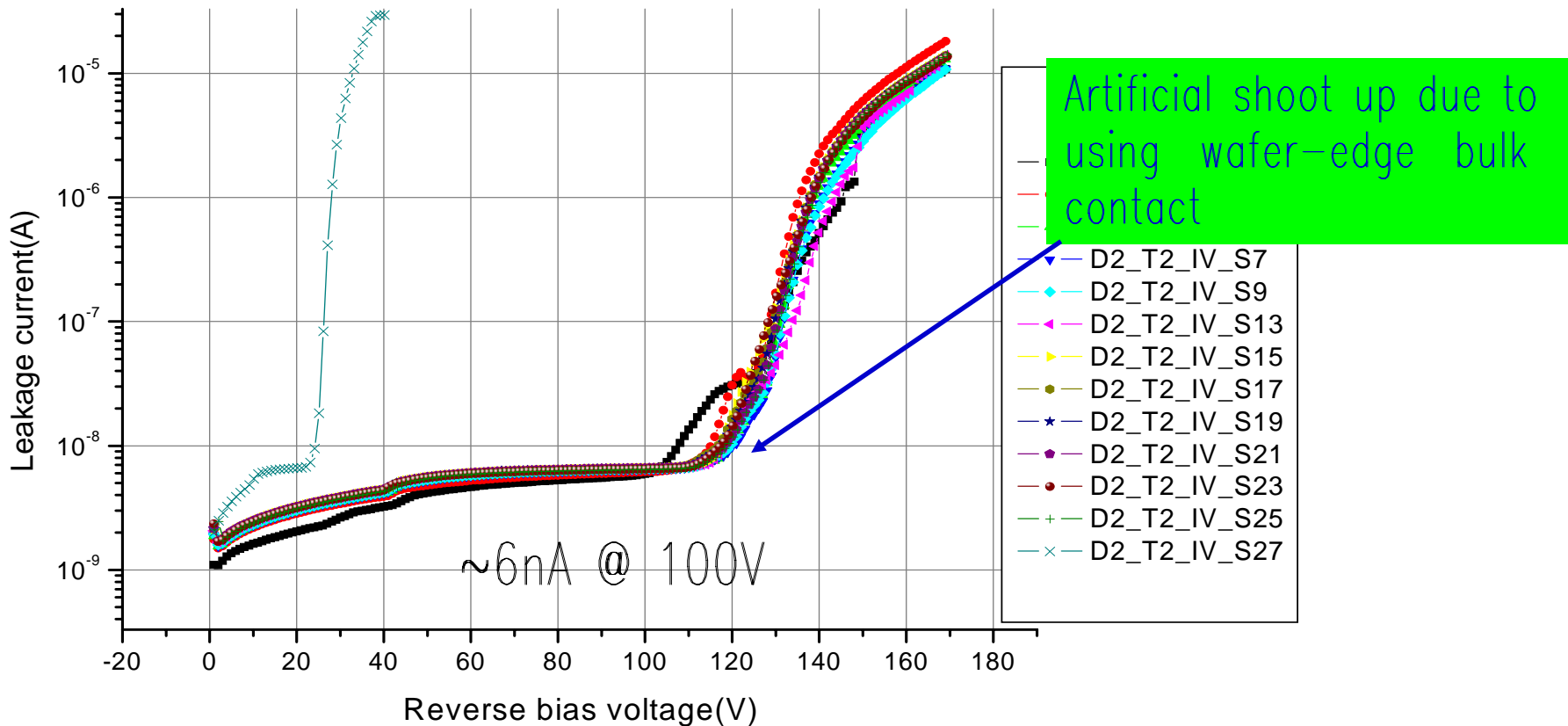
probe
n bulk pad(+) on n-side
&
p-guardring(ground) / p-strips



single p-strip IV (1st Run)



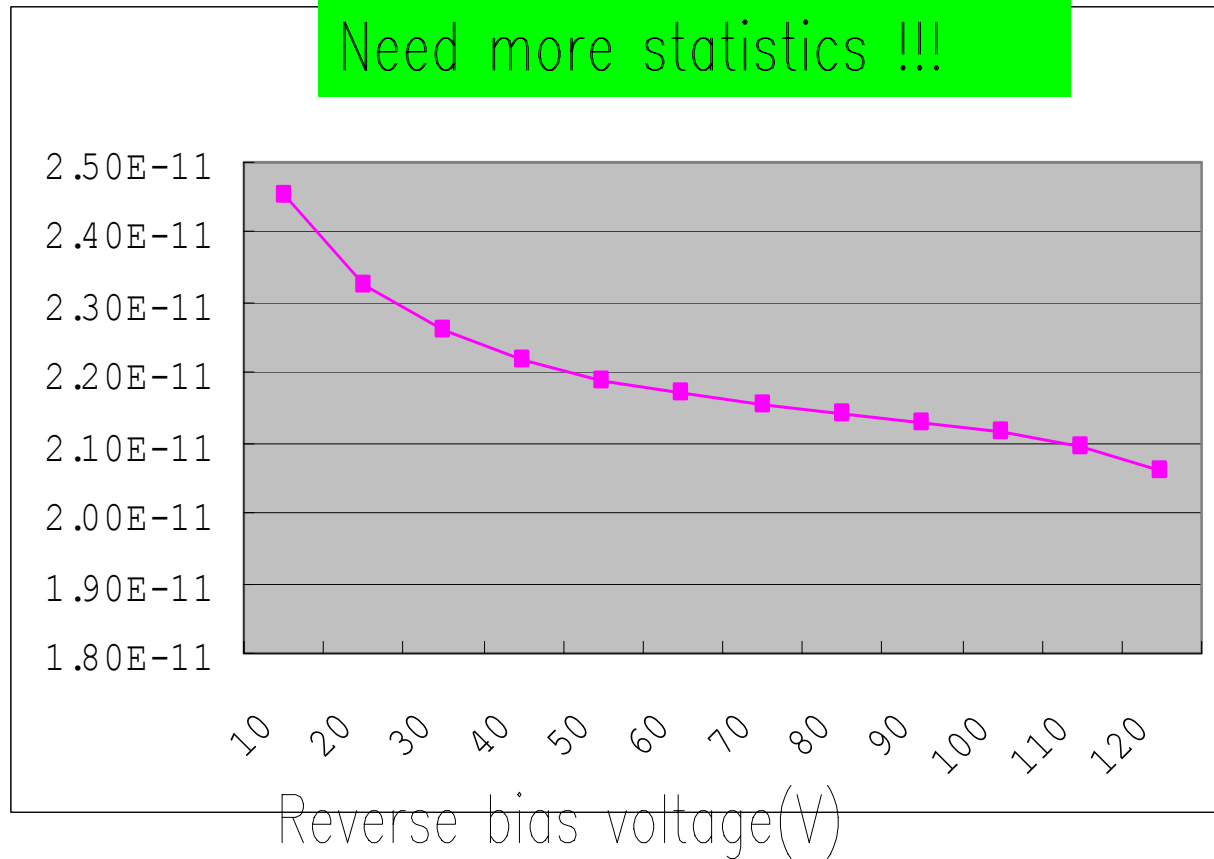
single p-strip IV (2nd Run)



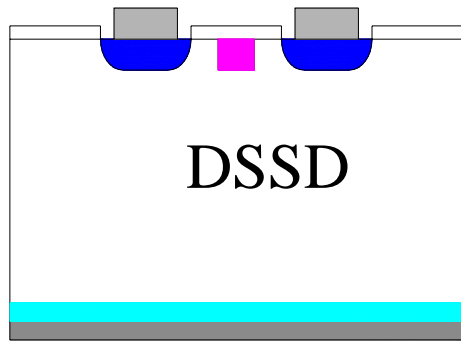
Strip leakage current $\sim 6\text{nA}$ (increased by $\sim 5\text{nA}$ compared to 1st run) as expected due to deep drive-I n of n & p junctions

single p-strip CV (1st Run)

CaPacitance (F)



Schematics of Readout and DAQ for DSSD



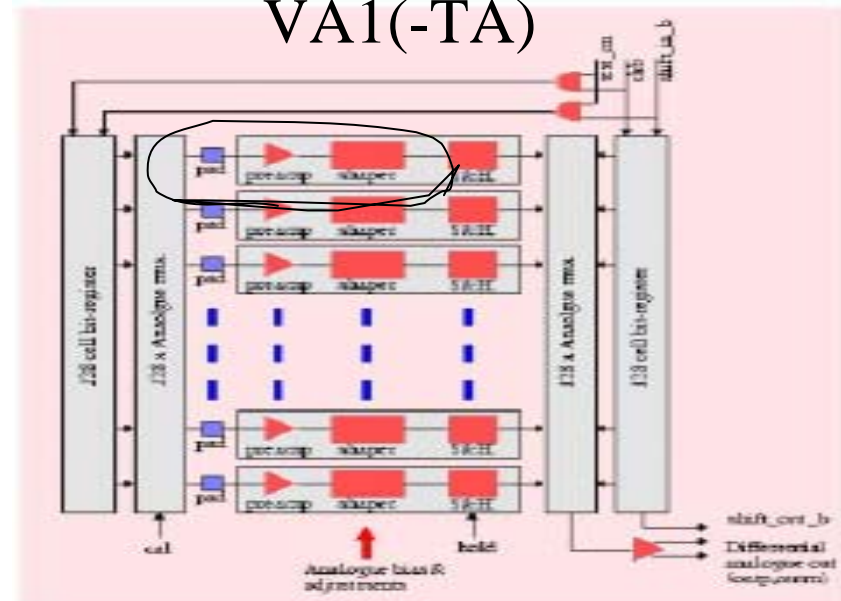
Flex cable

RC chip



HV

VA1(-TA)



Control Signal

FPGA

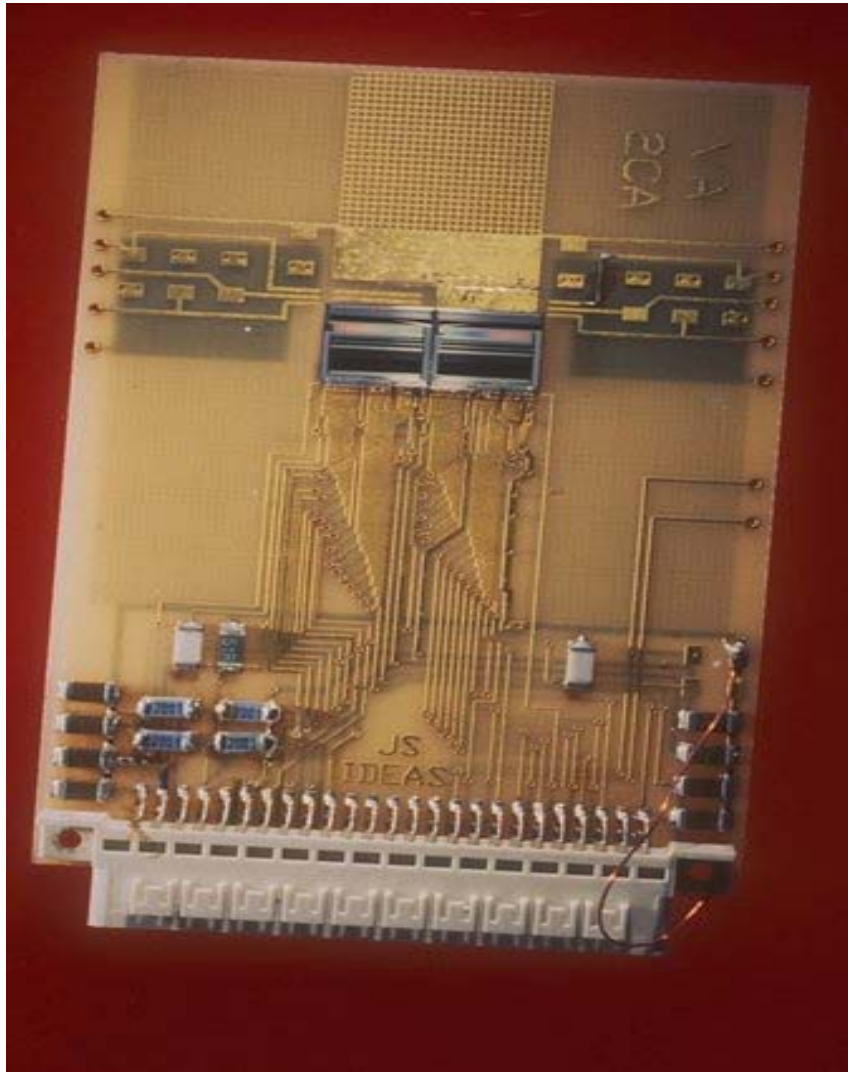
FADC

USB2
DAQ

Status and Plan for Readout and DAQ

- Flex cable to be designed and produced (size and line definition to be determined)
- RC chips (8) in hand
- VA1 chips (10) and VA-CA test board purchased (VA1-CA test and VA1 chip wire bonding necessary, and VA-TA chip to be purchased)
- FADC (25 MHz)+USB2 board and DAQ ready (need a FPGA program to operate VA chip)
- Hybrid board (RC+VA+FADC+USB2) to be designed

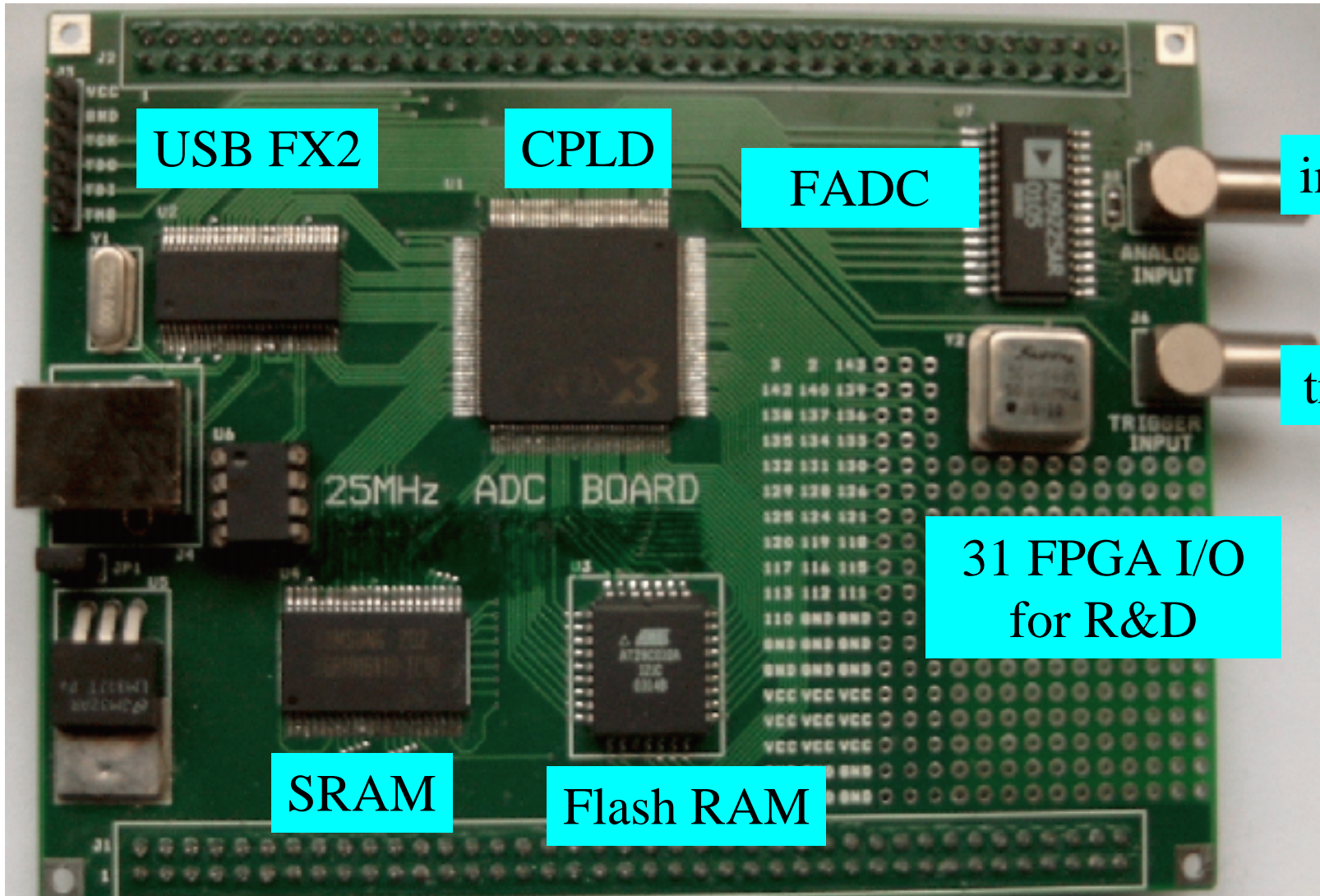
VA-CA test board



Pin	Signal	Pin	Signal
1	gnd	2	gnd
3	n.c.	4	gnd
5	outm	6	gnd
7	gnd	8	outp
9	Avss	10	gnd
11	Cal	12	Avss
13	Vfs	14	Pre_bias
15	Vfp	16	Sha_bias
17	Vref	18	Ibuf
19	Avdd	20	avdd
21	Cal_r	22	Gnd
23	Vdd_r	24	n.c.
25	Vss_r	26	n.c.
27	Gnd_r	28	n.c.
29	Vfp_r	30	n.c.
31	Extra1	32	Extra2
33	Vdd	34	Gnd
35	Holdb	36	Shift_out
37	Mon10/bi11	38	Ck
39	Dreset	40	Dresetb
41	Shift_inb	42	n.c.
43	Ckb	44	Hold
45	Teston	46	Vss (del_on)
47	Dvdd	48	Dvss
49	Dvdd	50	Dvss

The pin assignment list for the 'Standard VA interface' used by the VA2CA evaluation board.

FADC+USB2



USB FX2

CPLD

FADC

input

trigger

31 FPGA I/O
for R&D

SRAM

Flash RAM

Summary and Plan for Silicon Strip R&D

- 1st & 2nd runs of prototype fabrication were done
 - manual measurement in progress (pain stacking!)
- 3rd run being splitted (April) with feedback from test measurements
 - 2 for same process as 1st & 2nd runs
 - 2 for spray implantation
 - 2 for double implantation

- automatic probe station & wirebonder purchased and installed
 - faster and more reliable measurement
- probe card design in progress
- design revision will be needed
- test patterns should be added
- simulation in progress
- readout & DAQ design and production in progress

Stay Tuned !