Processing of ultra-thin silicon sensors for future e^+e^- linear colliders

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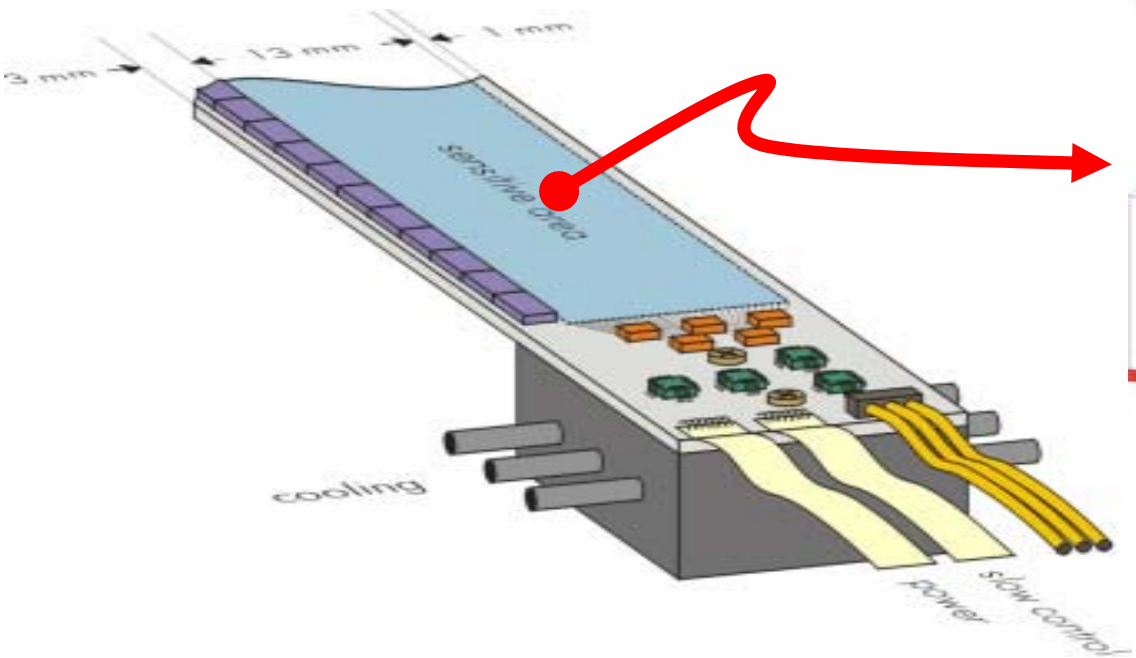
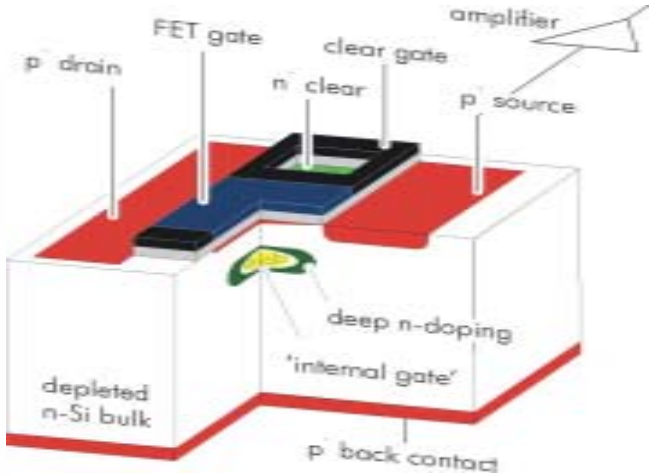
- **Module Concept**
- **Thinning Technology**
- **PiN Diodes on thin Silicon**
- **Summary and Outlook**

Module Concept

sensitive area thinned to 50 μm, supported by a 300 μm thick frame of silicon



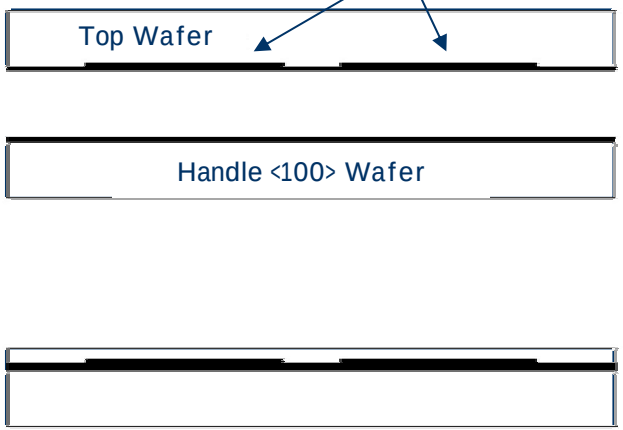


Depleted Field Effect Transistor

fully depleted & electrically active back side → non-standard thinning technology needed

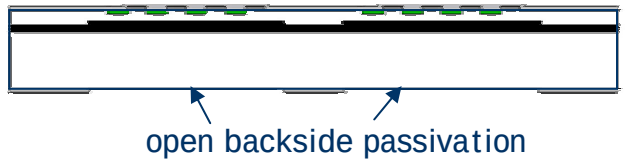
Processing thin detectors
- the Idea -

a) oxidation and back side implant of top wafer

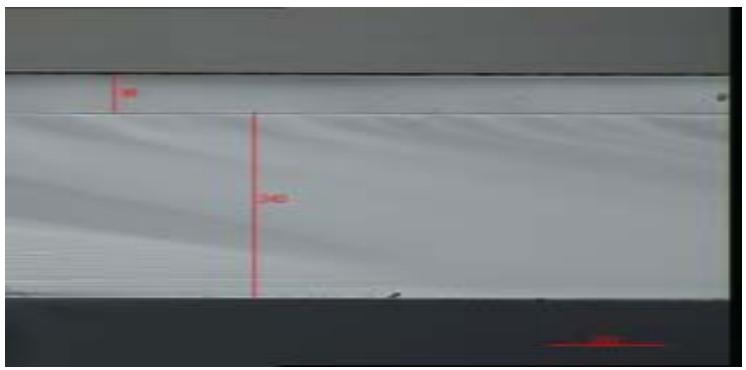


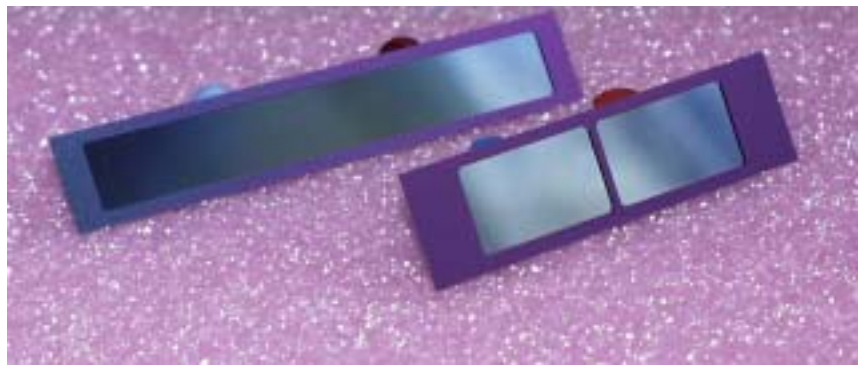
b) wafer bonding and grinding/polishing of top wafer

c) process ➔ passivation



d) anisotropic deep etching opens "windows" in handle wafer



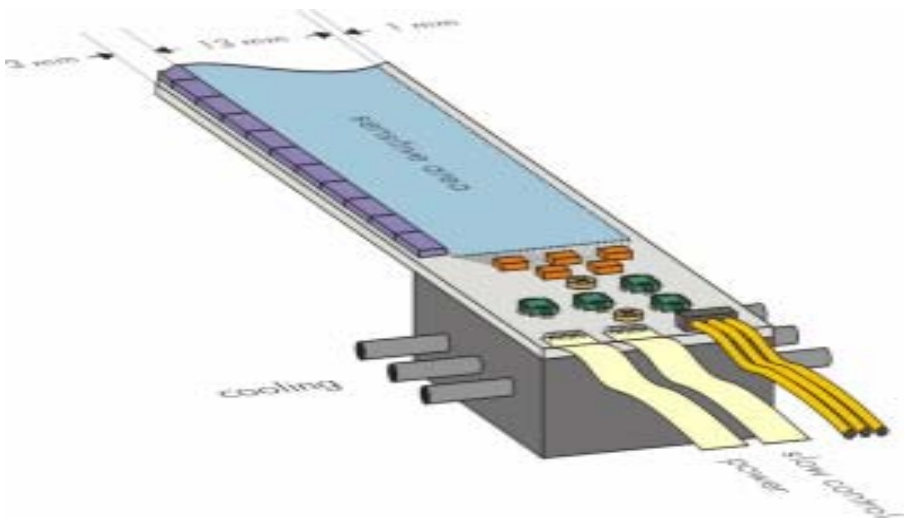


Module Concept
- Material Budget -

Estimated Material Budget (1st layer):

Pixel area: 100x13 mm², 50 µm : 0.05% X_0
steer. chips: 100x2 mm², 50 µm : 0.008% X_0
(massive) frame :100x4 mm², 300 µm : 0.09% X_0

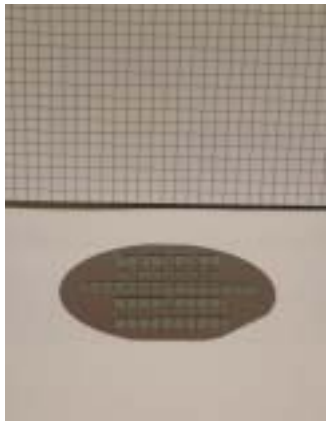
reduce frame material!!!
→ "support grid"



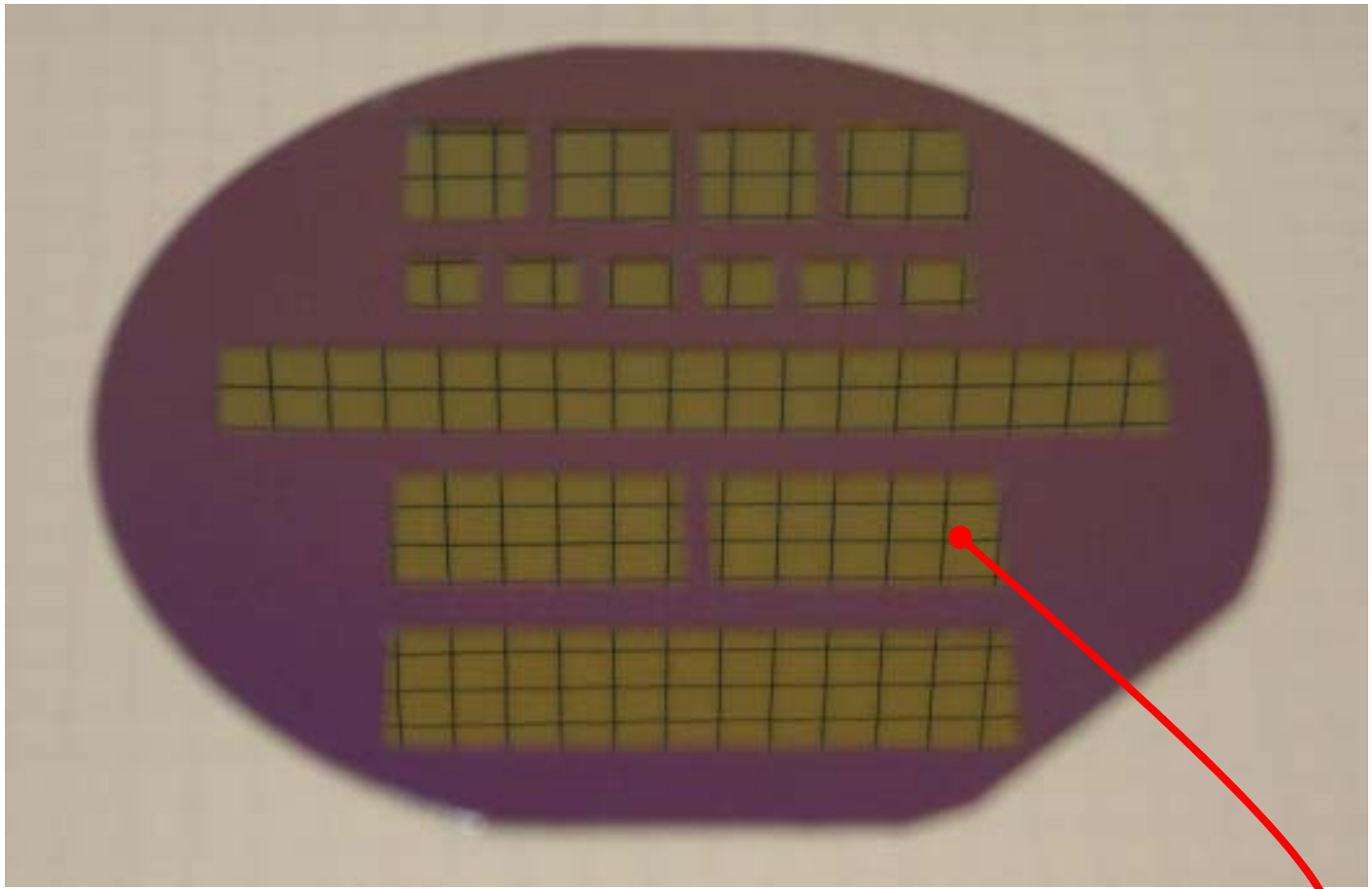
perforated frame: 0.05 % X_0

total: 0.11 % X_0

Mechanical Dummies

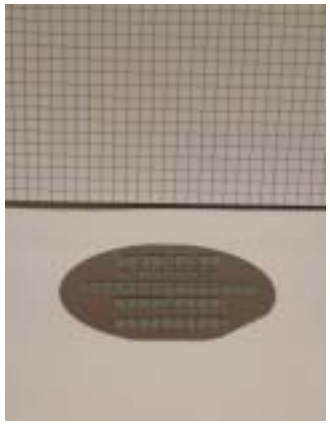


the mirror image of a 5mm grid…



polished back side of a **40 µm** thin top wafer after deep etching with TMAH

Mechanical Dummies



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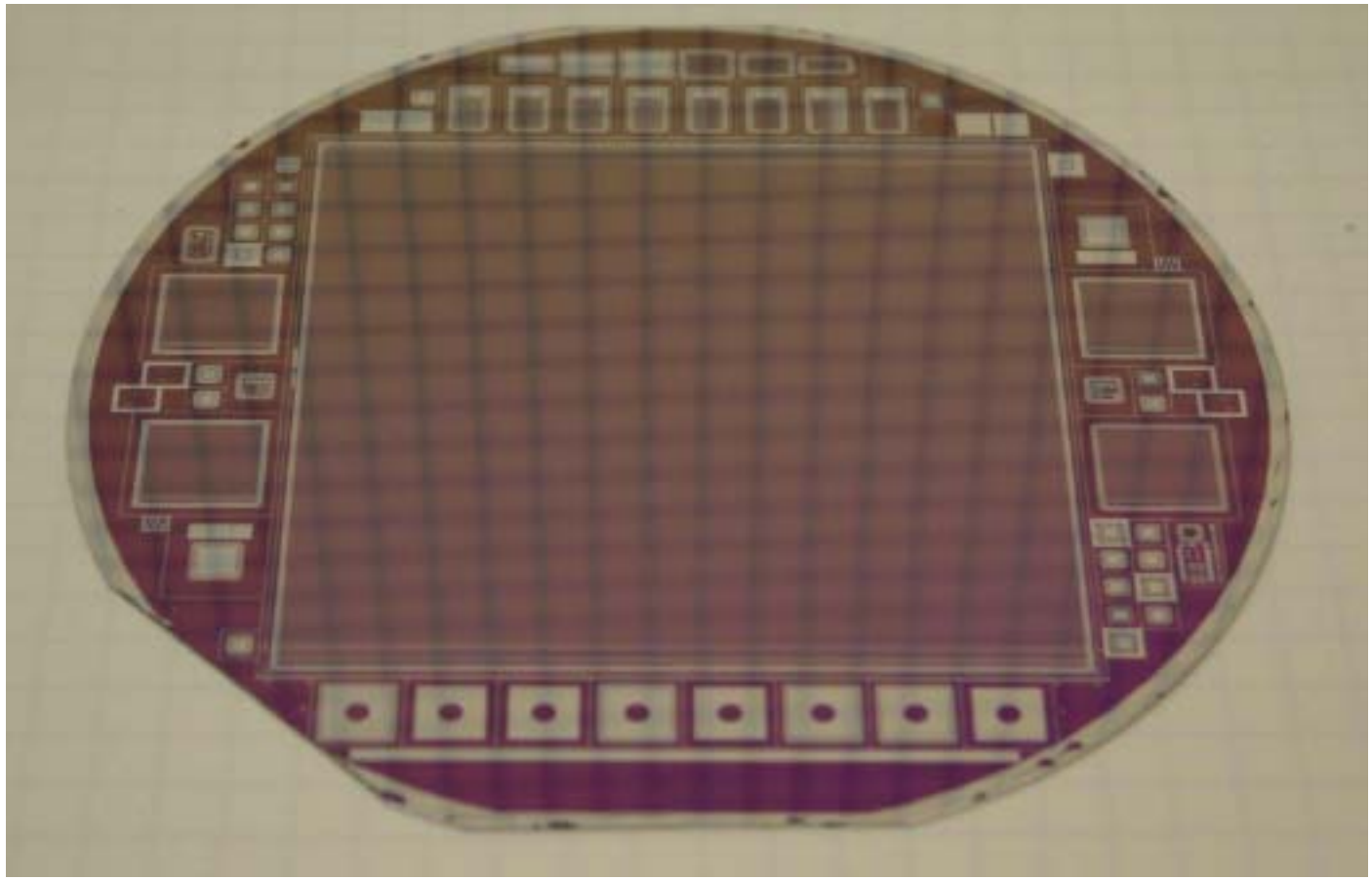
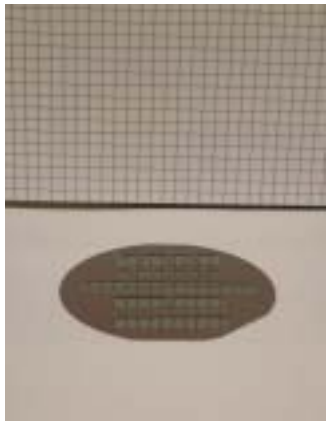


40 µm top wafer side: patterned aluminum layer (ATLAS strip detector prototype mask)

Mechanical Dummies



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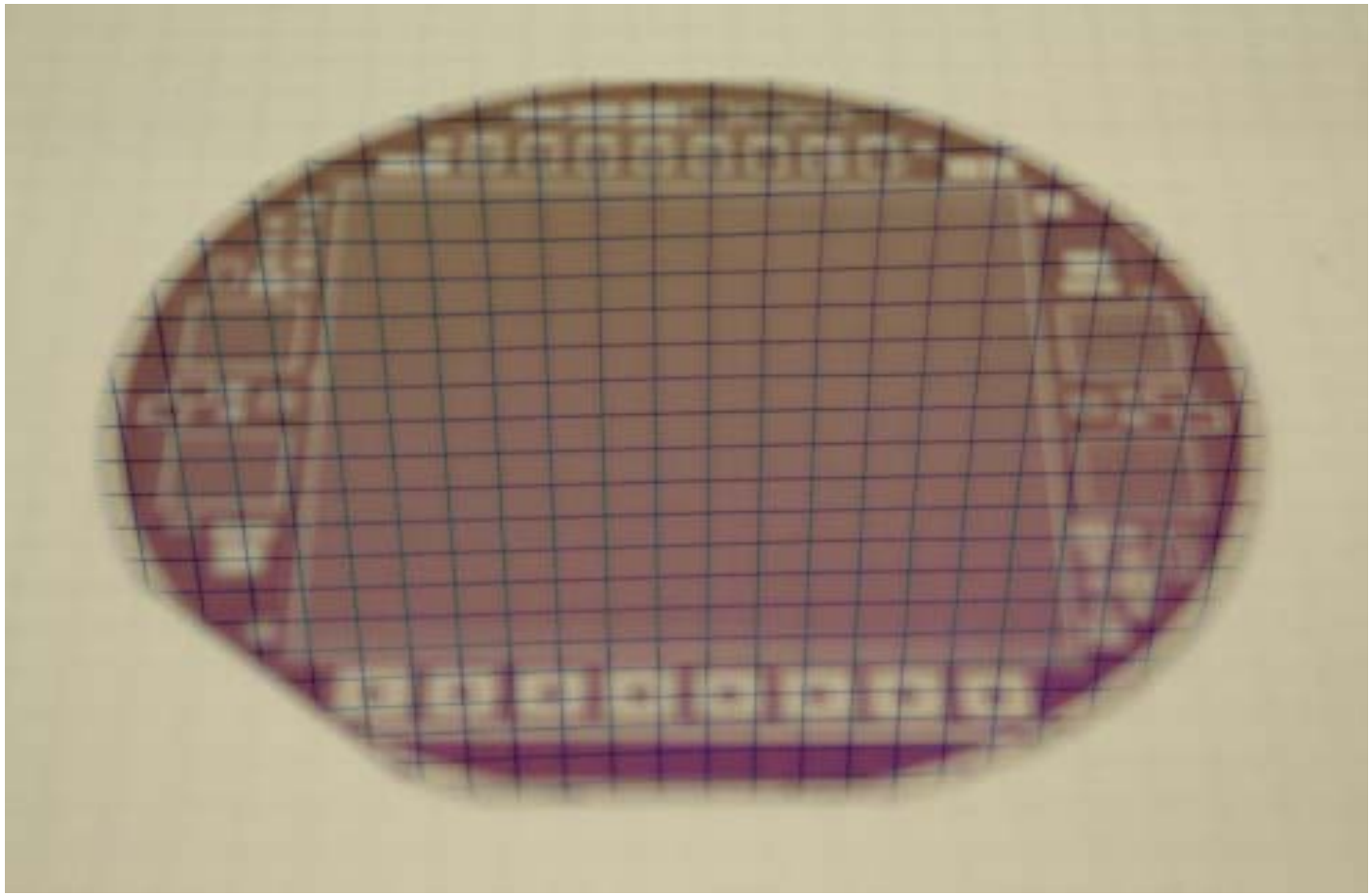
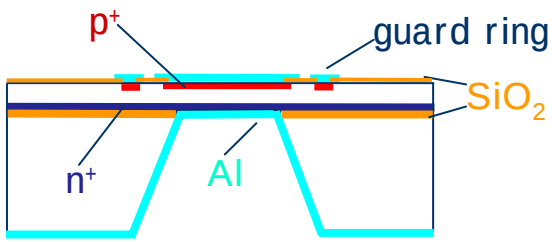


focus on the mirror image: **no distortions visible, even after single sided metallization!!**

PiN Diodes on thin Silicon

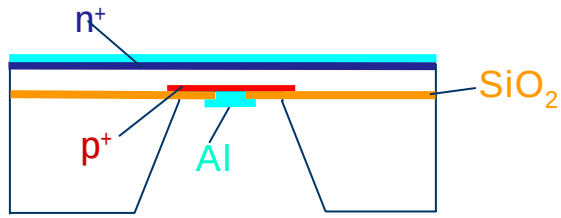
2 types of thinned diodes

Type I: Simplified standard technology



structured p+ on top
unstructured n+ in bond region

Type II: Implants like DEPFET config.

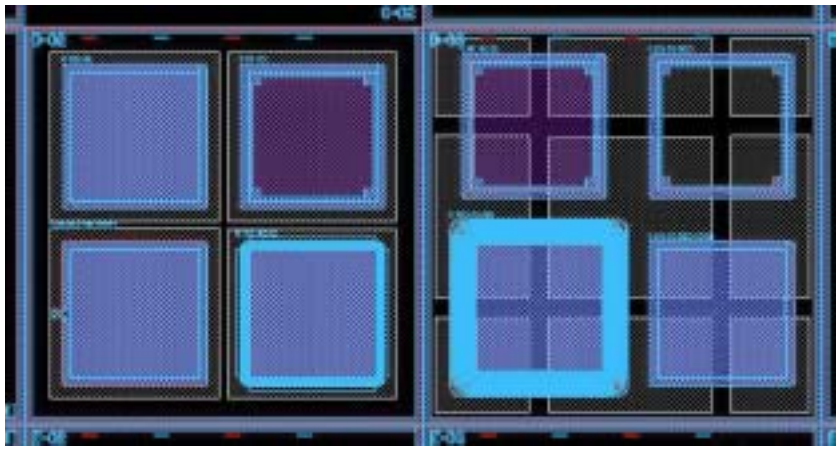


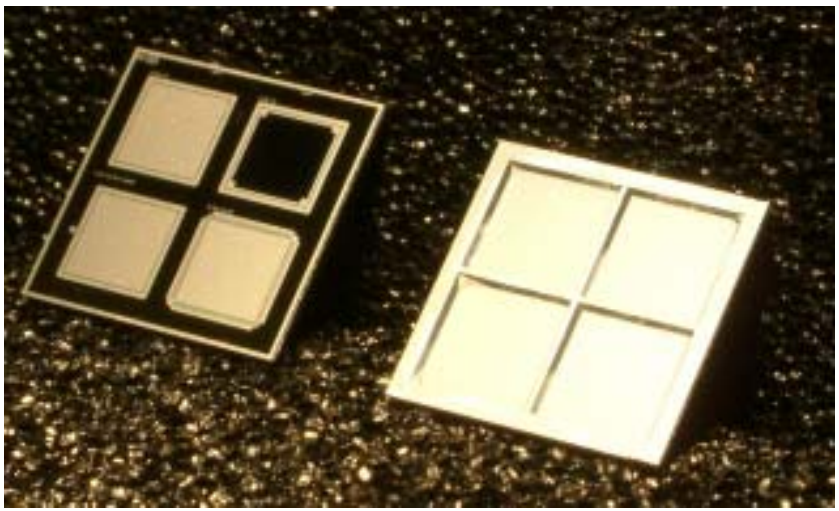
unstructured n+ on top
structured p+ in bond region

** + 4 Wafers with standard Diodes as a reference **

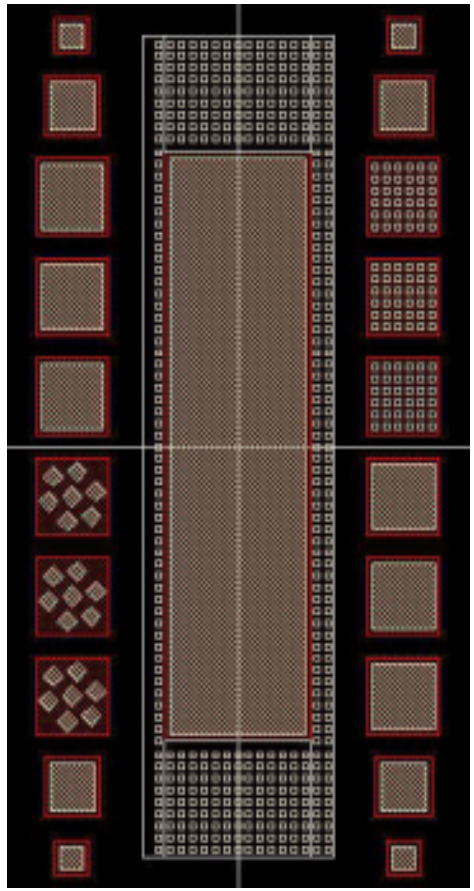
PiN Diodes on thin Silicon

Type I: pn-junction on top wafer surface



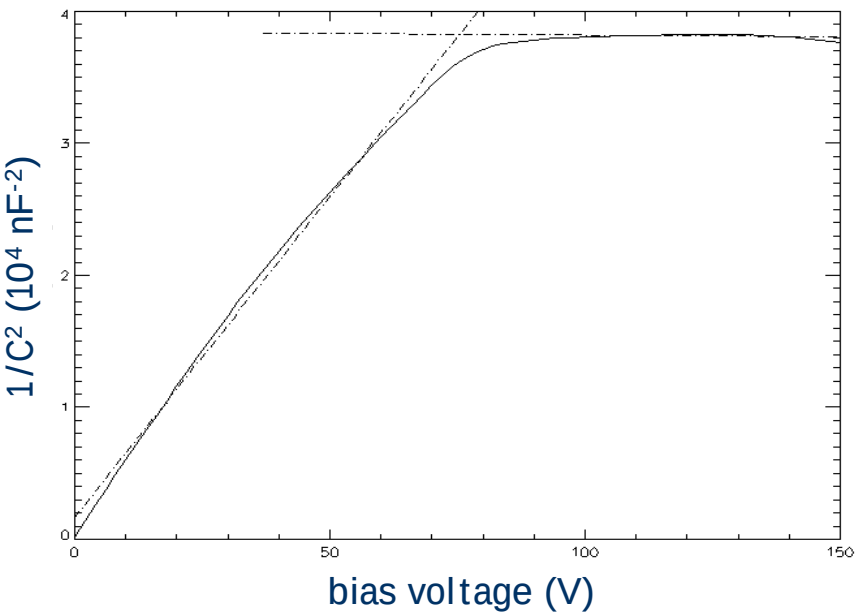


Type II: pn-junction in bond region

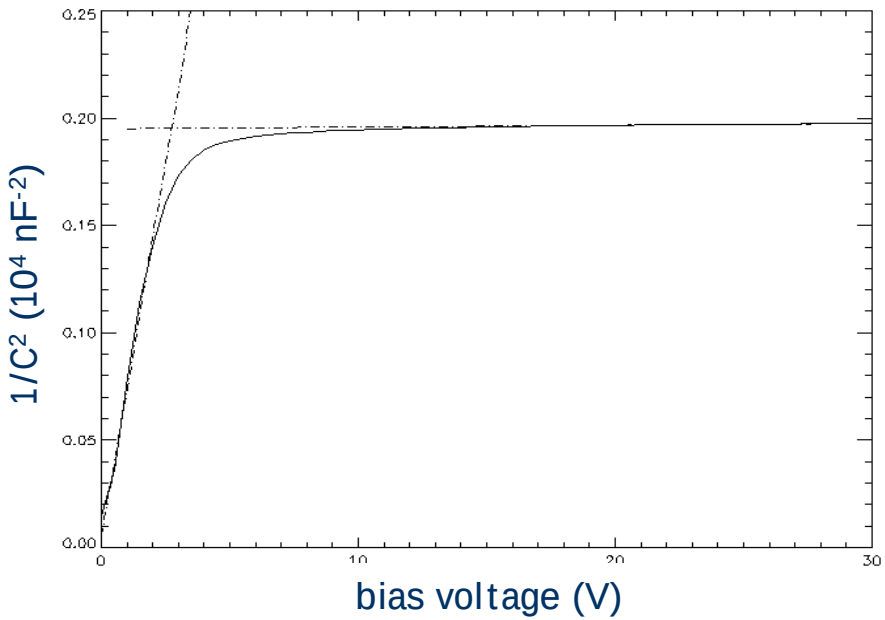


PiN Diodes on thin Silicon
- Type I: CV curves, full depletion voltage -

250 µm, type I diode, 10 mm²



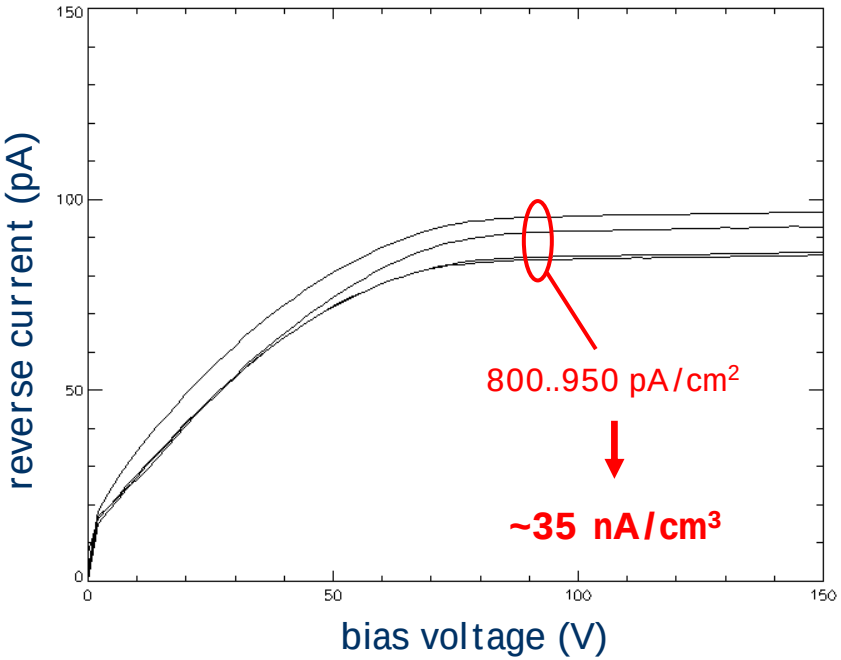
50 µm, type I diode, 10 mm²



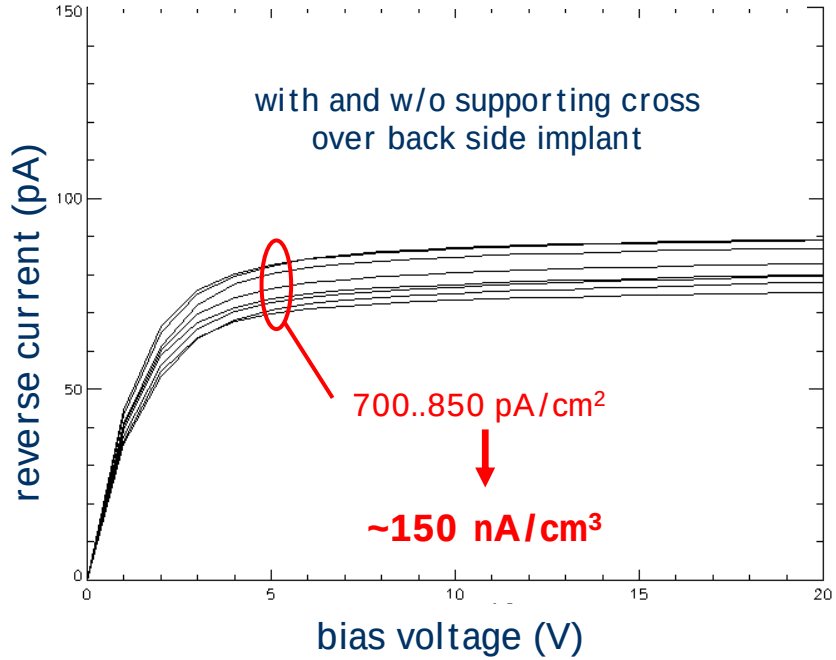
C(30V) ➔ t = 47 µm

PiN Diodes on thin Silicon
- Type I: IV curves -

250 µm, 4 type I diodes, 10 mm²



50 µm, 8 type I diodes, 10 mm²

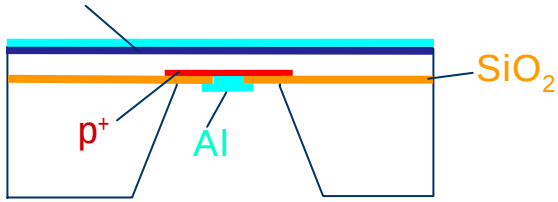


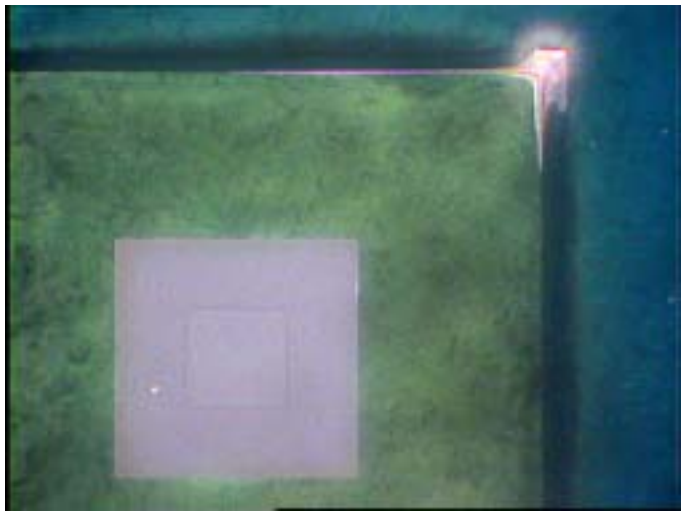
module in the first layer at TESLA: 13 cm²

→ **reverse current for the entire thin pixel array would be only 11nA at full depletion!!!**

PiN Diodes on thin Silicon
- Type II: IV curves -

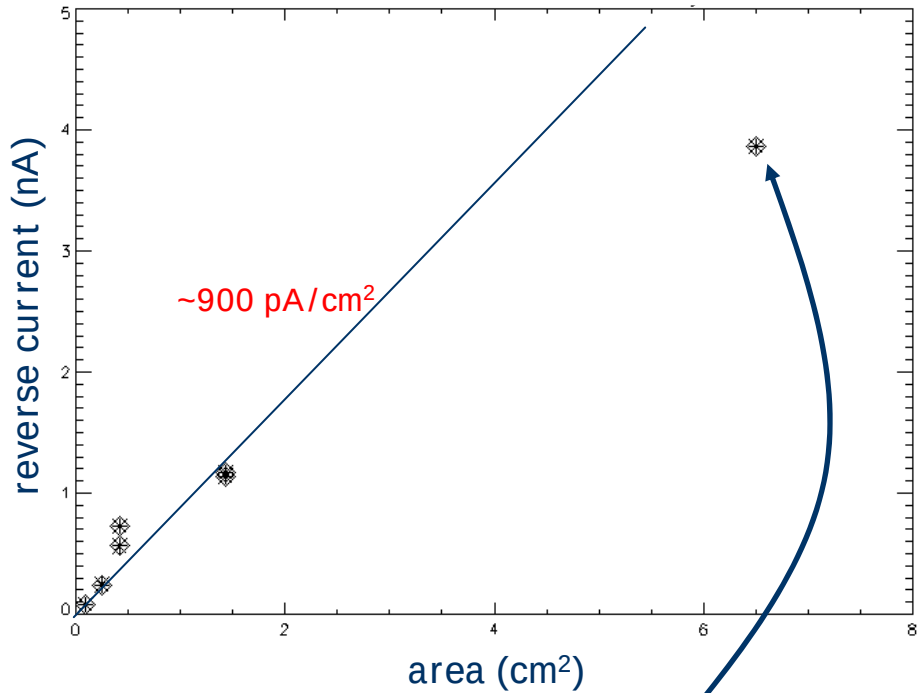
Type II: Implants like DEPFET config.





contact opening and metallization after etching of the handle wafer

Diodes of various sizes: 0.09 cm² – 6.5 cm²
surface generated edge current included
reverse currents at 5 V bias



➔ about 4 nA @ 5V for the 6.5 cm² diode, including edge generated current

Summary and Outlook

A thinning technology based on wafer bonding and etch back for **radiation sensors with implanted and structured back side (DEPFETs)** was presented.

The sensitive pixel area is thinned to **50 µm** and supported by an **integrated silicon frame**.

The feasibility of the thinning technology was shown:

- **Direct wafer bonding** after lithography and implantation is **possible.**
- **TMAH** deep etching does not deteriorate the devices on the top wafer.
- **Handling** of etched wafers and diced thin chips is **safe and easy.**

IV/CV measurements of **diodes on thin silicon** are **extremely encouraging:**
reverse current < 1 nA/cm² for large area PiN diodes, including edge generated current.

Next steps:

1. Material optimization (Simulation):
   What is the effect of the inhomogeneous material distribution on the impact parameter resolution ?

2. Process optimization and integration in the full process sequence for DEPFET matrices.