Phase I pixel ROC

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Scope

- Phase II ROC needs new architecture (**not** just evolution of present chip)
- This new chip will not fit into phase I schedule
  - → Phase I ROC is closely related to present chip or even unchanged
  - → Phase I ROC will be in 0.25μm (don‘t see a reason why not)
- Partial overlap in time of phase II ROC R&D and potential phase I ROC evolution → impact on needed manpower

Limitations of present ROC

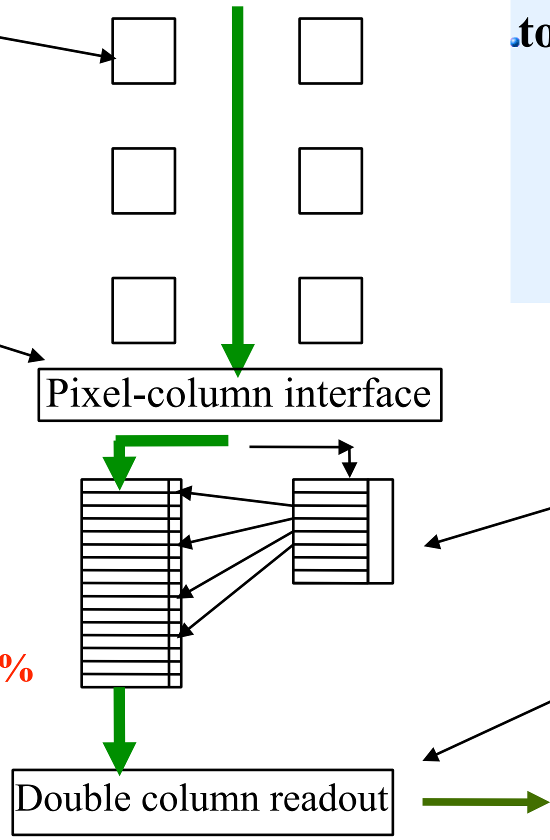
- Estimates on data loss based on:
  - High rate beam tests (pions at PSI)
  - Very high rate X-ray tests
  - Time domain simulations
- In short:
  - Buffer overflow dominates at $2 \cdot 10^{34}$
  - Next is readout losses caused by reseting column after readout
  - Rest is much smaller

Reminder: Data loss PSI46 @ $10^{34} cm^{-2} s^{-1}$ (LHC)

Pixel busy:
0.04% / **0.08%** / **0.21%**
pixel insensitiv until hit transferred to data buffer (column drain mechanism)

Double column busy:
0.004% / **0.02%** / **0.25%**
Column drain transfers hits from pixel to data buffer. Maximum 3 pending column drains requests accepted

Data Buffer full:
0.07% / **0.08%** / **0.17%**



total data loss @ 100kHz L1A:
- **0.8% @ 11cm**
- **1.2% @ 7cm**
- **3.8% @ 4cm**

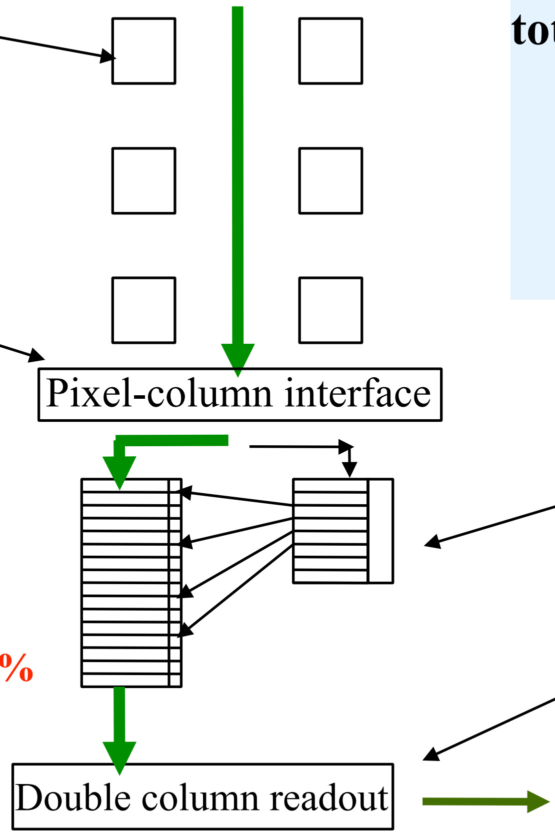
Timestamp Buffer full:
0 / **0.001%** / **0.17%**

Readout and double column reset:
0.7% / **1%** / **3.0%**
for 100kHz L1 trigger rate

Data loss PSI46 @ 2 x $10^{34}cm^{-2}s^{-1}$ (Phase I)

Pixel busy:
0.09% / 0.18% / 0.48%

Double column busy:
0.003% / 0.18% / 1.3%



Timestamp Buffer full:
0 / 0.05% / 6.8%

Data Buffer full:
0.09% / 0.17% / 0.83%

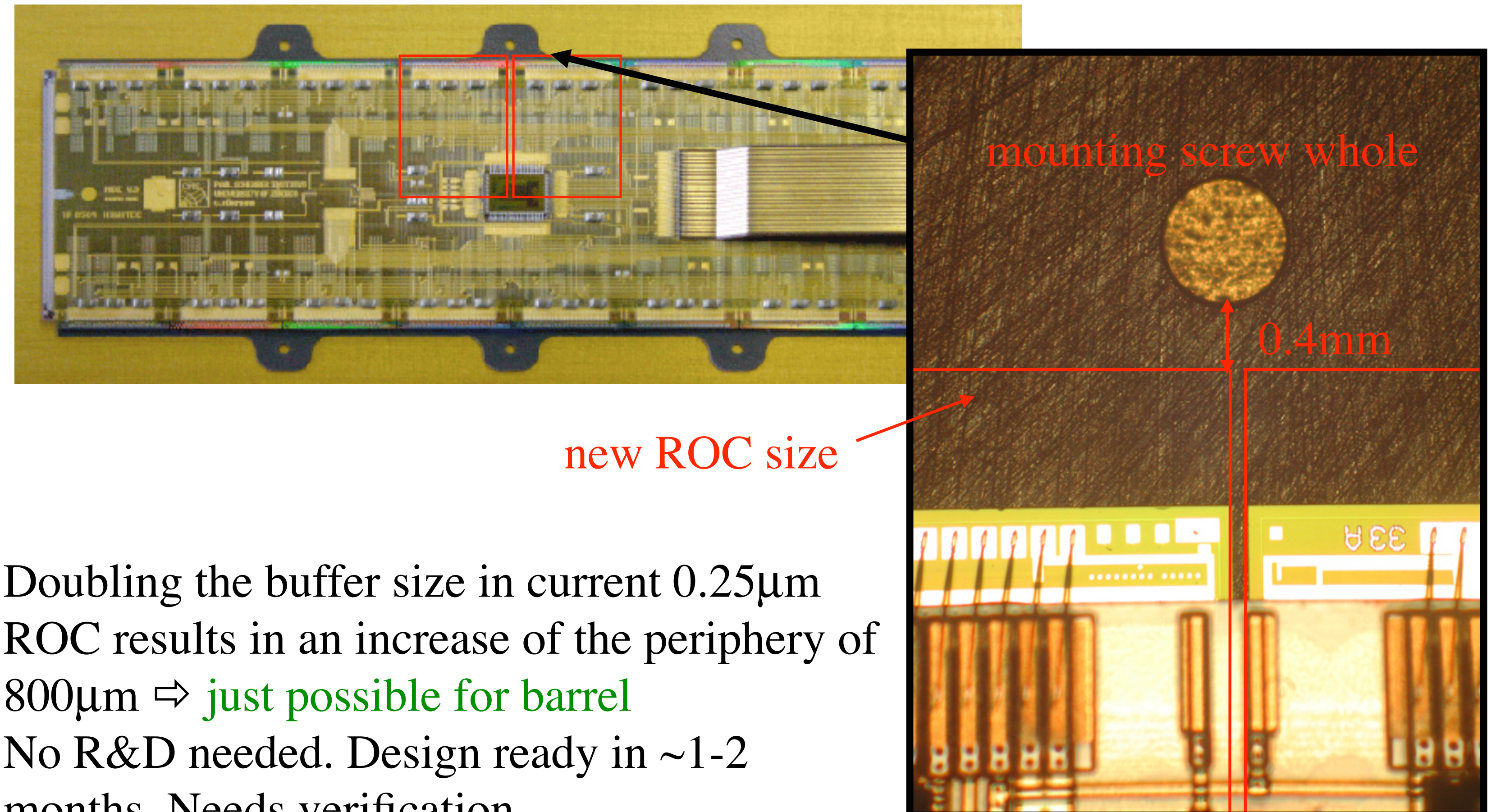
Readout and double column reset:
1.1% / 2.1% / 6.7%
for 100kHz L1 trigger rate

total data loss @ 100kHz L1A:
- **1.3% @ 11cm**
- **2.7% @ 7cm**
- **16% @ 4cm**

Doubling the buffer size

- Zero suppressed readout is data driven. Buffer sizes for timestamps and hit data depend not only on trigger latency, but also on track rates.
- Increasing the buffer sizes can compensate for this.
- Is it possible in 0.25um ?

Doubling the buffer size



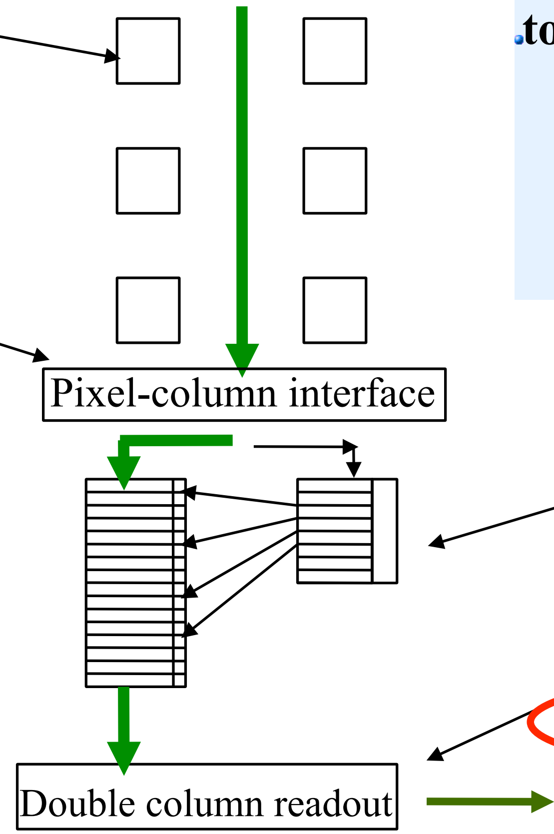
Doubling the buffer size in current 0.25µm ROC results in an increase of the periphery of 800µm ⇨ just possible for barrel

No R&D needed. Design ready in ~1-2 months. Needs verification

Data loss @ 2 x 10^{34}cm^{-2}s^{-1}, buffer sizes doubled

Pixel busy:
0.09% / 0.18% / 0.48%

Double column busy:
0.002% / 0.2% / 2.1%



total data loss @ 100kHz L1A:

- **1.2% @ 11cm**
- **2.8% @ 7cm**
- **10% @ 4cm**

Timestamp Buffer full:
0% / 0% / 0%

Data Buffer full:
0% / 0% / 0%
Now fully efficient infact

Readout and double column reset:
1.1% / 2.5% / 7.6%

Larger than before: was partially masked by buffer inefficiency

Can we reduce the r/o losses ?

- Where do they come from?
  - Once a dcol receives a L1A, the dcol stops data acquisition in order not to overwrite valid data → dead time while waiting to be read out.
  - After readout dcol is reset because buffer data is no longer valid → loose history of length=trigger latency (dominating contribution)
- Solution would be additional buffer stage for L1A data. Implications on overall schematic not clear yet. Do not want to sacrifice the well understood and debugged logic. Some ideas around.

Bandwidth limitation

- Not a ROC limitation, but huge impact on ROC
- Bandwidth of present analog links ≈ 40MHz · 2.5 bits (6 levels) = 100MBit/sec
- It is used ≈ 50% @ 4cm and 100kHz L1A
- Doubling the data volume will exceed the available bandwidth§ since
  - We can‘t use 100% of peak bandwidth
  - We have no additional fibres we could use
- Solutions:
  - 80 MHz analog: not really (my personal opinion). Probably feasible but non-trivial and painfull (think of present system)
  - Digital link at 160 or 320 MBit/sec. Also non-trivial but more standard. Potential partner
  - Doing some very clever but yet unknown tricks to make almost 100% use of available bandwidth

§ Present S-links will not take twice the data rate either

Conclusion

- Phase I ROC will be evolution of present ROC in 0.25μm
- We will probably need some modifications to reduce data losses for innermost layer which is O(16%). This is (almost) trivial for dominating contribution (enlarge buffers) and a lot more involved for NLO contribution O(10%) (additional buffer stage)
- Rest is ok O(2%) and won‘t be touched
- Uplink bandwidth is a problem with implications on the ROC
- Digital link would be beneficial (my view, open for discussion). But: big implications on overall system. Manpower? Partners?