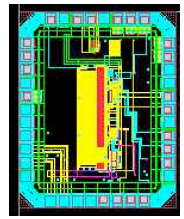
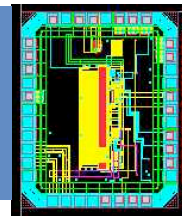


Radiation hard fast electronics for LHC experiments

Geoff Hall

Imperial College London

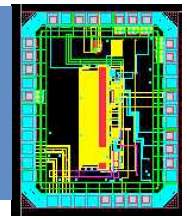
Outline



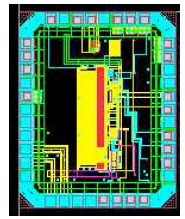
- Some brief historical remarks
- Requirements for LHC
- Choice of technology
- Radiation effects on electronics
- Examples - *try to relate effects to CMS implementations*
- Final comments

- Assumptions
  - This talk deals only with on-detector electronics
  - Audience is not circuit designers or electronics professionals

LHC electronics… in 1990

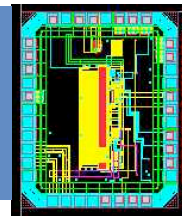


- Expected radiation levels were unprecedented
  - ~10Mrad in tracking regions
  - experience of failures at below krad levels
- Customised electronics was essential
- Several space-qualified processes, mostly of military origin
  - SoS, SoI, bipolar, GaAs, hardened CMOS,…
  - at least as many companies…
- Space system methodology not applicable
  - shielding plus qualification of commercial components
- As well as technology, there were several important other issues, primarily…
  - government regulation
  - cost



Requirements for LHC experiments

LHC parameters



- Major factors which influence electronics design and implementation

directly

- Clock speed
- Storage time
- Readout rate
- Granularity
- Data volume

indirectly

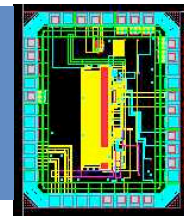
- Integrated L (radiation)
- Operating temperature
- T stability

implied

- Operating voltages
- **Power**
- Performance

	p-p	**Pb-Pb**
Luminosity	10^{34} cm^{-2}s^{-2}	10^{27} cm^{-2}s^{-2}
Annual integrated L	5x10^{40} cm^{-2}	
CM Energy	14 TeV	5.5 TeV/N
$\sigma_{inelastic}$	~70mb	~6.5b
Interactions/bunch	~20	0.001
Tracks/unit rapidity	~140	3000-8000
Beam diameter	20μm	20μm
Bunch length	75mm	75mm
Beam crossing rate	40MHz	8MHz
Level 1 trigger delay	≈3.2μs	≈3.2μs
Mean L1 trigger rate	<100kHz	<8kHz

Sub-detector requirements

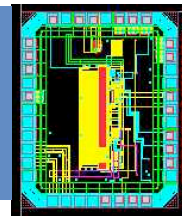


- All electronics are in a radiation environment at LHC

	physics	**technical**
Tracking	high spatial precision large channel count limited energy precision limited dynamic range	low power ~ mW/channel high radiation levels ~10Mrad
Calorimetry	high energy resolution large energy range excellent linearity very stable over time	intermediate radiation levels ~0.5Mrad power constraints
Muons	very large area moderate spatial resolution accurate alignment & stability	low radiation levels

1 Gray = 100 rads

Generic LHC systems

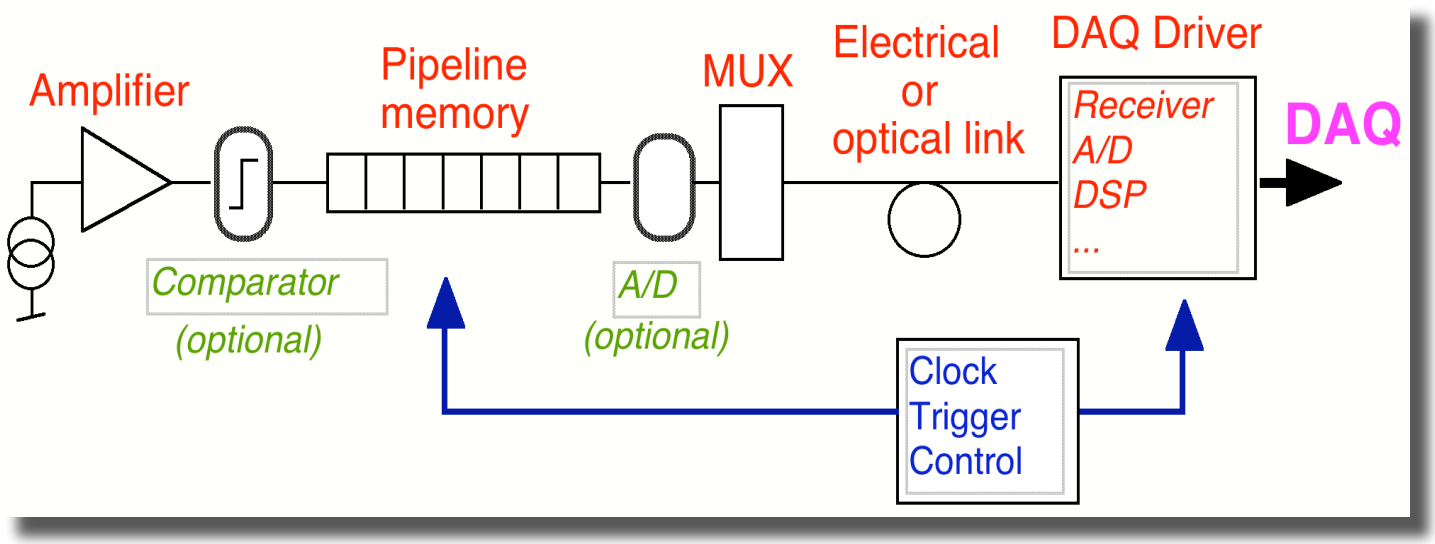


- functions required by all systems
  - amplification and filtering
  - analogue to digital conversion
  - association to beam crossing
  - storage prior to trigger
  - deadtime free readout @ ~100kHz
  - storage pre-DAQ
  - calibration
  - control
  - monitoring

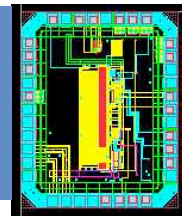
- Special functions for Calorimeters and Muon systems
  - first level trigger primitive generation

  (*so far not feasible for tracking*)

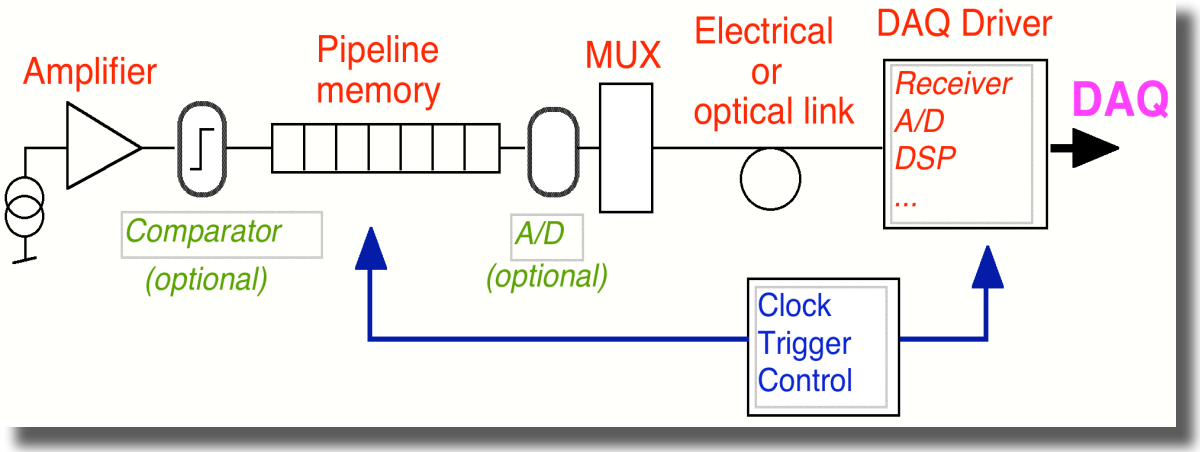
- example

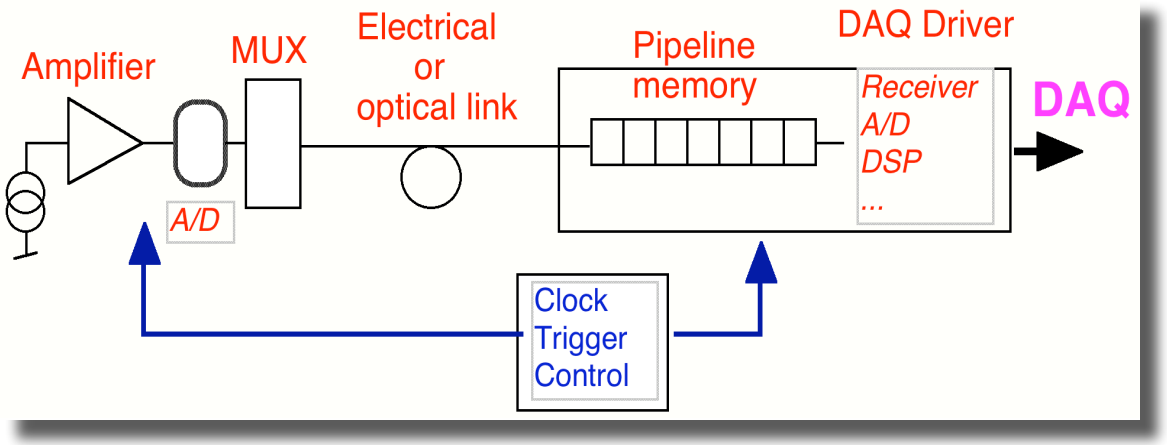


Possible implementations

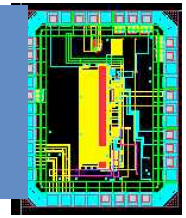


- As usual, there are several ways of doing the same thing
  - Ideally, take a system view from early design stage
- May be hard to say in advance which is best but decisions have consequences, eg:
- A-D conversion
  - On-detector = power, custom components,…
  - Off-detector = no of links, cost,..
- Link technology
  - Electrical: power, speed, noise issues,..
  - Optical: cost, technical challenges,…





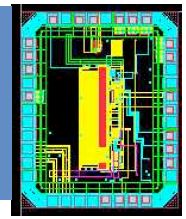
Implications of choices



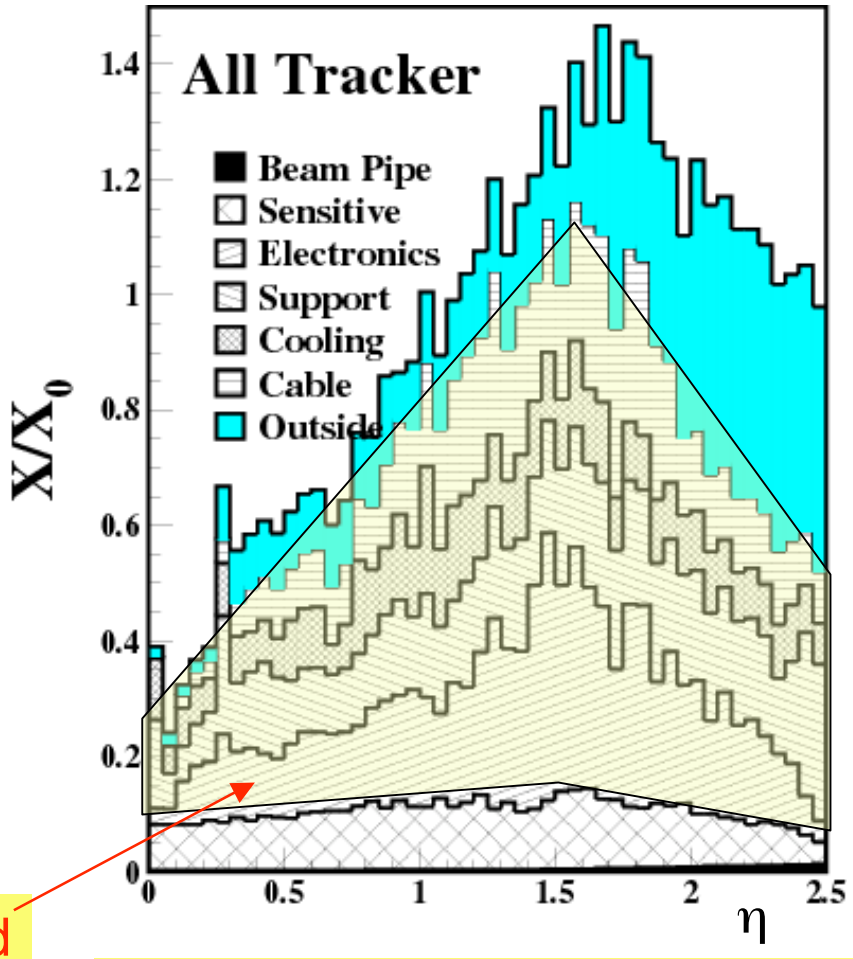
- Performance
- Power consumption
- Circuit size
- Programmability
- Uniformity
- Quality (Yield = fraction of working circuits)
- Testability

- Translate into choice of technology, cost, impact on detector, flexibility and ease of use,…
  - example: power

Impact on detector design



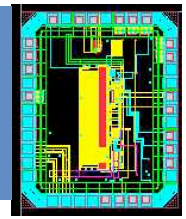
- Power dissipated in circuits is only part of the problem
- Long resistive cables typically consume more power than active electronics
  - weight, cooling,..
- Consequent impact on material budget, especially for interior regions of experiment



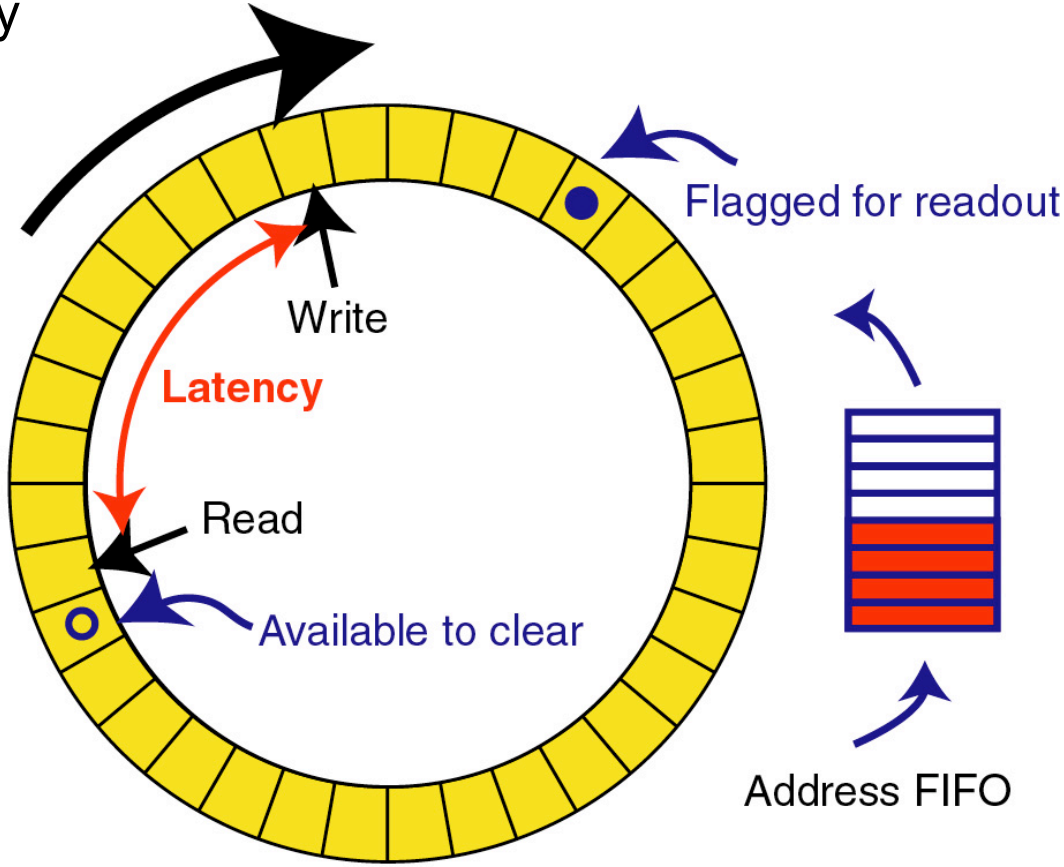
All electronics related

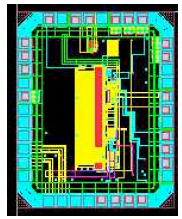
Material budget in CMS Tracker

“Deadtime free” operation



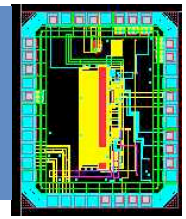
- Data stored in pipeline memory with “ring” topology
- Pointers record current (write) location and location of data being read
- Addresses of used locations stored in FIFO to be skipped during writing
  - pipeline length is dynamic
- Pipeline length, buffer depth, storage time chosen to ensure that rate of data lost is sufficiently small
  - queuing problem





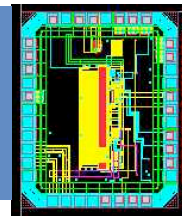
Choice of technology

Technology choice

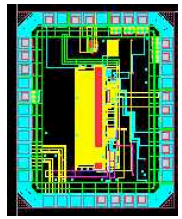


- CMOS has become the preferred technology
- Modern CMOS meets LHC speed and power constraints
- It has been shown to be very radiation hard
- Quality and uniformity has been demonstrated to be high
- Commercial electronics is dominated by CMOS
  - It is very costly to swim against the stream
- HEP is a very small community compared to industry
  - Largest LHC orders <1000 wafers
  - Commercial foundry production >40,000 wafers per month
- There are benefits from adopting a few common technologies and standards

Alternative technologies

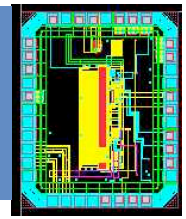


- All considered, and some are used..
- GaAs - intrinsically hard to high level
  - few processes, not analogue
- SoI/SOS CMOS (Silicon on Insulator, Silicon on Sapphire)
  - investigated but excessive noise
- Hardened CMOS
  - **few** specialised processes, even **fewer** foundry services
  - most to ~1Mrad
  - expensive
- bipolar - neutron sensitive, especially power devices
  - ICs tolerant to high level but observed dose & rate effects

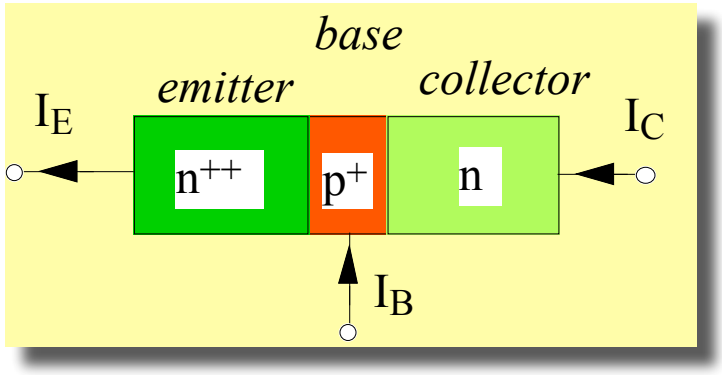


Radiation effects

Basic bipolar radiation effects

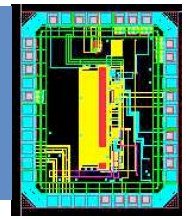


- Transistor operation
  - Carriers flow from emitter to collector, via base
  - Recombination in base controls transistor action (gain)
- Effects of radiation
  - Hadrons cause atomic displacement
    - Traps (band gap energy levels)
    - Increased carrier recombination in base

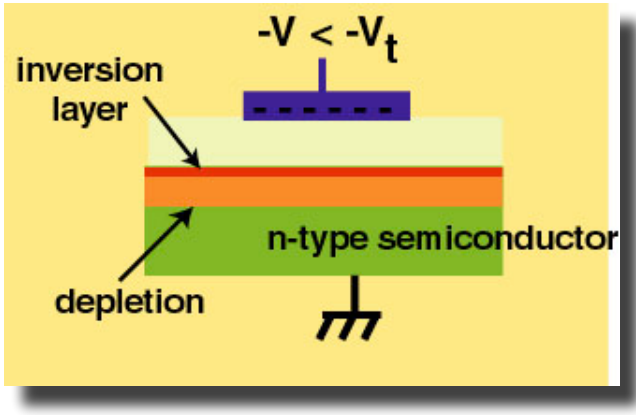


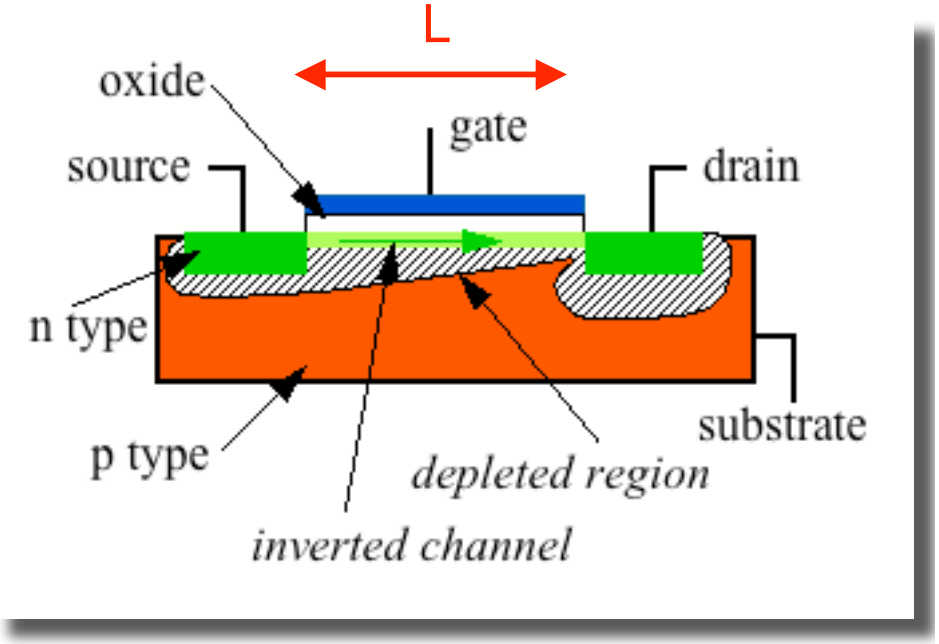
- Consequences
  - gain degradation, transistor (mis-)matching, dose rate dependence
- NB bipolar processes can also be sensitive to surface effects
  - like CMOS

CMOS transistor operation

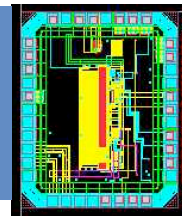


- Reminder of basic FET physics
  - bias “metal” gate to deplete substrate
  - beyond a certain threshold voltage, substrate does not deplete deeper
  - instead “inversion layer” created
- Inversion layer
  - extremely shallow, at oxide-silicon interface
  - carriers mobile in applied field
- Transistor operation
  - Modulation of source-drain current via V_{gate}

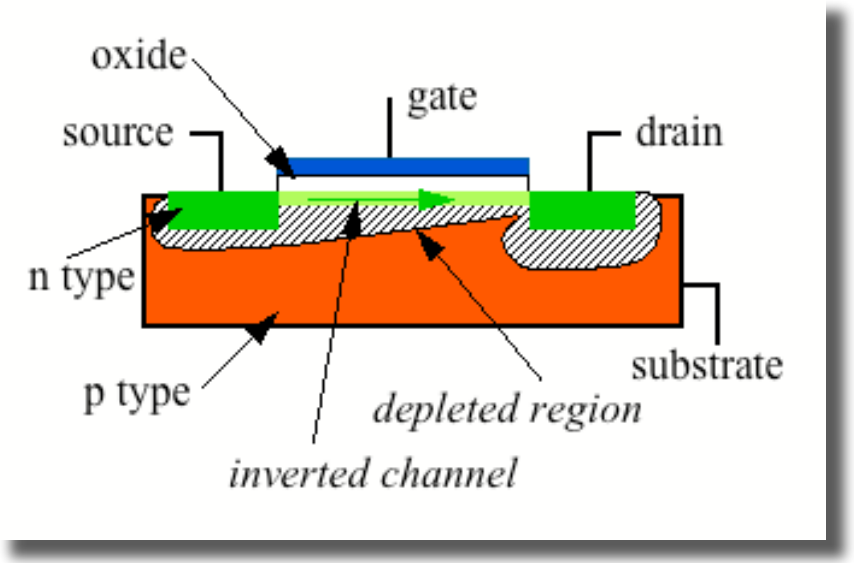




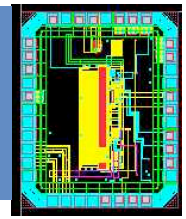
CMOS radiation effects



- Inversion layer is so shallow that bulk damage has no effect
  - so CMOS is hard against neutrons
- Real oxide contains trapped (positive) charge at interface
  - Compensated for during manufacturing process
- Charged particle and gamma irradiation generates carriers in oxide
  - become trapped at Si-SiO_2 interface
  - interface traps influence short-term behaviour
    - details depend on bias
- Consequences
  - threshold (gate) voltage shift,
  - leakage current through or around transistor (especially NMOS)



Other CMOS radiation effects

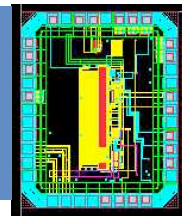


- Latch-up - can affect all technologies
  - charging of surface layers influences charge in substrate
  - *parasitic* bipolar devices draw current, and can be **destructive**
  - generally avoided by technology design

- Single event effects - **non-permanent**
  - large ionisation charge deposited within device, usually from recoiling ion
  - Some of the charge collected on sensitive circuit node
  - Influences voltage and can change state of node

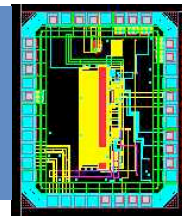
  - Important for digital logic
  - Essentially undetectable at the time
  - But can be mitigated by design, including majority logic circuits

Noise sources



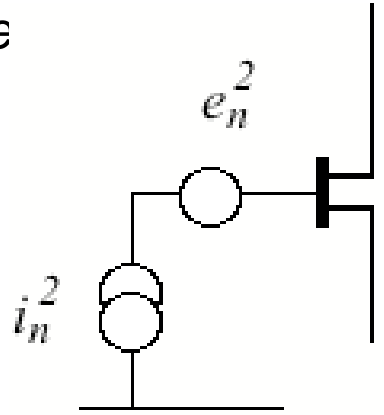
- Thermal noise
  - Quantum-statistical phenomenon; carriers in constant thermal motion
    - macroscopic fluctuations in electrical state of system
  - Typically associated with input transistor or resistive components
- Shot noise
  - Random fluctuations in DC current flow
  - Typically associated with sensor
- *1/f* noise
  - commonly associated with interface states in MOS electronics
  - Luckily, less important for high speed electronics
- In a properly designed amplifier system, the dominant noise sources should be at the input
  - Generally can ignore noise sources after front-end

Noise in MOS circuits



- Gate shot noise is negligible *insulating gate and no curre*
- Thermal noise voltage from channel
  - $e_n^2 = 4kT\gamma(\frac{2}{3g_m})\Delta f$ γ = *excess noise factor ~ 1*
- Transconductance
  - $C_{ox} = \varepsilon_{ox}/t_{ox}$
  - W/L = transistor width/length

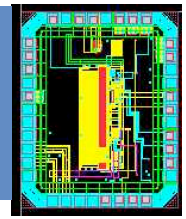
$$g_m = \sqrt{2\mu C_{ox} I_{DS}\left(\frac{W}{L}\right)}$$



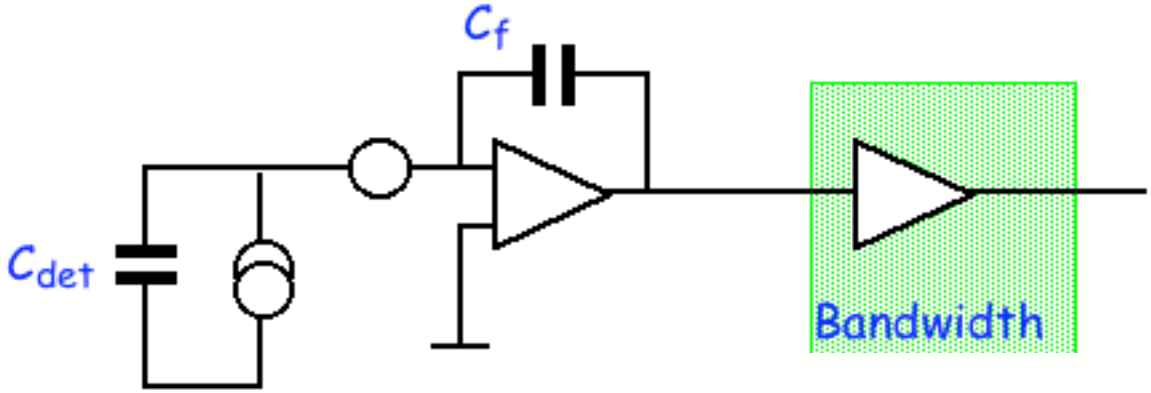
C = capacitance
T = temperature
Δf = bandwidth
μ = mobility (v/E)

- *1/f* noise usually unimportant (for LHC)
- Implications
  - To achieve low noise, aim for large W/L and large (tolerable) I_{DS}
  - but $C_{amp} = C_{ox}WL$ and require capacitance matching: $C_{amp} \approx C_{det}/3$
  - Mobility is also T dependent $\mu(T) \sim T^{-3/2}$

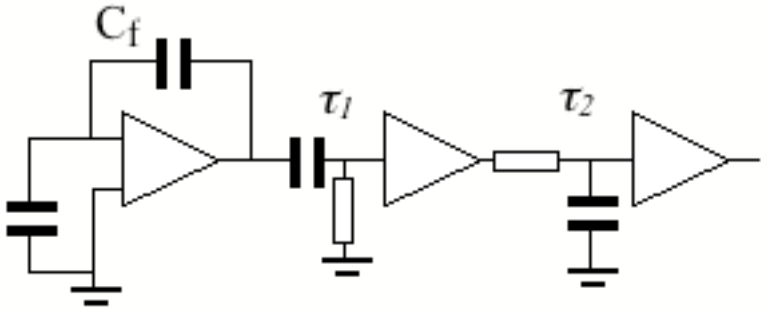
Signal processing

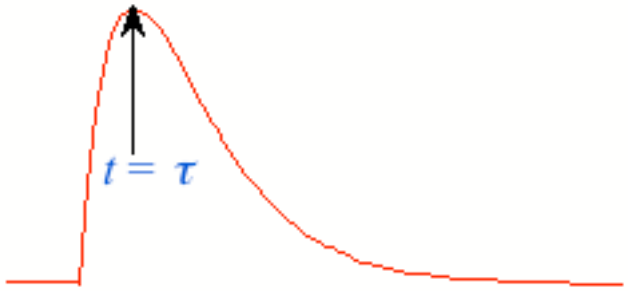


- Once noise sources are known, their impact can be calculated
  - Pulse shaping use
  - or other filtering te



  - Useful point of cor





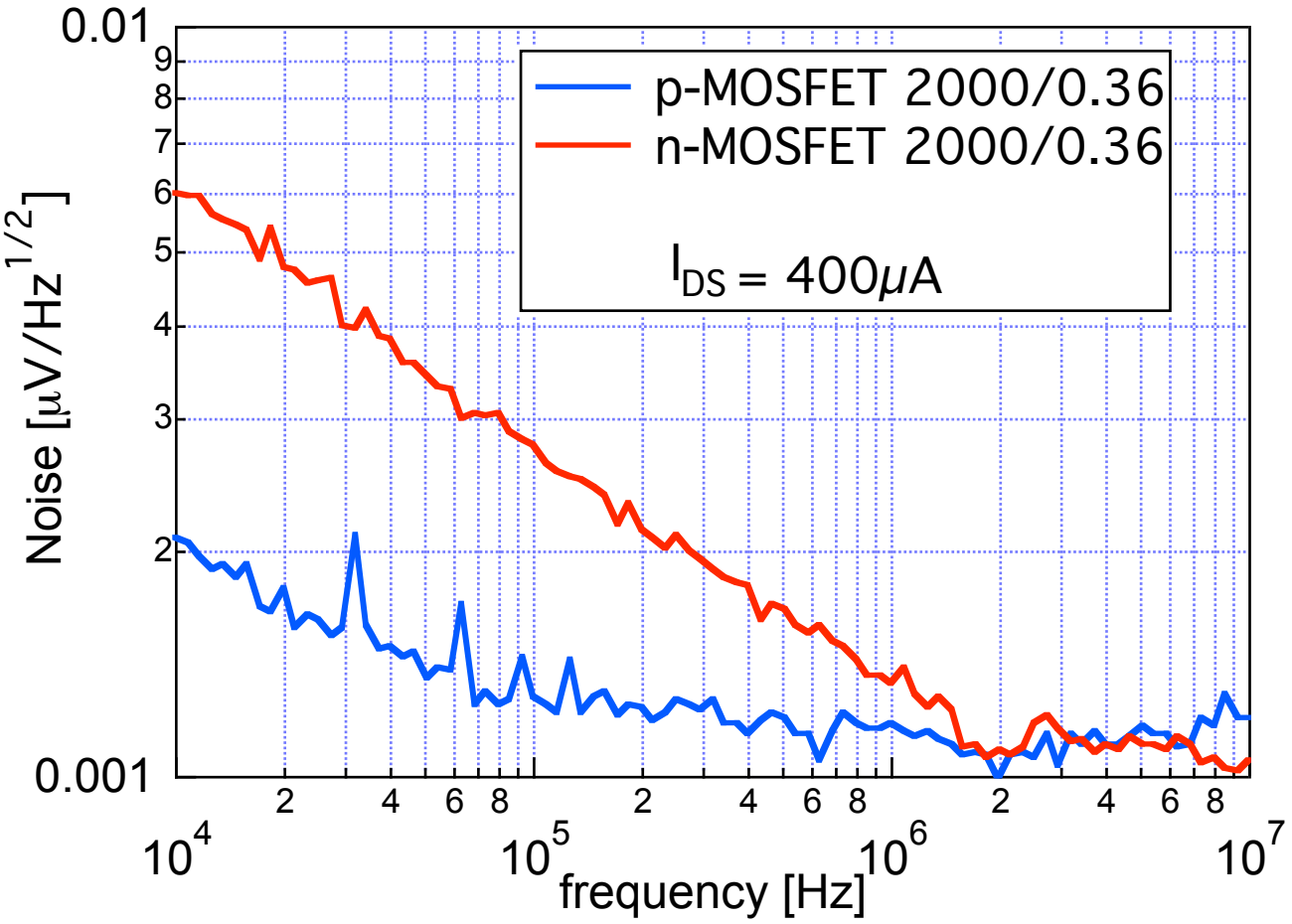
$$ENC^2 = \frac{e^2}{8}\left(\frac{4kTR_sC_{tot}^2}{\tau} + 2eI\tau + 4A_fC_{tot}^2\right)$$

Noise spectra

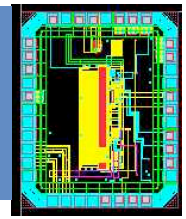
- pMOS preferred for lower 1/f noise

- 3dB bandwidth

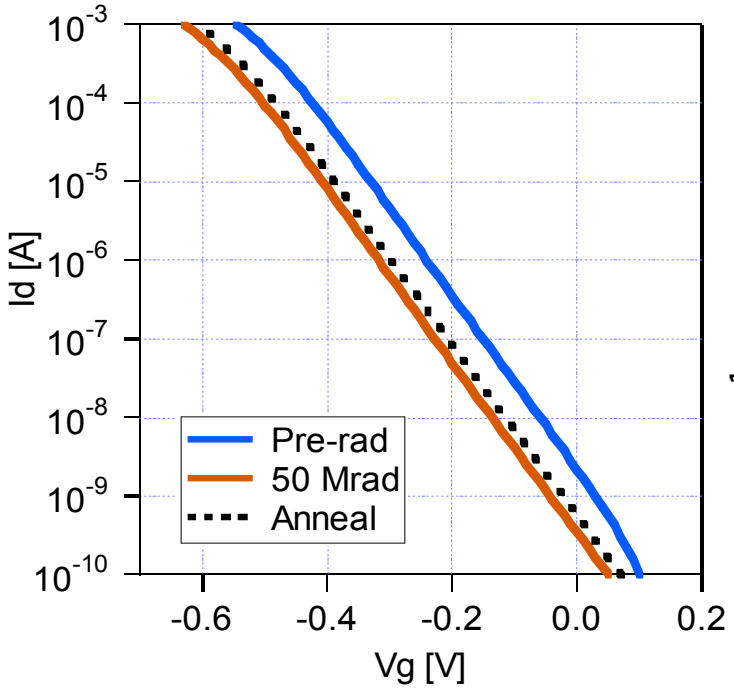
Δf_{3db} =
2.6 - 15.4MHz
  - CR-RC pulse shaping
  - τ = 25ns



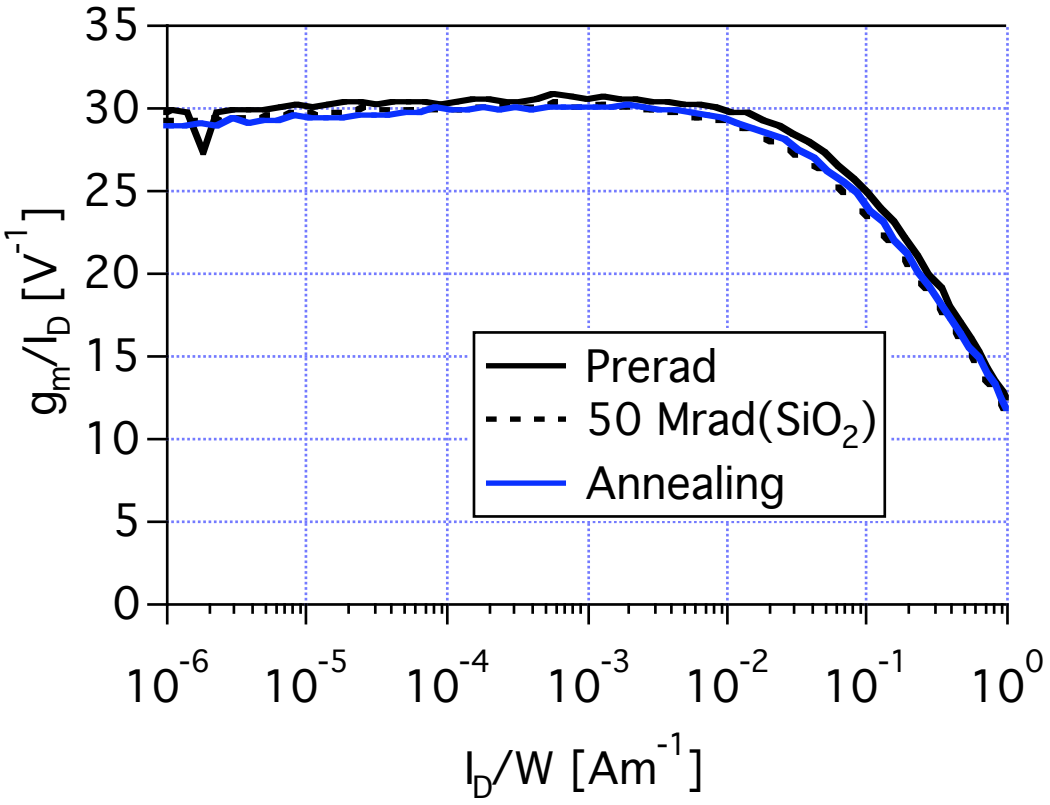
Post-radiation (0.25µm pMOS)



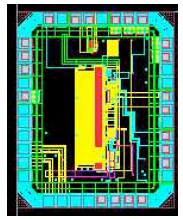
- Threshold voltage



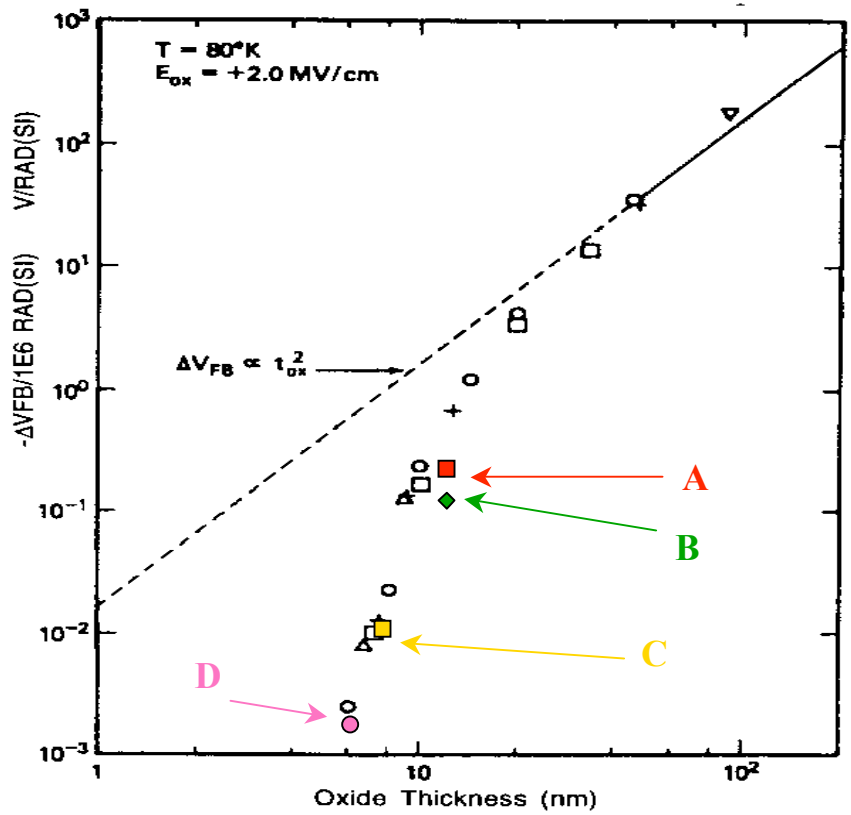
- Transconductance



Why so radiation tolerant?



Gate oxide scaling



After N.S. Sacks, M.G. Ancona, and J.A. Modolo, IEEE Trans.Nucl.Sci., Vol.NS-31 (1984) 1249

- Electron tunneling neutralizes trapped holes in thin oxides.
- Total dose effects, such as V_t shift, are naturally reduced in deep submicron processes.

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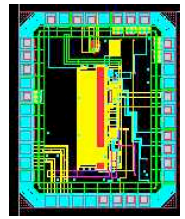
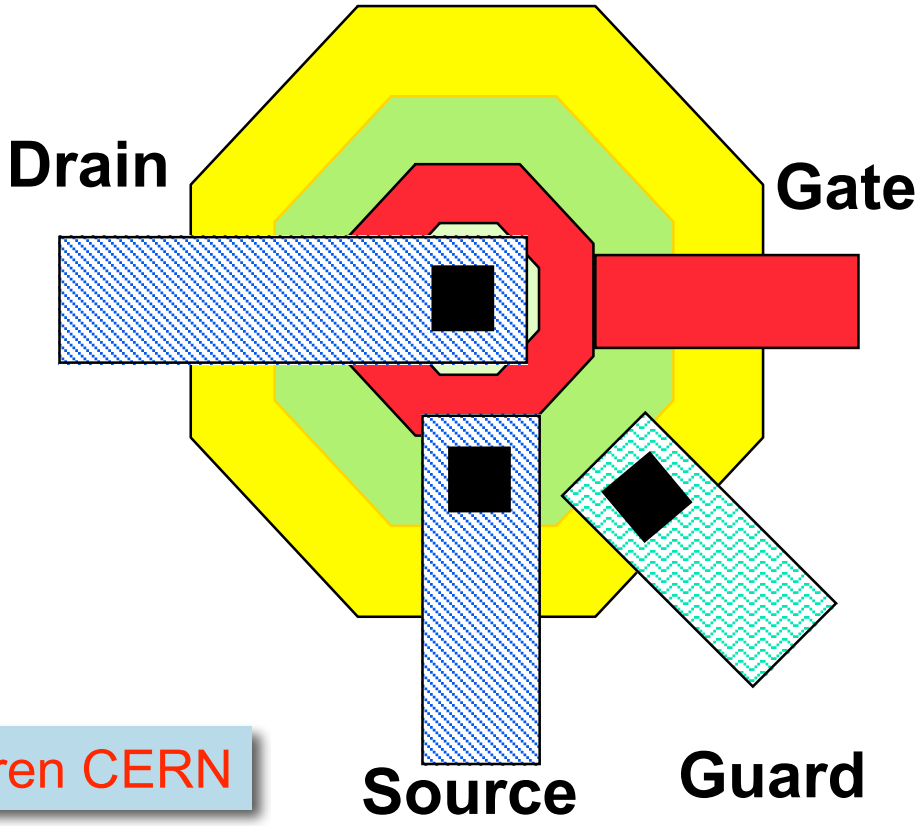
Radiation tolerant design



Thin gate-oxides + Gate all-around layout

- Min-size NMOS layout
  - Edge-less structure eliminates leakage via parasitic edge transistor.
  - Guard ring eliminates leakage between devices and provides latch-up protection.
  - Higher capacitance of gate all-around structure improves SEU tolerance.
    Further SEU tolerance by circuit design (SEU-tolerant flip-flops) or system design (triple-redundant logic, error detection and correction coding etc.)



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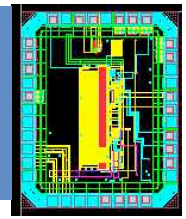
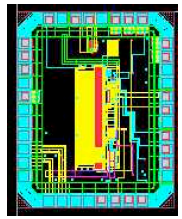
“Standard” features in 2004

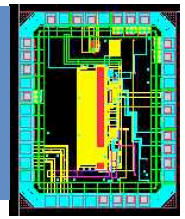


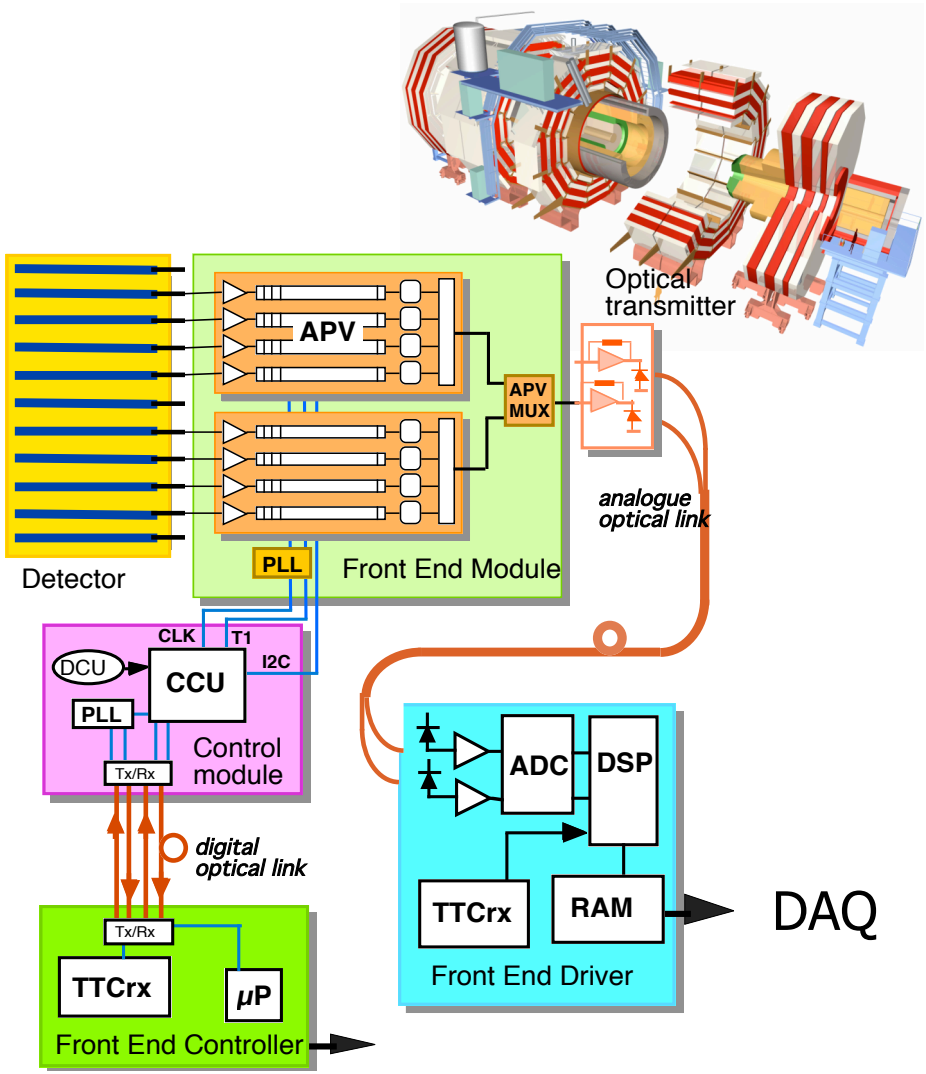
- Small dimensions and multi-levels of metal allow room for many useful programmable features…
  - internal control of bias currents, voltages (shaping time, etc)
  - capacitor values (by summing/switches)
  - adjustable thresholds (via DAC)
  - switchable gains, signal polarity, signal processing
  - standard interfaces (I^2C, LVDS,…)
  - redundant logic, for SEU effects
  - internal self-calibrate
- Many of these are vital for evaluation and large scale test
  - or tuning during operation



Examples from CMS

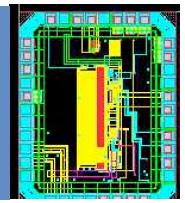
CMS Tracker Electronic System



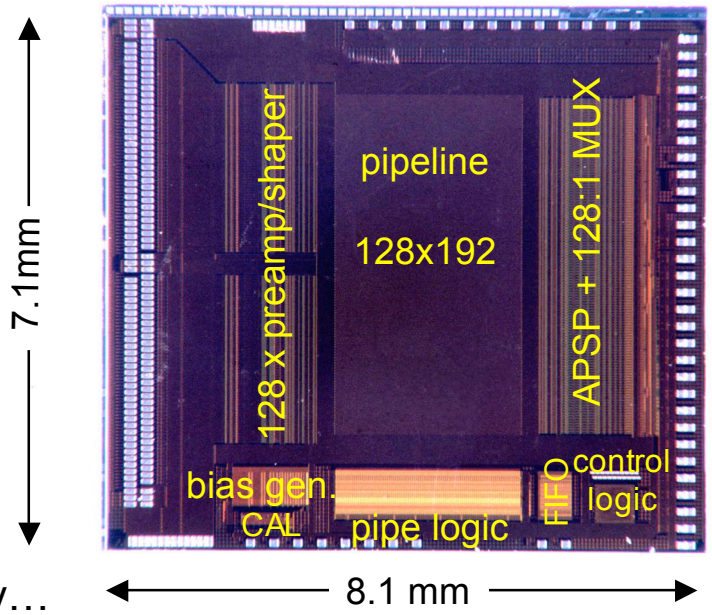


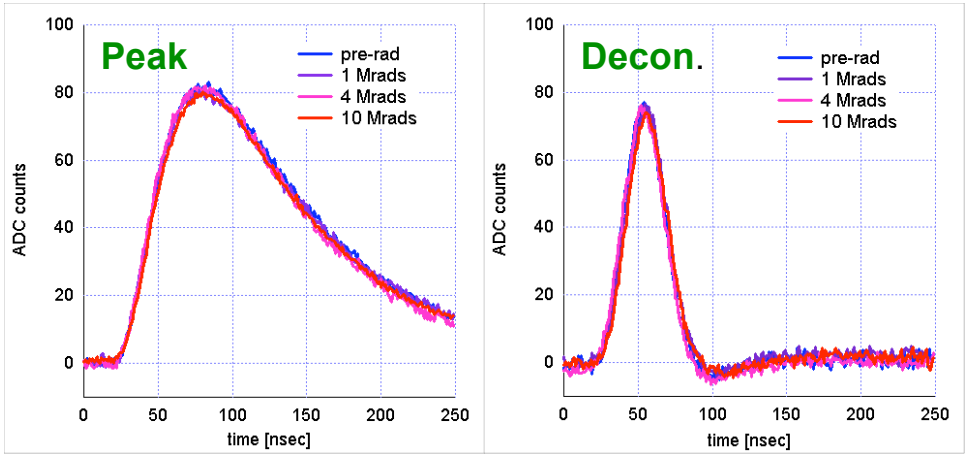
- Main features
  - Analogue readout
  - No on-detector zero suppression
  - Optical analogue data transfer
  - Control signals sent optically
  - Local electrical transfer
- Only 0.25µm ASICs
  - APV25
    - ~100,000 die, inc spares
  - Complete control system
    - 5000 - 20000 die of:
    - DCU, PLL, CCU, LD…
    - LVDSbuf/mux

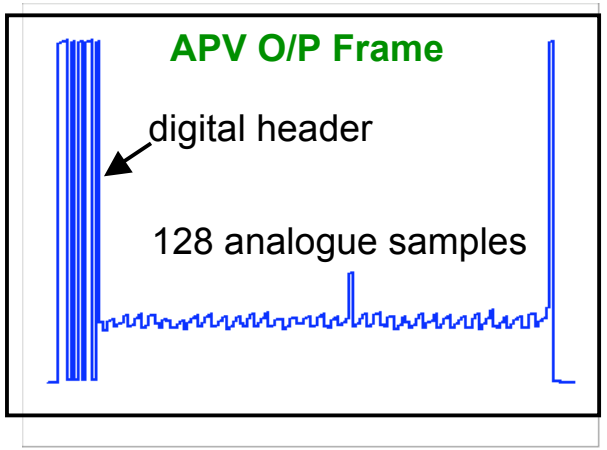
APV25



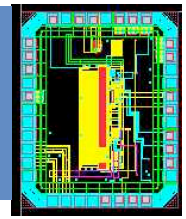
- Main features
  - 128 readout channels
  - 50 ns CR-RC amplifier
  - 192 cell pipeline memory
  - alternate operating modes
    - peak, deconvolution, multi-mode
    - on-chip analogue signal processing
  - on-chip ancillary functions
    - eg calibration, I²C, programmable latency…



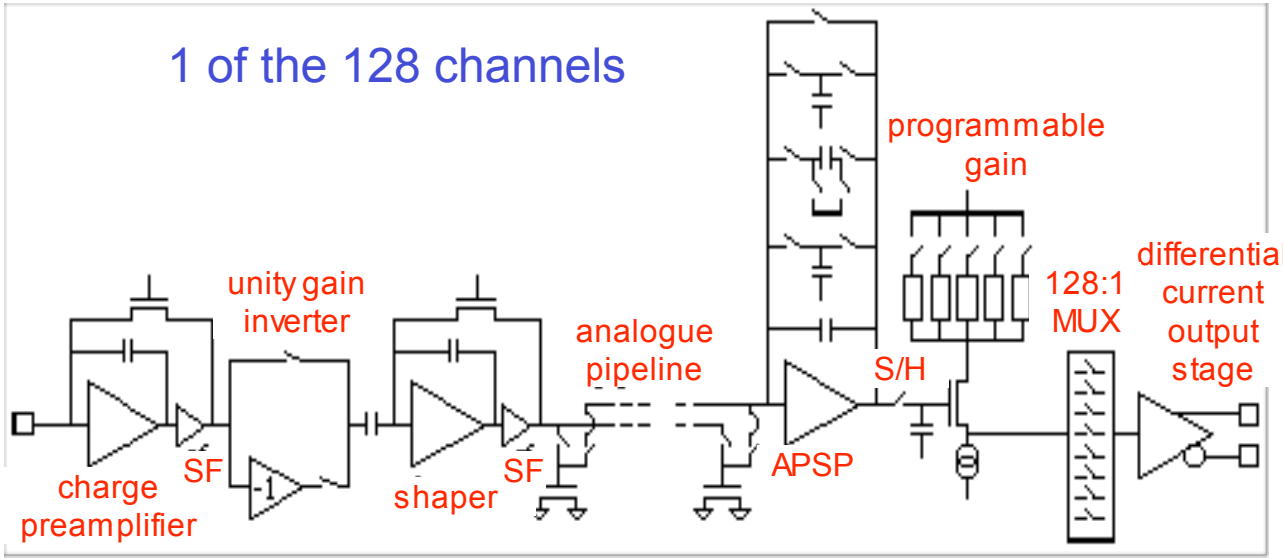




APV25 design



V_{supply}	0 - 2.5V
Power/channel	1.9mW analogue + 0.4mW digital
Input transistor	pMOS W/L= 2000/0.36 I_{DS} = 400µA
Filtering	50ns CR-RC or 3 weight analogue sum (deconvolution)
Pipeline length	192 cells, including 32 [max] cells readout buffer



Analogue power	mW
Preamplifier + buffer + inverter	0.90
Shaper + buffer	0.25
APSP	0.20
OP & MUX	0.54

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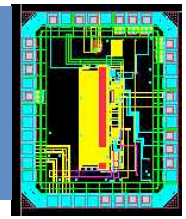
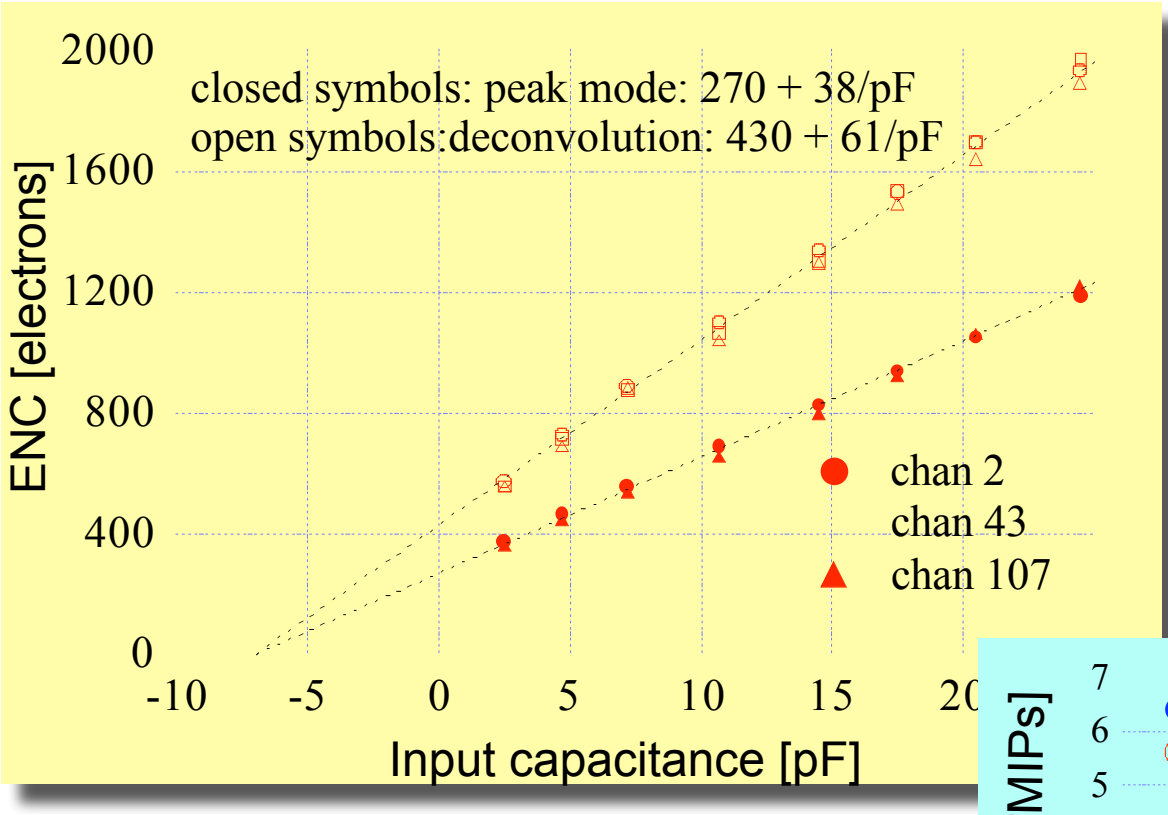
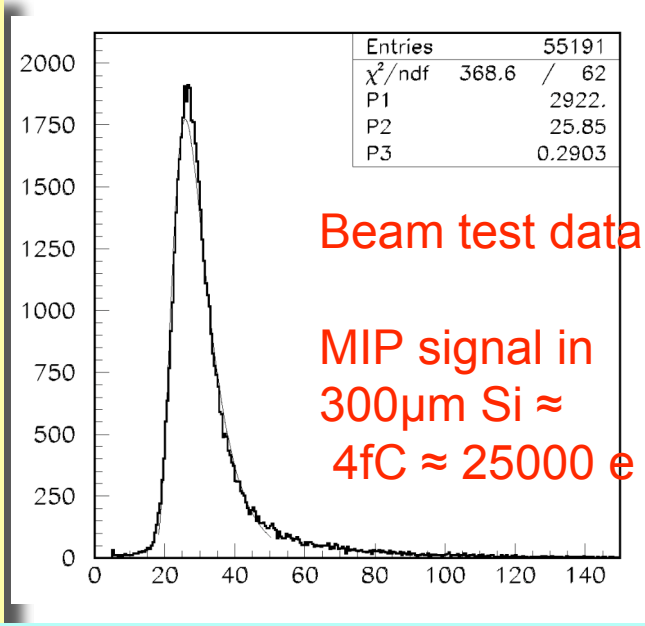
Imperial College

APV25 performance

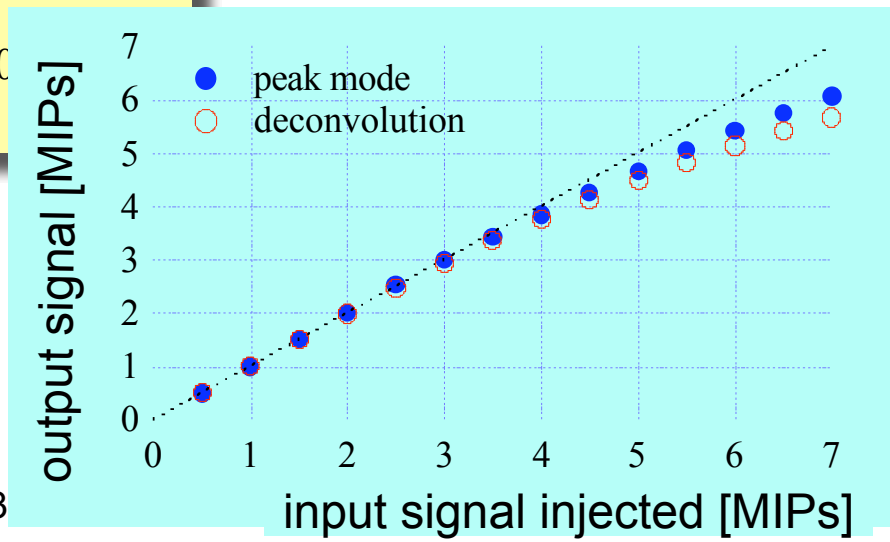






Beam test data

MIP signal in 300μm Si ≈ 4fC ≈ 25000 e



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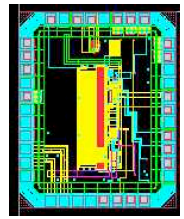
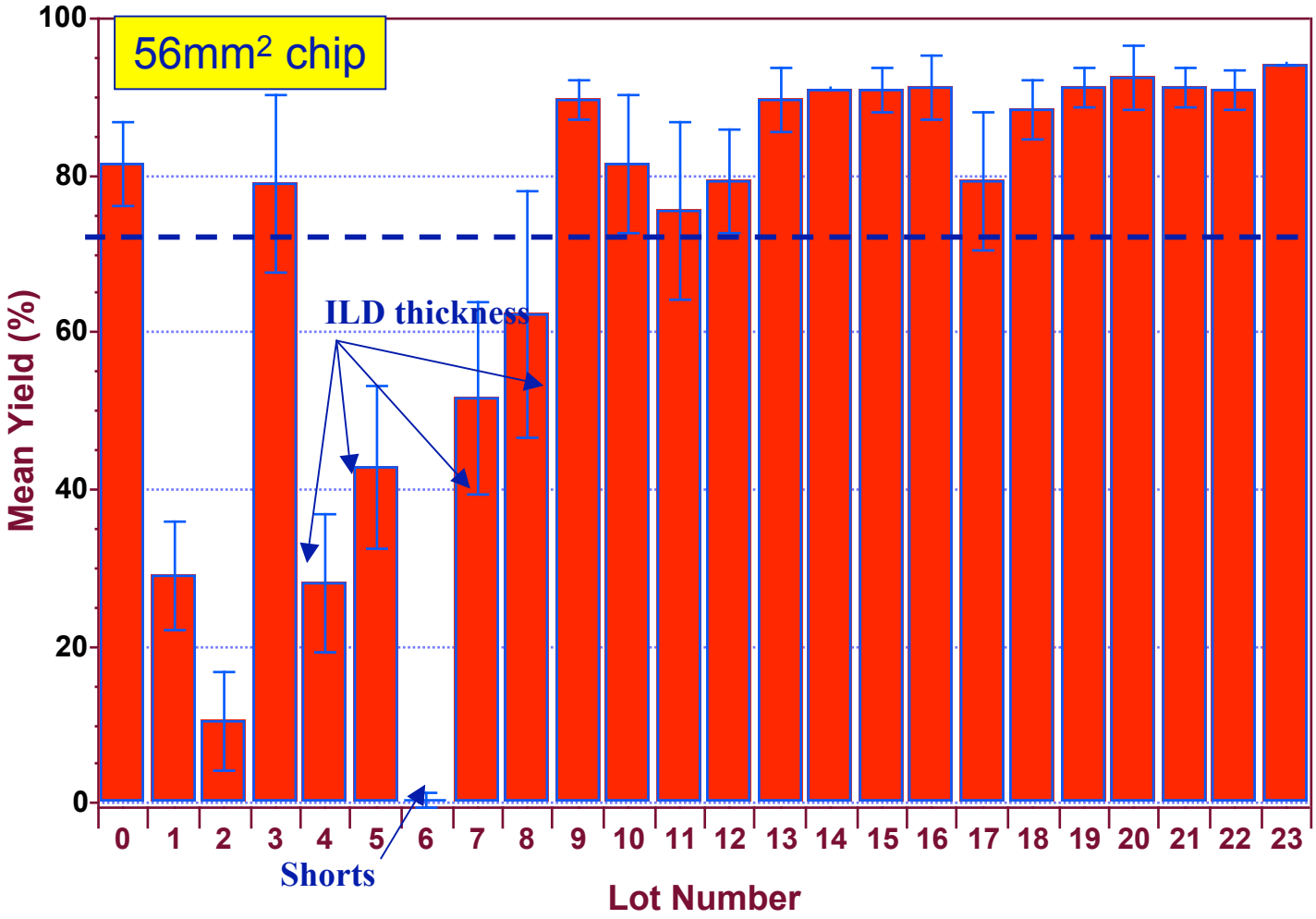
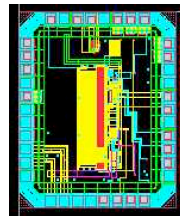
APV25 Yield



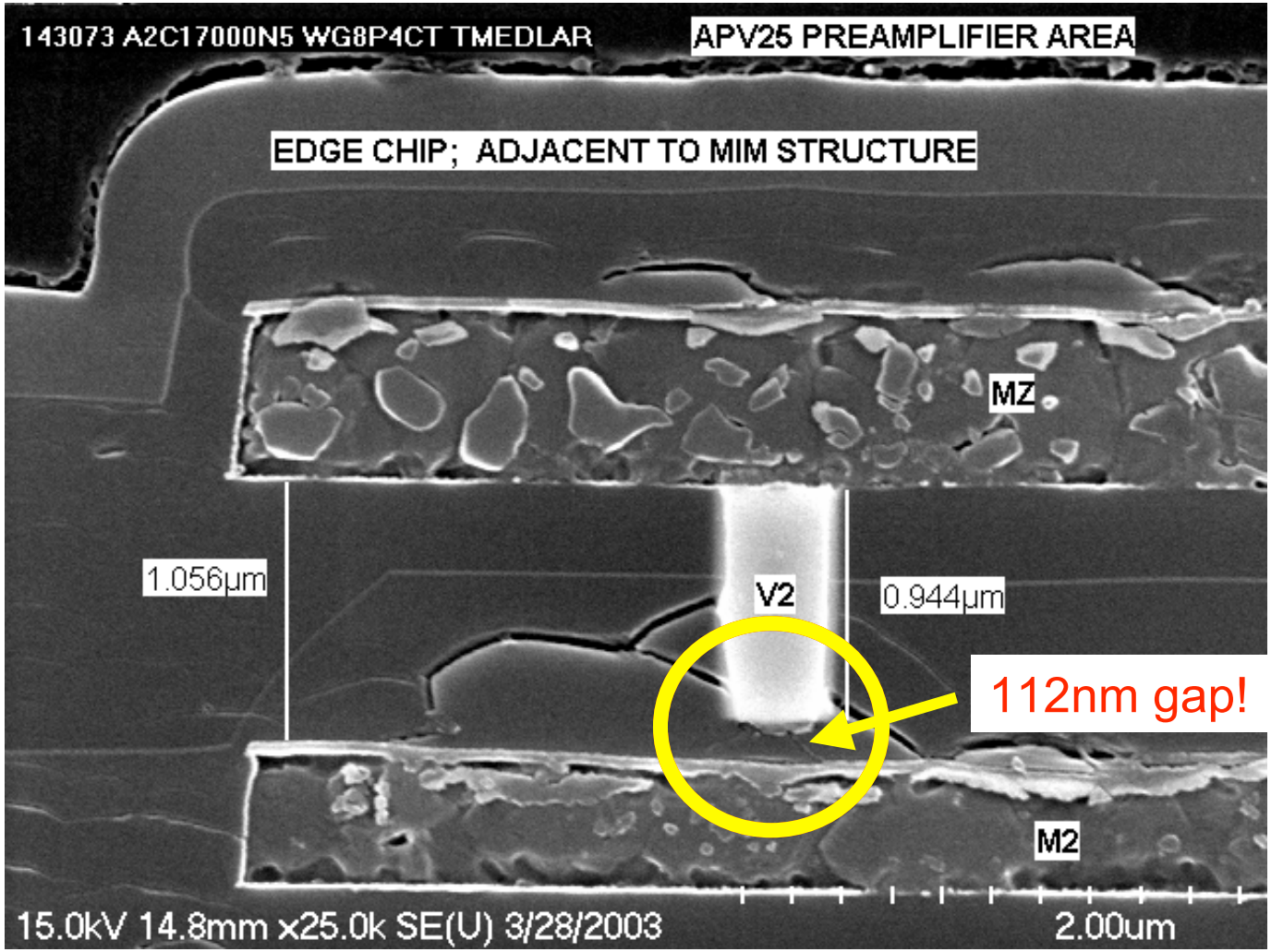
- Some process optimisation was necessary in early production runs due to heavy use of one metal layer
- Common to many other HEP designs



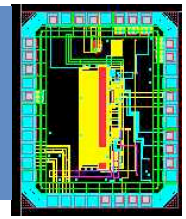
IBM failure analysis



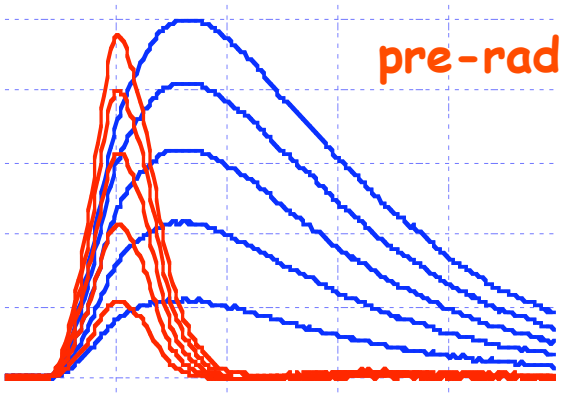
- One of **many** complex images and details provided of foundry process and monitoring…
- Illustrates the importance of good cooperative relationship with vendor

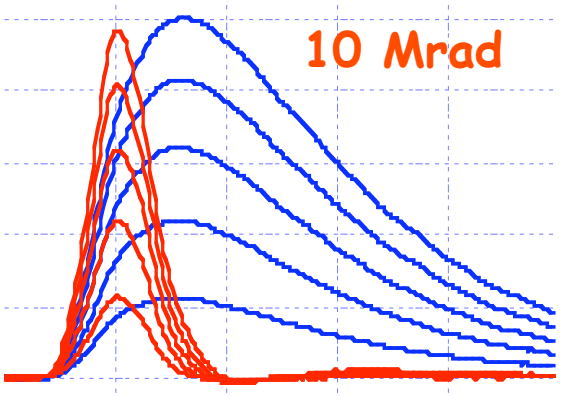


APV25 irradiation results



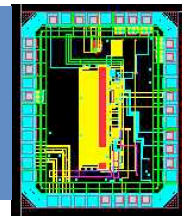
- Only minor effects after irradiation
  - Compensated for by minor tuning of parameters at long intervals during operation



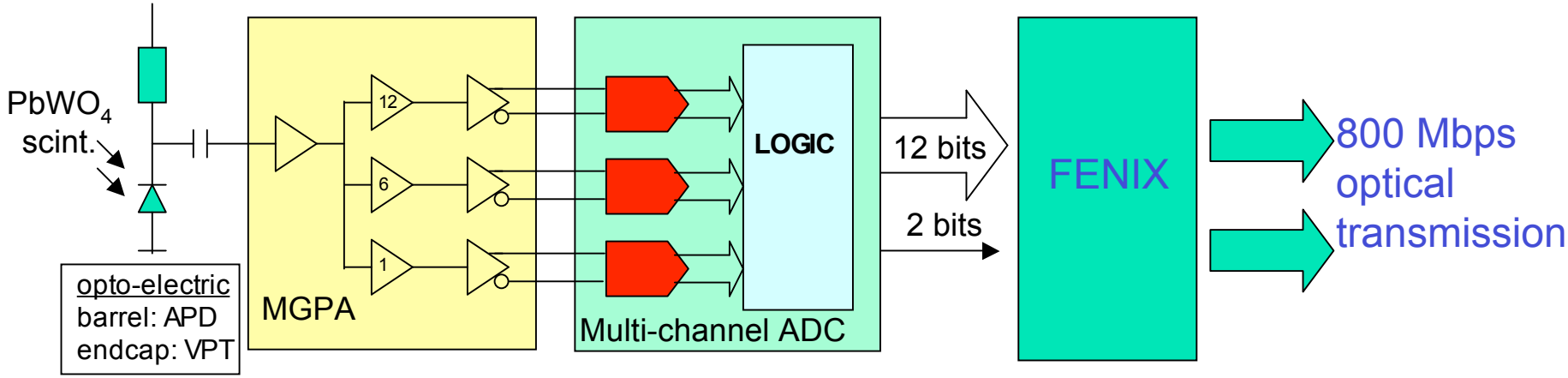


  - True for noise and other parameters
    - plots now “uninteresting”

CMS ECAL electronics



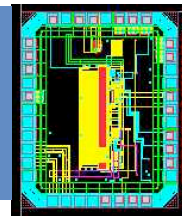
- High resolution crystal calorimeter
  - requires $\sigma/E = 0.5\%$, with 16 bit dynamic range



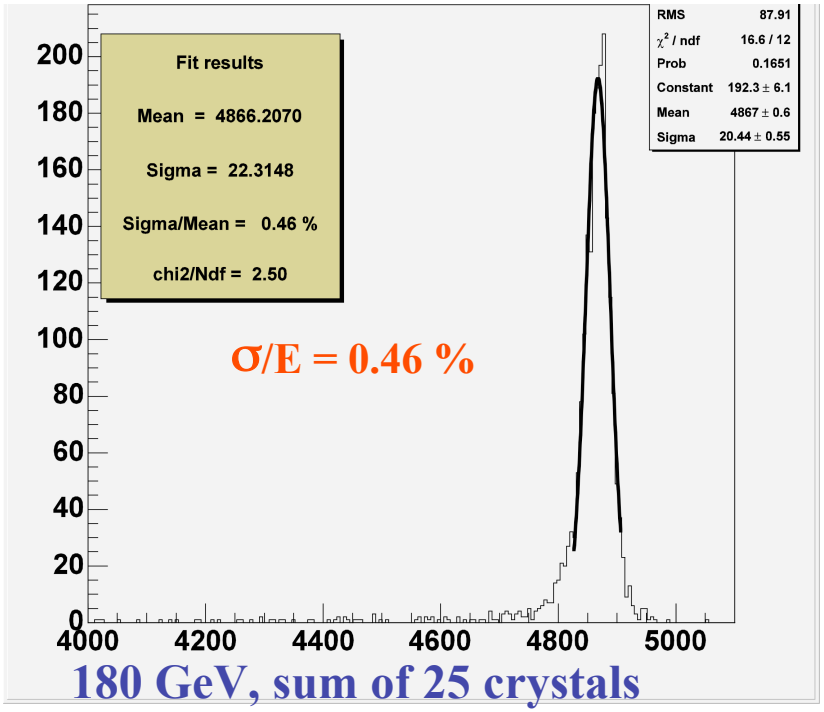
  - MGPA: multi-gain amplifier
  - 12-bit ADC: CMS collaboration with specialist design house
  - FENIX: multi-function digital chip - VHDL translation to ASIC
  - 0.25µm control ASICs developed for tracker
  - high speed 0.25µm GOL optical link driver

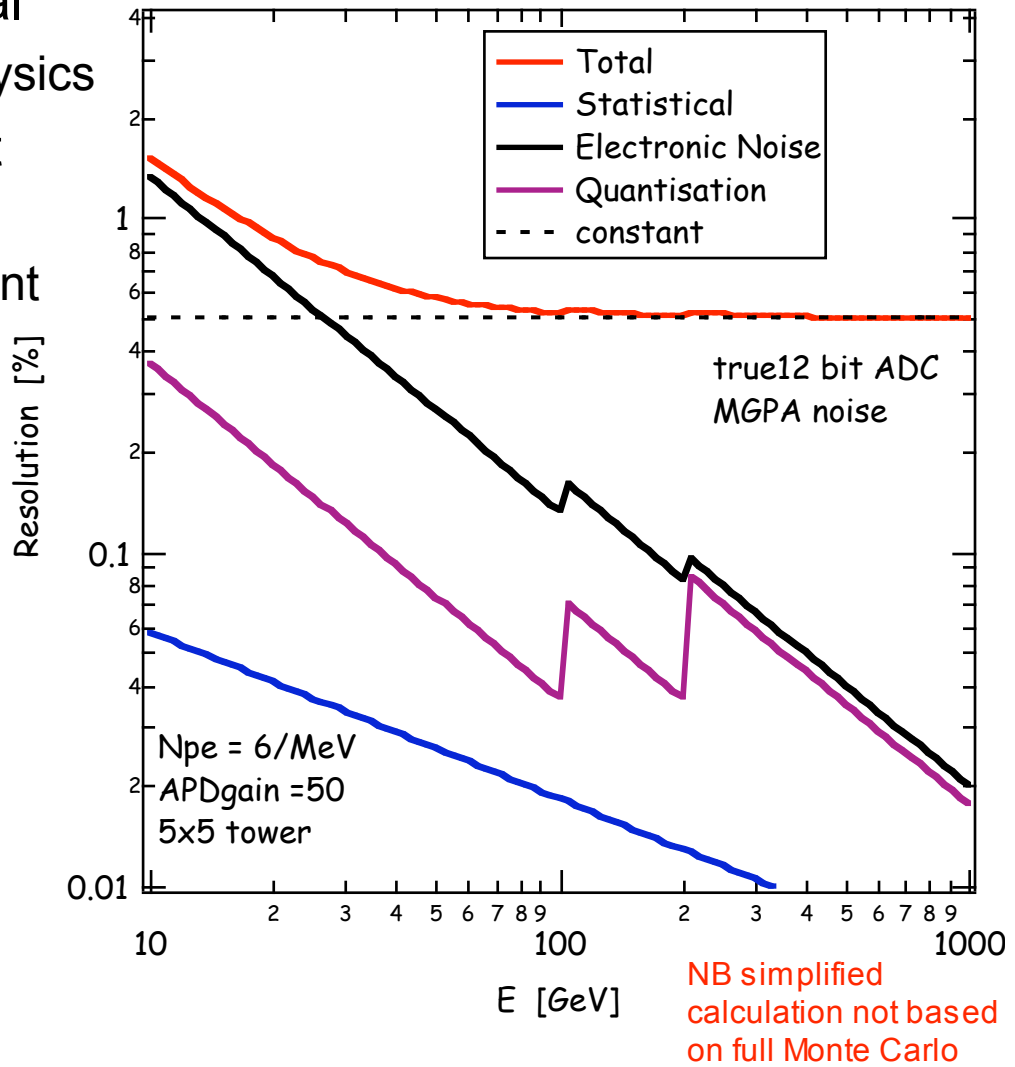
Now all based on 0.25µm CMOS

Energy resolution



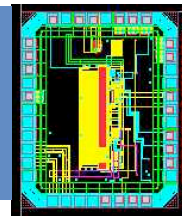
- High gain channel is most crucial
  - should hold most interesting physics
- Higher noise tolerable on lowest gain range
  - because electronics not dominant





NB simplified calculation not based on full Monte Carlo

MGPA requirements



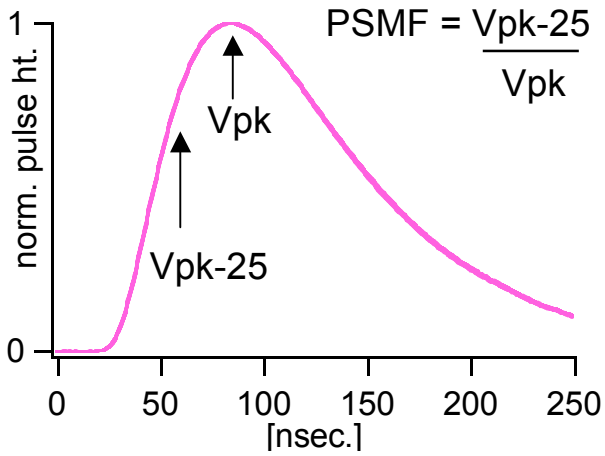
- Specifications

Parameter	Barrel	End-Cap
Full-scale signal	60pC	16pC
Rms noise	10,000 e (1.6fC)	3,500 e (0.56fC)
Input capacitance	~200pF (APD)	~50pF (VPT)
Gain ranges	1, 6, 12	
Gain tolerance	±10%	
Linearity	0.1% full scale (each range)	
Pulse shape (impulse)	40ns CR-RC	
Channel to channel pulse shape matching	<1%	
Supply voltage	0 - 2.5V (0.25µm CMOS)	
Output signals to ADC	Differential 1.8V, ±0.45V around ≈1.25V	

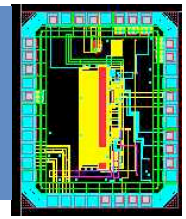
•Additional requirements;

calibrate - for functionality verification

I2C setting channel offset



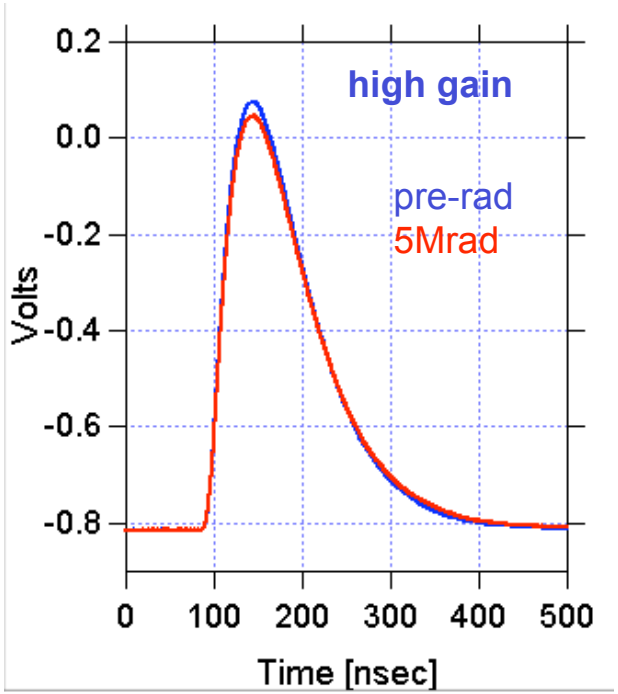
Main design features



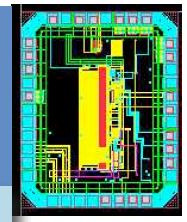
- Gain switching allows to achieve dynamic range and resolution
  - Custom ADC required to match amplifier at acceptable cost
  - ASIC approach allows 3 identical ADCs in single chip
  - and ensure radiation hardness
- Single MGPA design with external components satisfies both barrel and endcap

	C_f	R_f
Barrel	33pF	1.3kΩ
End-Cap	10pF	4kΩ

- Large PMOS input
  - 30,000/0.36, I_{DS} = 20mA -> C_{GS} ~ 60pF, g_m ~ 0.3S
    - needed for short rise-time, C_{det} ~ 200pF (barrel)
    - MGPA power = 600mW
  - In this case, significant noise sources apart from input transistor
  - Noise dominated by R_f (little C_f influence)
    - happily - noise scales for endcap in right ratio

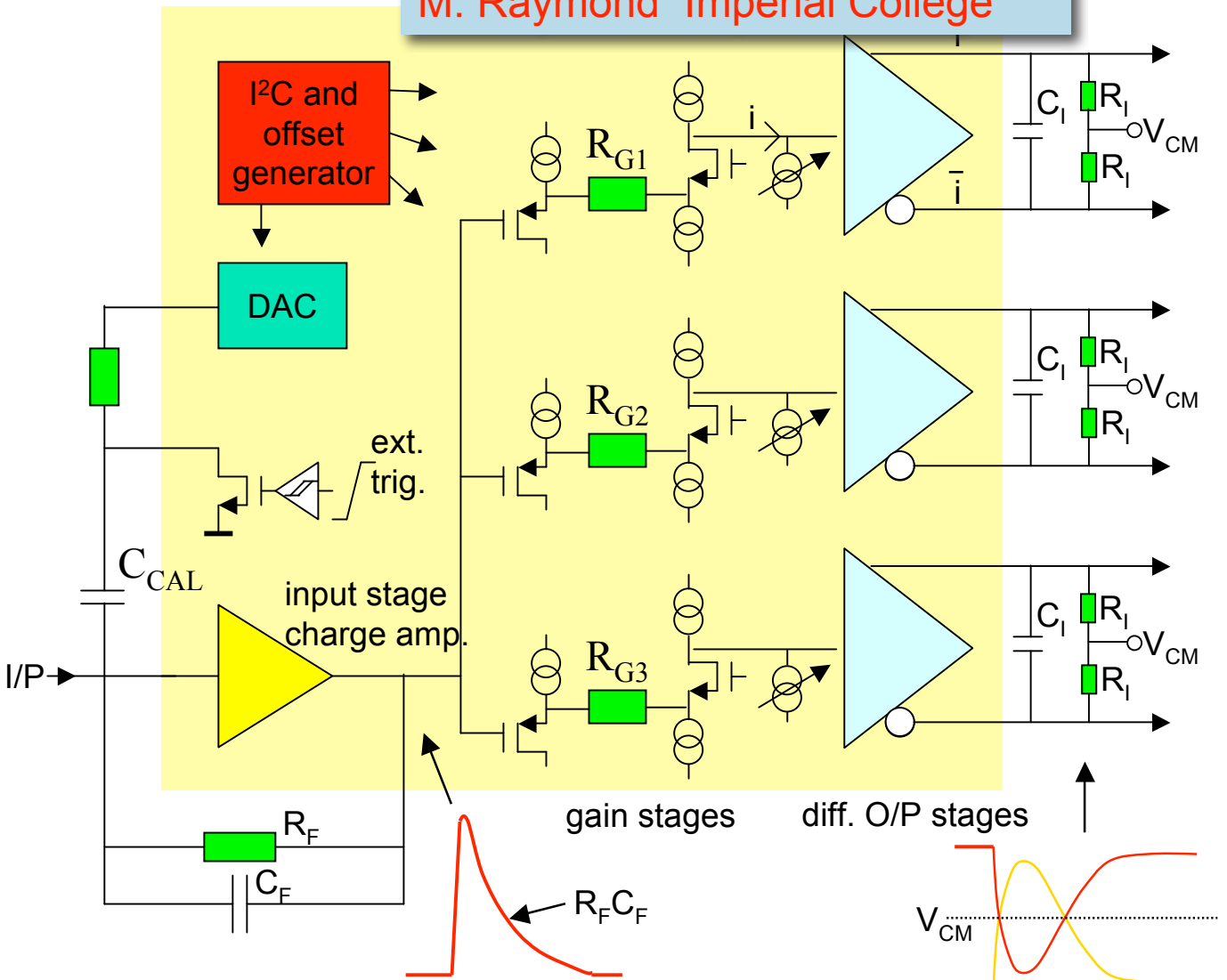


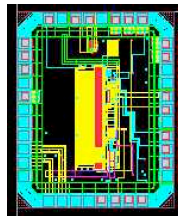
MGPA architecture



M. Raymond Imperial College

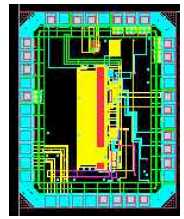
- Single preamplifier
- 3 shapers - gains set with on-chip resistors
- C_F & R_F external components
- C_F chosen for max. possible gain
- R_F chosen for 40 ns decay
- 1 chip suits barrel & end-cap





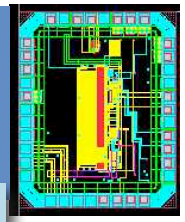
The future

Relevant technology trends



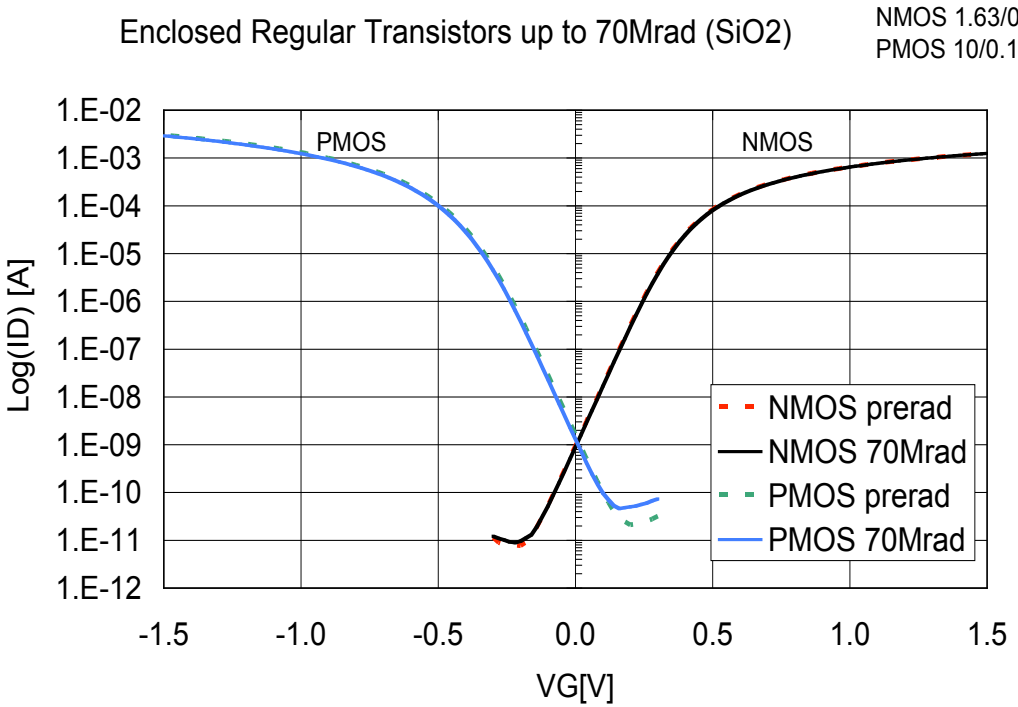
- 0.25µm CMOS probably available until ~2009
  - 0.18µm and 0.13µm already available
    - radiation hardness looks good
    - 300mm wafers next standard, already in use
  - Supply voltage reduction (0.13µm 1.2V/1.5V)
    - challenge for designers
  - Power consumption remains a major issue
    - trend to higher speed and lower power applications
      - but reduced voltages may not imply reduced currents
    - more digital logic possible in smaller area
      - programmable functions to tune, correct, test, debug,…?

0.13µm radiation results



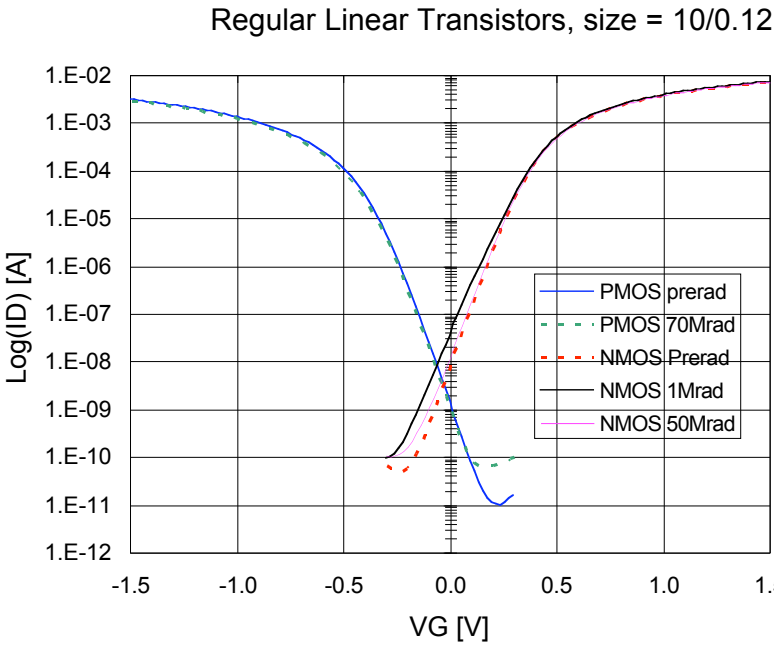
F.Faccio et al CERN

- Not much difference between edgeless and normal transistors



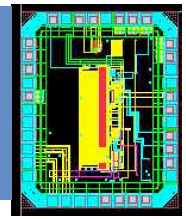
x-ray irradiation

to 70Mrad



- Single Event Effects
  - higher SEU sensitivity
  - SEL not observed

Conclusions



- ASICs are now **vital** for HEP experiments
  - but…
- Electronics technology is still advancing rapidly
  - and we are forced to follow technology trends
- There are huge potential benefits from doing so
- Final thought
  - ASIC technology is undoubtedly expensive
    - foundry cost in Y2000 ~$2B
    - manufacturing increasingly targets major consumers
  - Yet (round figure!) production costs (2005) of
    - CMS Silicon sensor ~10CHF/cm^2
    - CMS 0.25μm ASIC wafer ~10CHF/cm^2

Thanks to many CMS colleagues for data and information