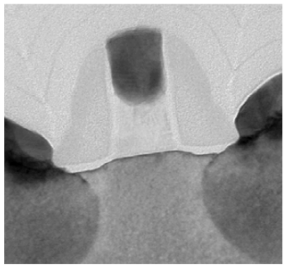
VLSI Technologies for SLHC

Do we need this?



A. Marchioro
CERN – Div. PH

Why not:

- Starting with a base price of ~80K$/Mask set at 250nm, each generation increases in price by about a factor of 2: we can't afford it!
- Difficulty of design increases even faster
  - This is difficult to quantify in HEP, industry quantifies by the single parameter of $/design
- The margin of performance advantage does not increase as fast as desired, in some parameter it even decreases, because technology is approaching intrinsic physical limits in many aspects

Key problems for SLHC

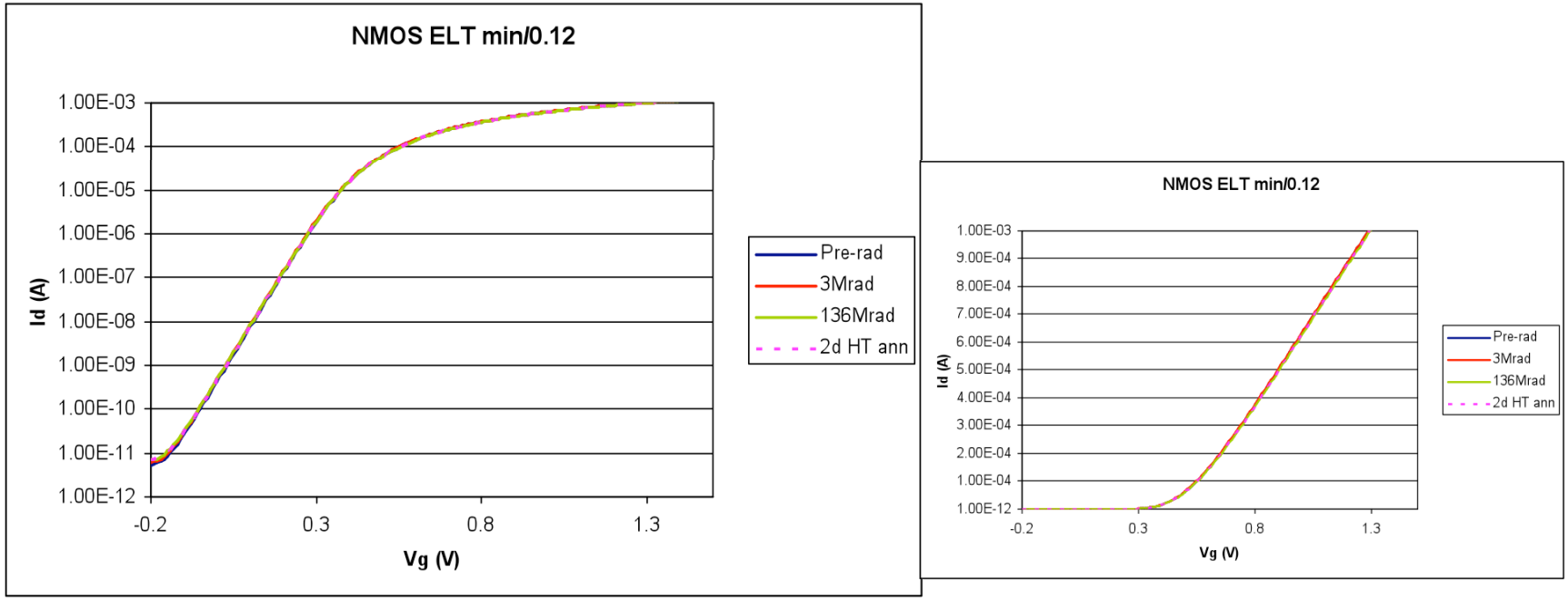
- Reduction of power consumption in FE systems
  - By technology
  - By design (Circuit and architecture)
  - By optimizing power transport to FE
- Low power links
  - Local (< few cm)
  - Long-distance (> 5 m)
- Rad-hard technology for embedded power supplies
- Cost of module/system assembly
  - Avoid "boutique-like" technologies (i.e. use low-cost, high volume packaging and assembly wherever possible)

LHC vs. SLHC

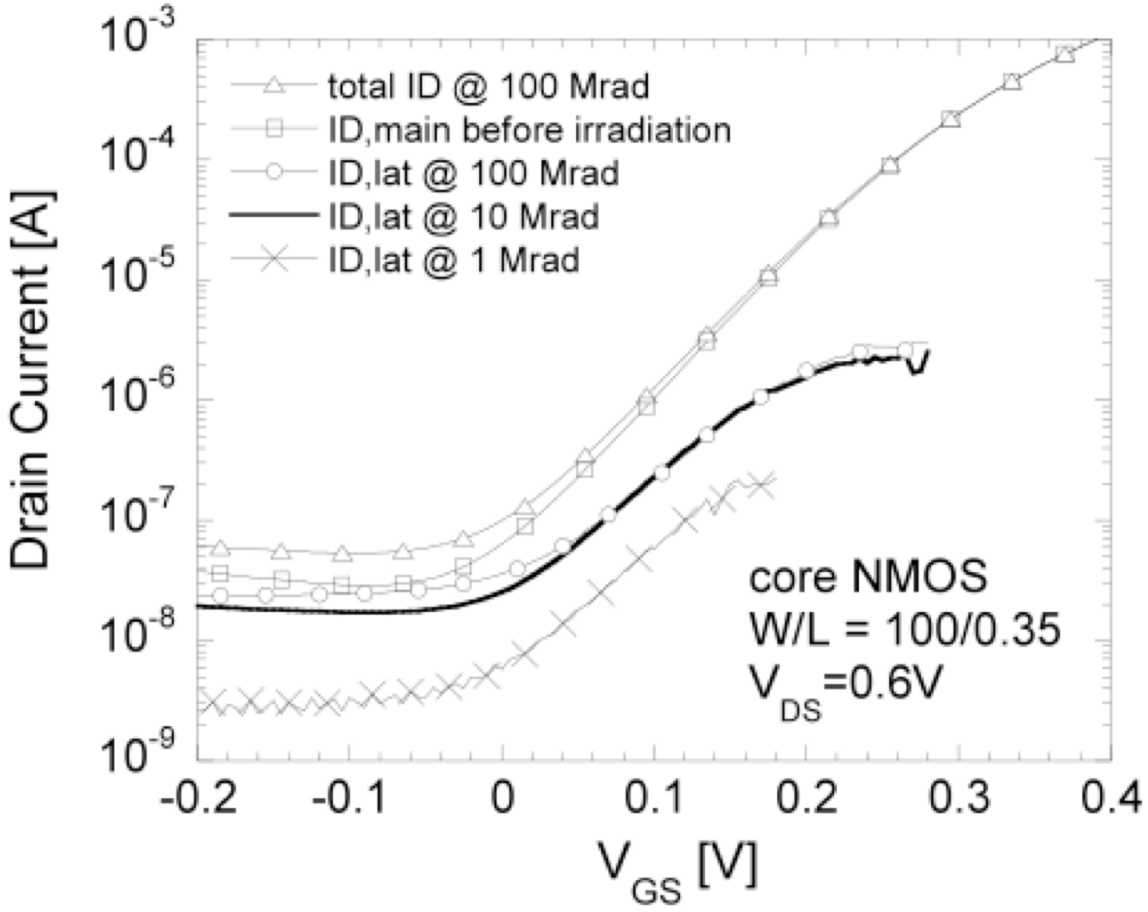
- LHC
  - The radiation hardness age
- SLHC
  - The power efficiency age

130 nm Core transistors, ELT layout

- The 'natural' radiation hardness of the gate oxide for 130 nm devices (in several fabs) is such that practically no effect is observed up to > 100 Mrad

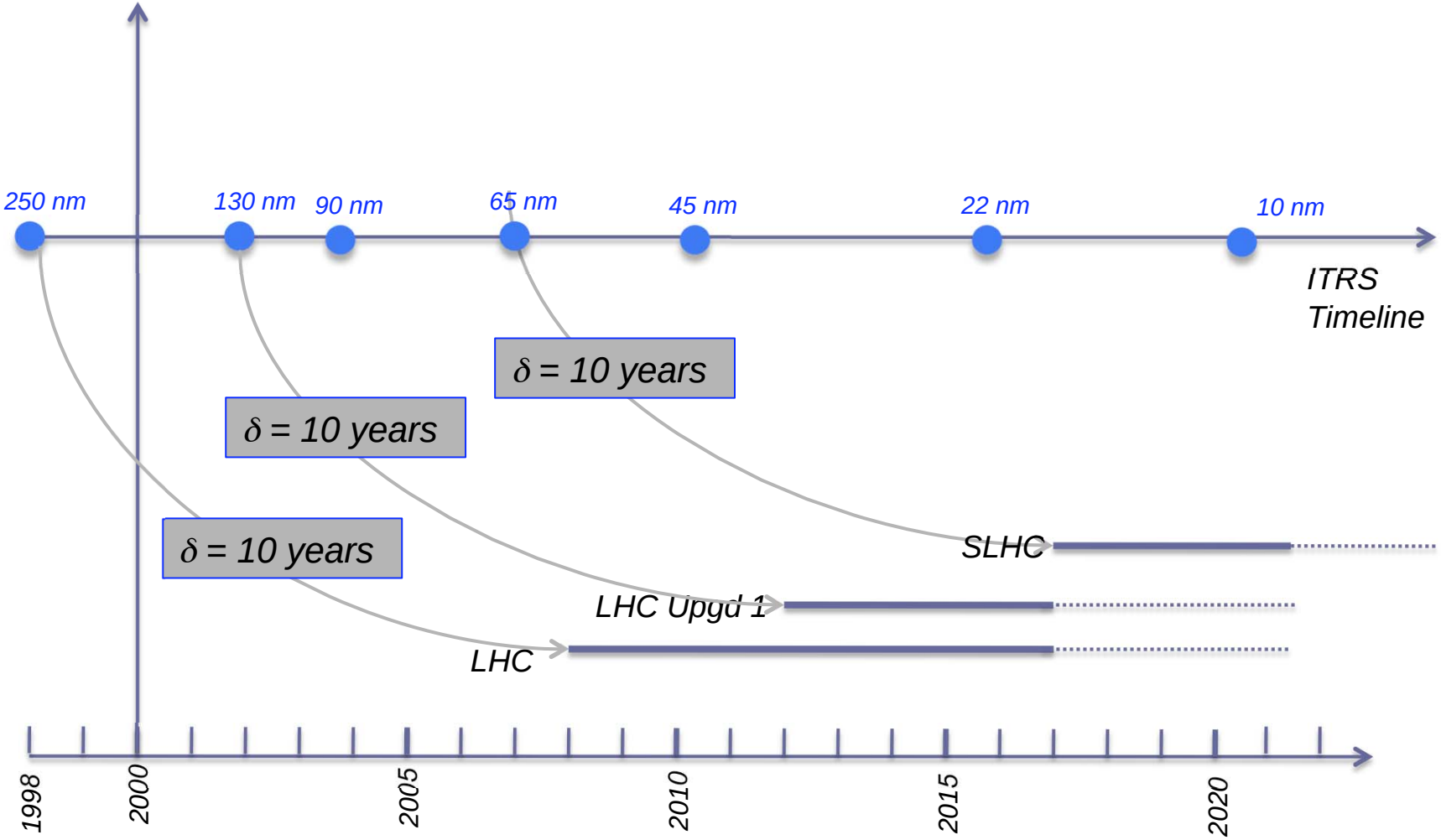


90 nm TID

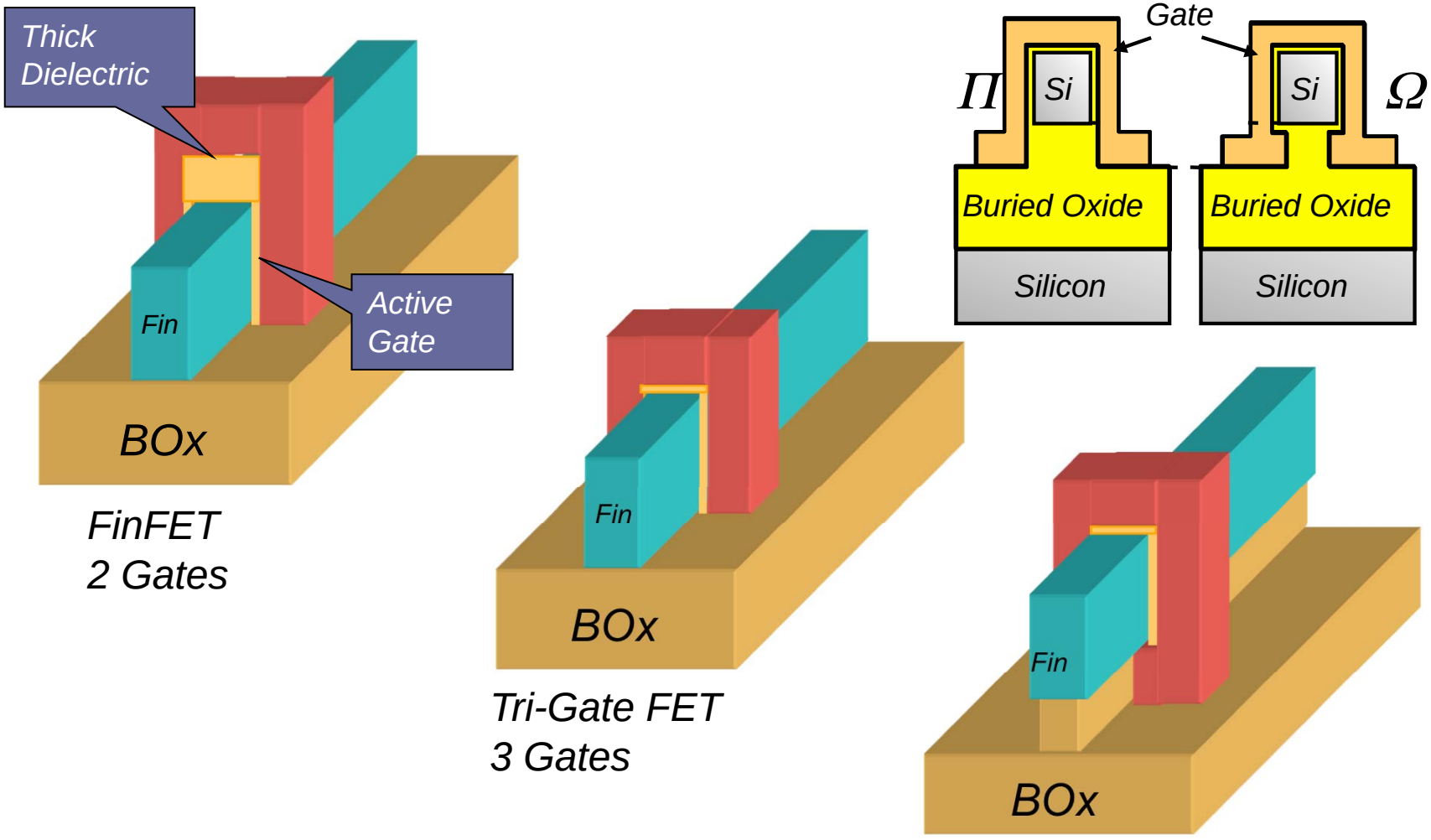


Courtesy of V. Re et al., "Comprehensive Study of Total Ionizing Dose Damage Mechanisms and their Effects on Noise Sources in a 90 nm CMOS Technology", at NSREC 2008

Perspectives

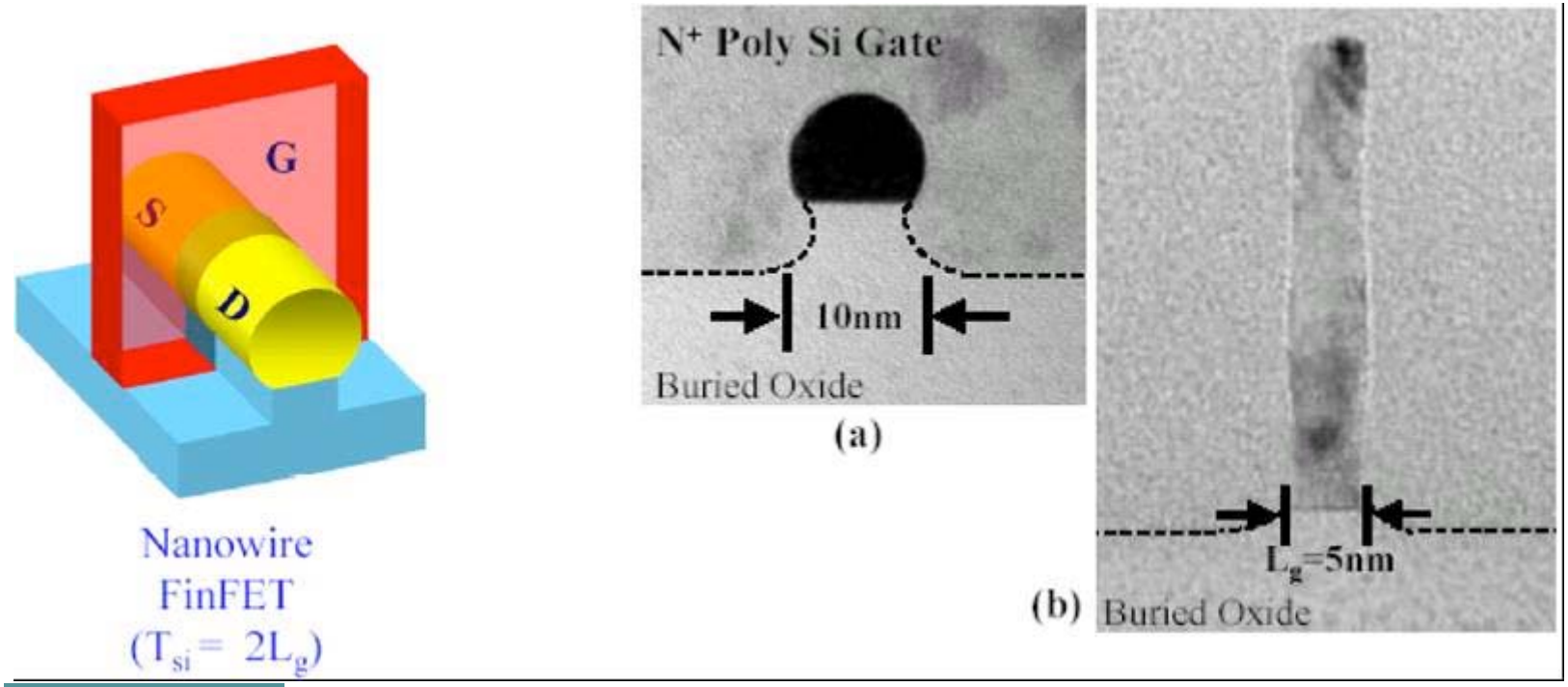


Beyond planar MOSFETS (1)



from R. Doring, TI

Beyond planar MOSFETS (2)



TSMC, 2004

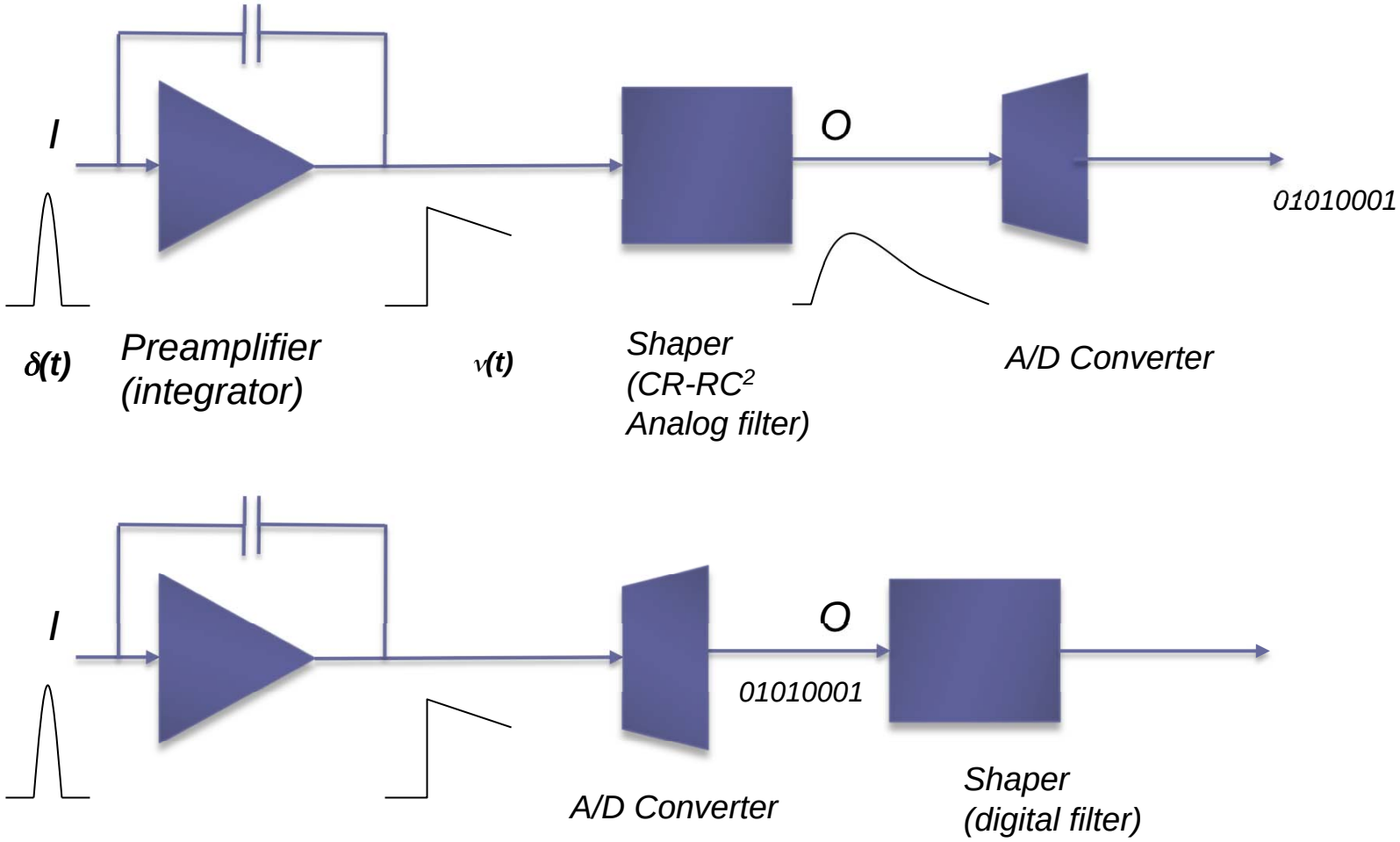
Abstract:
A new nanowire FinFET structure is developed for CMOS device scaling into the sub-10nm regime. Accumulation mode P-FET and inversion mode N-FET with 5 nm and 10nm physical gate length, respectively, are fabricated. N-FET gate delay (CV/I) of 0.22ps and P-FET gate delay of 0.48 ps with excellent subthreshold characteristics are achieved, both with very low off leakage current less than 10 nA/um. Nanowire FinFET device operation is also explored using 3-D full quantum mechanical simulation.

Power Reduction Opportunities

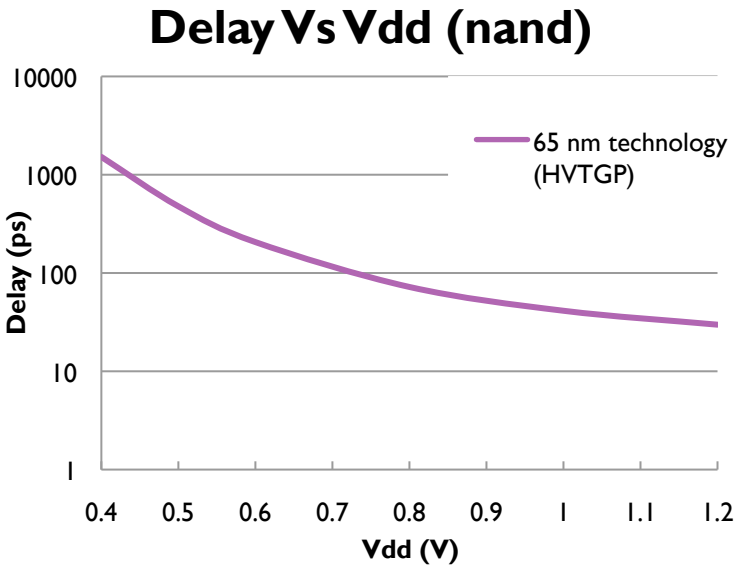
Power reduction opportunities

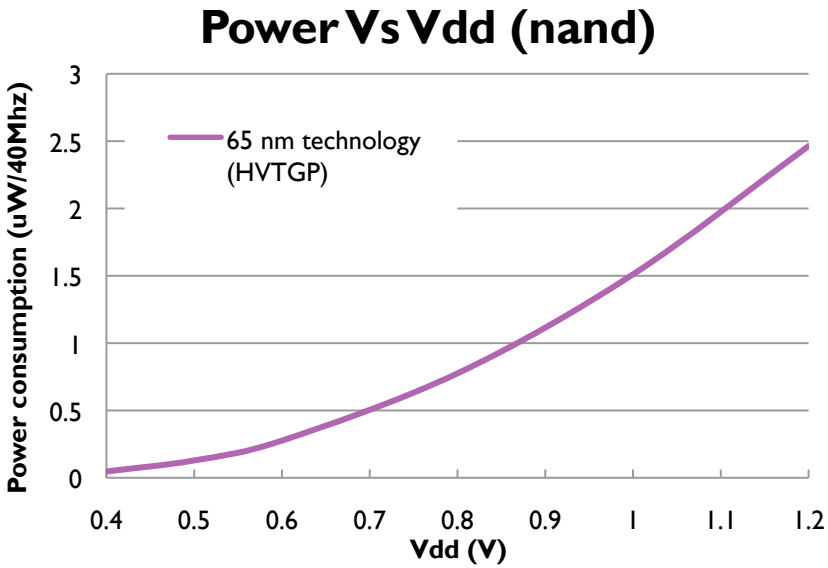
	Analog Circuit (Speed Limited)	Analog (Noise limited)	Digital Circuit
Intrinsic Technology Improvement			
Circuit Improvement			
Architectural Improvement			

Opportunities?

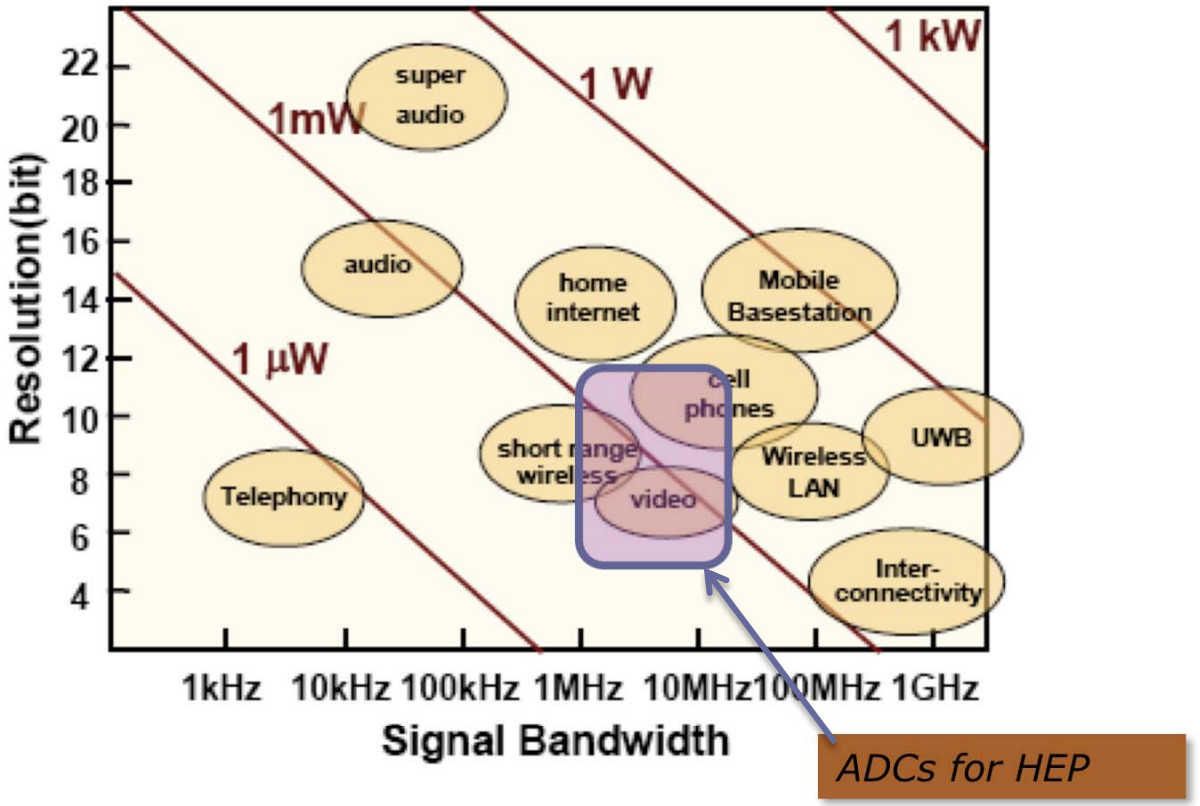


Gains in digital





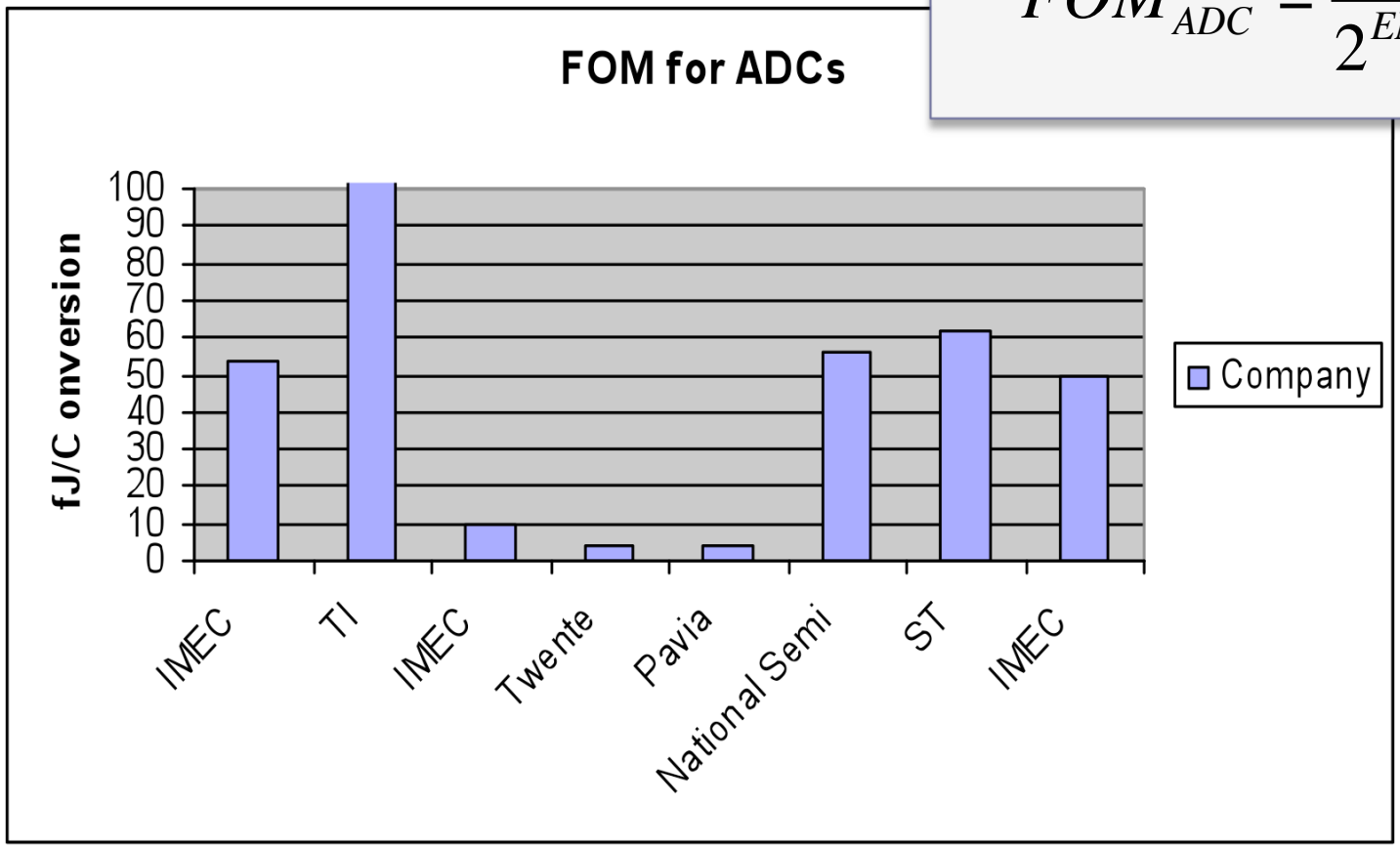
ADC roadmap



From ITRS, 2007

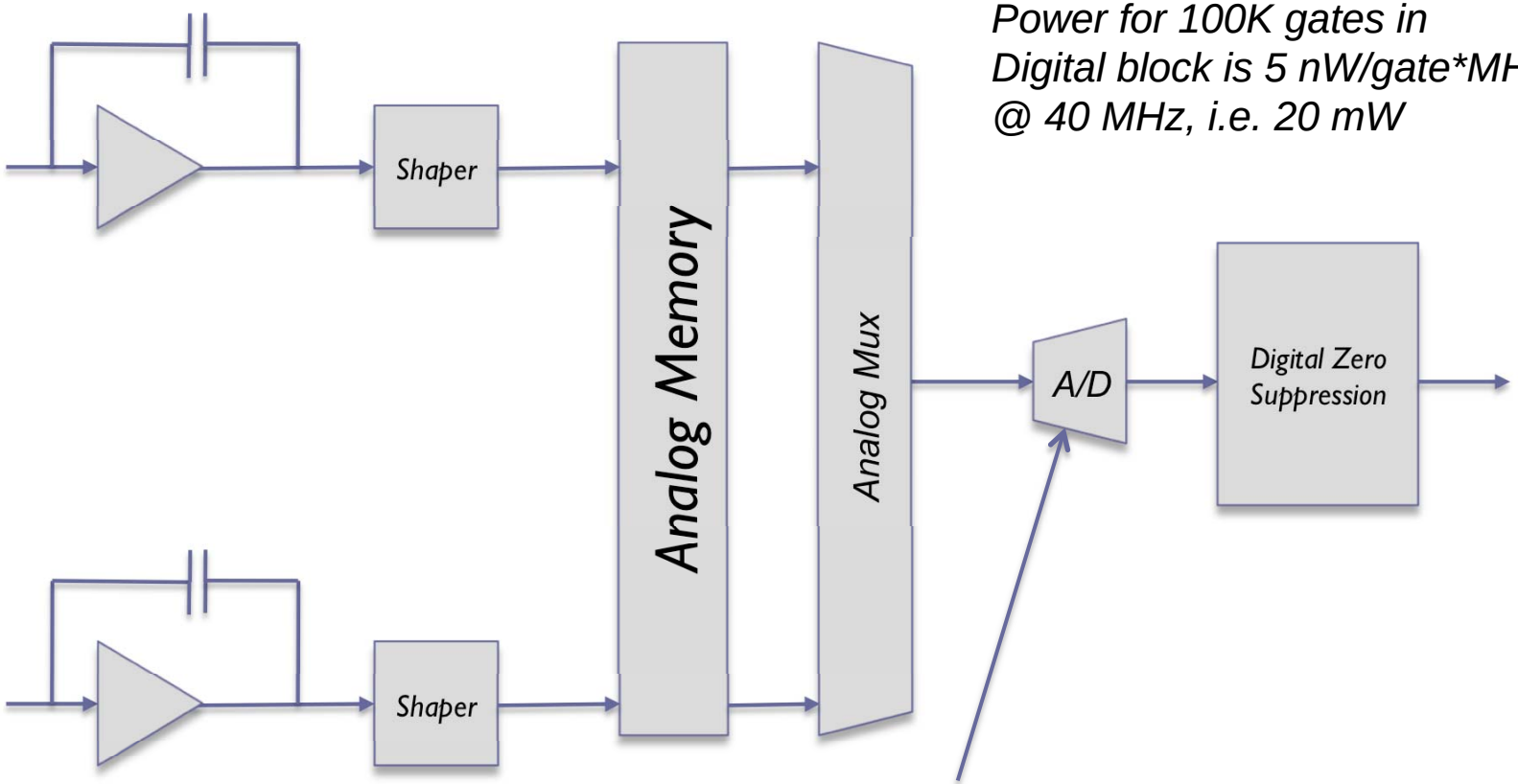
ADC FOM in conference papers 2008

$$FOM_{ADC} = \frac{PWR}{2^{ENOB} f_S} \quad [J]$$



Most designs in 90 and 65 nm

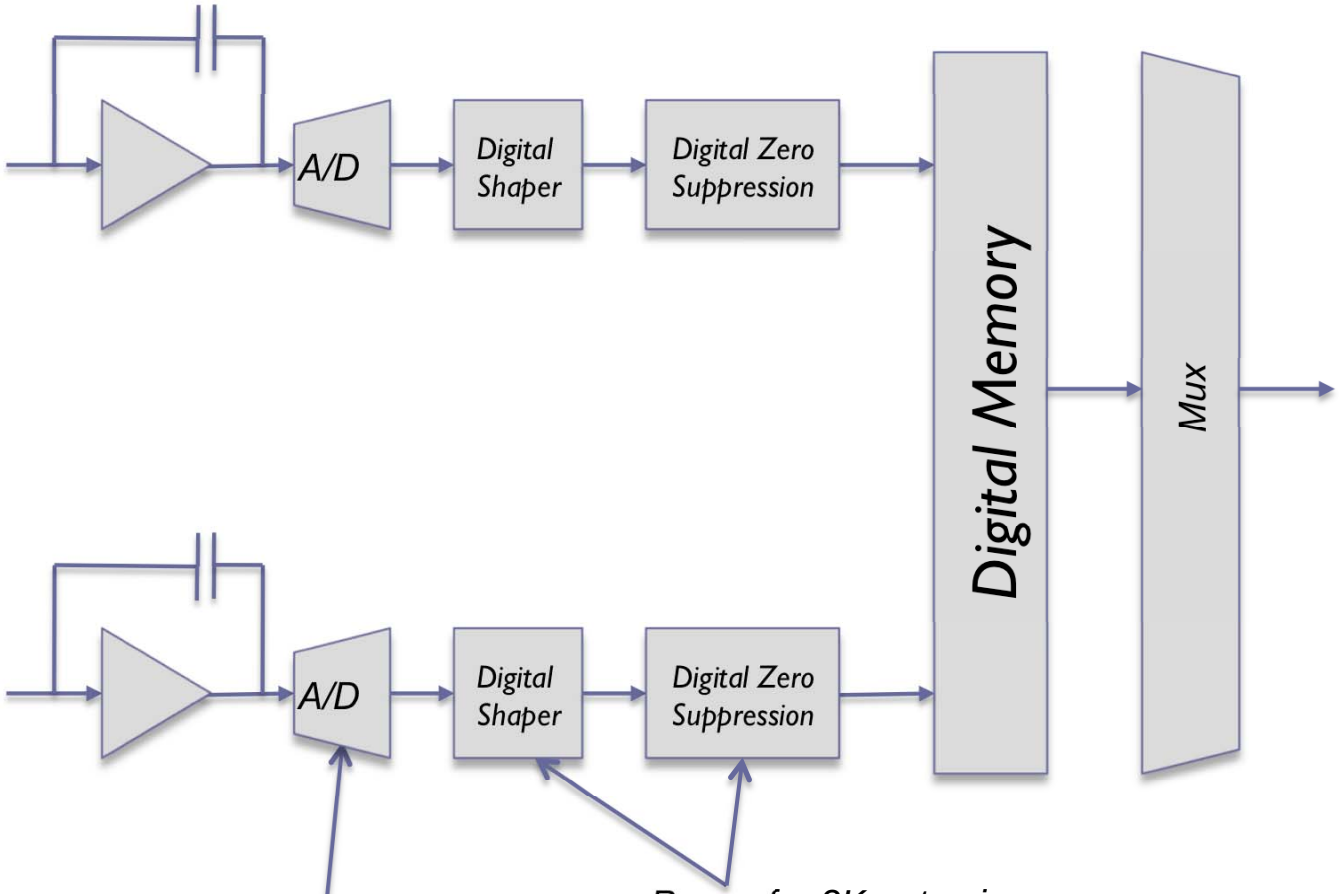
A possible Si Strip Read-Out chip



*Power for 100K gates in Digital block is 5 nW/gate*MHz @ 40 MHz, i.e. 20 mW*

Power for 10 bit AD @ 40 MS/s: ~ 2 mW

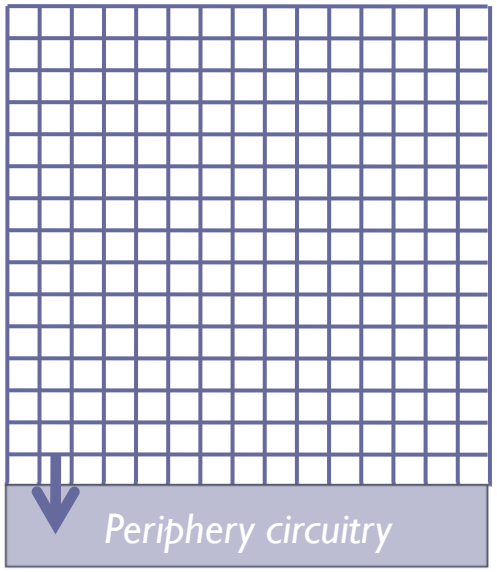
Another possible Si Strip Read-Out chip



Integrated Sensor/Detector

- (see talk of W. Snoeys)
- 90 nm allows new solutions
  - Sufficient charge collection depth to integrate a fully monolithic pixel with good S/N
  - Dense enough metal interconnect structure for innovative FE circuit architecture
  - Low power for digital as to implement trigger primitives, proper and reliable serialization protocol

Dense metals, low-K dielectric



Metalization has to accommodate
~100 signals within ~100 um cells pitch

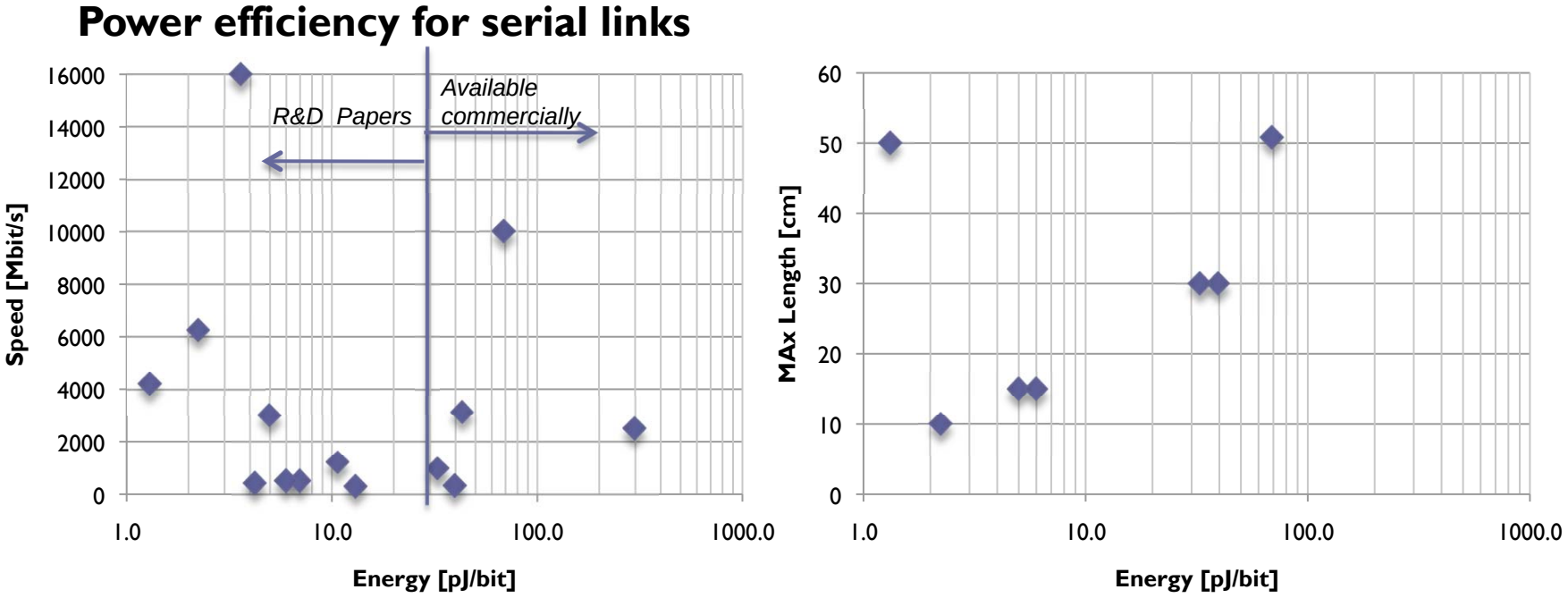
- Wire to wire capacitance reduction through use of Low-K dielectric starting at 90 nm:
  - $\varepsilon_{Low\text{-}K}$ ~ 65-75% of normal oxide ε

Opportunities for links

- GBT (or similar) in 130 nm
  - Max TX rate: 5 Gbit/sec
  - Number of fibers: "N"
  - Power: "P"
- GBT in 90/65 nm
  - Max TX rate: 10 Gbit/sec
  - Number of fibers: N/2
  - Power: < P
- Cost of "opto" part for link 200-250 USD
- Cost for 20K chips in 90 nm:
  - (2 MPW + 1 Mask set + 25 wafers: (150K+600K+100K)/20K = 42 USD/chip
  - If 40K chips, 1 GBT90 costs ~ 24 USD

Local links

- Connectivity at the 1 to 20 mm level for trigger primitives
  - Issue: power



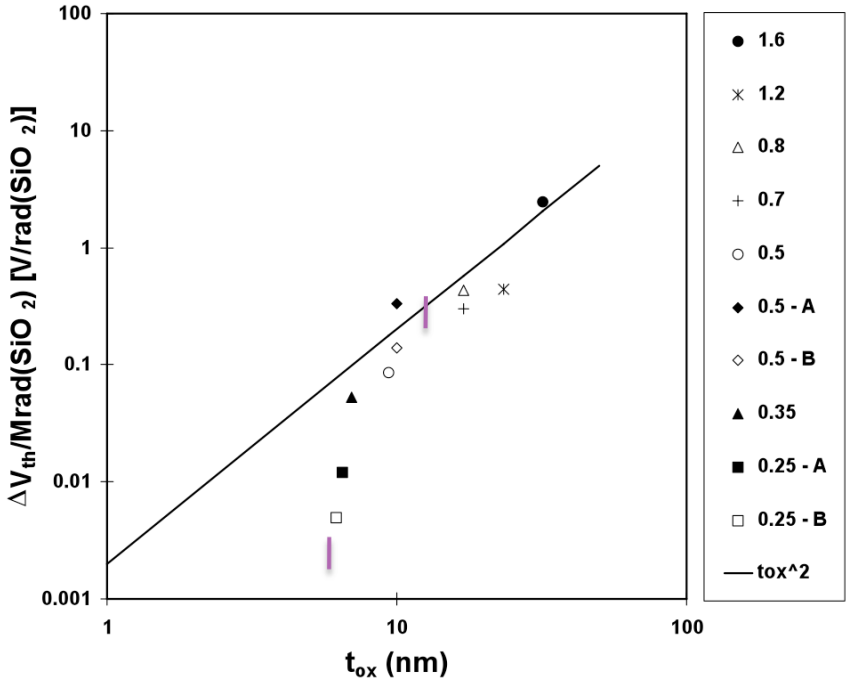
A possible scenario for new e-Cal

- 100K channels
- ADC: 4 ADC @80 Ms/s, 12 bit (assume 12.5 ns BX rate)
  - Power = 4 * 8 mW = 32 mW (500 mW now)
- Local digital processing (a' la Fenix):
  - 1M gates @ 40 MHz (@1V Vdd, 5 nW/MHz): 200mW, to be compared with 650mW now
- Links:
  - @ 90 nm, a 10Gbit/sec could take ~ 2 W (now 3W), but reduce the number of fibers by ~5-10
  - What was the installation cost of the fibers?

… and its cost @90nm

- ADC
  - IP macro: 500K$
  - 1 MPW: 80K$
  - Full Mask Set 600K$
  - 100 Wafers: 400K$
  - **Price/chip: 16$**
- Of course it would be proper to include the preamp-shaper in the same IC
  - Move the shaping to the digital world
- Fenix2 (20 K parts):
  - 1 MPW 80K$
  - Full mask set 600 K$
  - 25 wafers 100 K$
  - **Price/chip 40$**
- If ADC and Fenix combined on same mask set (assume 4 ADC/1 Fenix):
  - IP macro: 500K$
  - 2 MPW: 160K$
  - Full Mask Set 600K$
  - 125 Wafers: 500K$
  - **Price/chip: 18$**

Power Devices for DC-DC Converters



N.S. Saks et al., IEEE TNS, Dec. 1984 and Dec. 1986

	Tech α	Tech α'	Tech β
T_{ox} [nm]	4.5	12.5	12
V_{gs} [V]	1.8	5.5	5.5
V_{ds} [V]	20	25	20

All these technologies are derived from a 180nm base lithography

Problems to expect

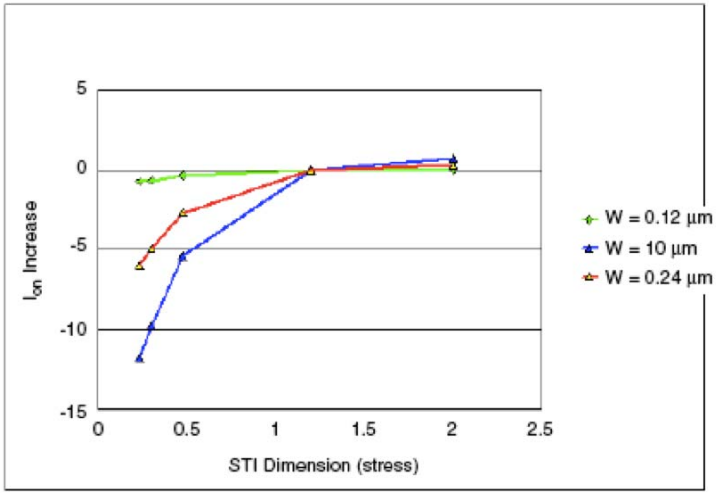
New complexities

- Gains in the analog world are limited
  - Think about moving more processing in the digital world
  - Think system and not FE transistor
- Process has more variability
  - Designers need to cover more thoroughly process corners, in some cases correct digitally
- Design complexity (tools etc.) considerably more complicated:
    - statistical matching across chips, wafers, lots
    - metal filling
    - design methodology for AMS
    - multiple separate power domains
  - Use commercial support, don't reinvent in HEP

Design Complexity

- Size of design manual (trivia)
  - 250 nm: 157 pages, 1 manual
  - 130 nm : 460 pages, 1 manual
  - 90 nm : 1149 pages, 4 manuals

- STI induced MOSFET variation



Examples of process variability

- Spatial
  - Within chip
    - Proximity effects
    - Orientation
    - Local stress (transistor's parameters depend on very local physical effects)
    - Large "analog" content in today's HEP chips
  - Across chips
    - Exposure inaccuracy
    - CMP
  - Across wafers
    - Processing effects on lot and across lots
    - Process stability on small lots (likely for us!)

More process variability

- Temporal
  - Parameters change in time (on very different time constants) due to:
    - Transistor wear-out
      - NBTI for PMOS
      - Hot Electrons for NMOS
    - Metalization wear-out
      - Electromigration
    - Local electrical conditions (short term charging effects)
    - Intrinsic
      - Doping with few 100 atoms has natural Poisson distribution
    - Environmental
      - Temperature
      - Radiation

Don’t panic

Looking ahead through an excellent conference paper

A 45nm Logic Technology with High-k+Metal Gate Transistors, Strained Silicon, 9 Cu Interconnect Layers, 193nm Dry Patterning, and 100% Pb-free Packaging

K. Mistry, C. Allen, C. Auth, B. Beattie, D. Bergstrom, M. Bost, M. Brazier, M. Buehler, A. Cappellani, R. Chau*, C.-H. Choi, G. Ding, K. Fischer, T. Ghani, R. Grover, W. Han, D. Hanken, M. Hattendorf, J. He#, J. Hicks#, R. Huessner, D. Ingerly, P. Jain, R. James, L. Jong, S. Joshi, C. Kenyon, K. Kuhn, K. Lee, H. Liu, J. Maiz#, B. McIntyre, P. Moon, J. Neirynck, S. Pae#, C. Parker, D. Parsons, C. Prasad#, L. Pipes, M. Prince, P. Ranade, T. Reynolds, J. Sandford, L. Shifren%, J. Sebastian, J. Seiple, D. Simon, S. Sivakumar, P. Smith, C. Thomas, T. Troeger, P. Vandervoorn, S. Williams, K. Zawadzki

Logic Technology Development, *Components Research, #QRE, %TCAD, Intel Corp., Hillsboro, OR, U.S.A.

ABSTRACT

A 45nm logic technology is described that for the first time incorporates high-k + metal gate transistors in a high volume manufacturing process. The transistors feature 1.0nm EOT high-k gate dielectric, dual band edge workfunction metal gates and third generation strained silicon, resulting in the highest drive currents yet reported for NMOS and PMOS. The technology also features trench contact based local routing, 9 layers of copper interconnect with low-k ILD, low cost 193nm dry patterning, and 100% Pb-free packaging. Process yield, performance and reliability are demonstrated on 153Mb SRAM arrays with SRAM cell size of 0.346μm^2, and on multiple microprocessors.

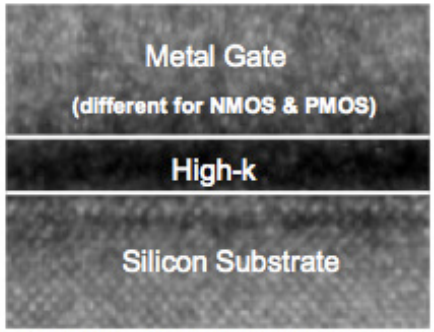


Fig. 2 TEM of High-k + Metal Gate transistor stack

Paper published by Intel at IEDM 2007

Conclusion

- Technology alone is NOT "the solution" for better instruments in SLHC
- Combination of:
  - Adequate and "standard" technologies (not only in microelectronics, low cost packaging and assembly is probably just as important)
  - New architectures
  - System engineering


Thank you!