Forschungszentrum Karlsruhe
in der Helmholtz-Gemeinschaft
Institute for Data Processing and Electronic

Packaging Technology for the ALICE Transition Radiation Detector

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Why IPE?
What's the task?
Where's the problem?
What we learn for packaging?

Centre for packaging since 2001

160 m² gray room

SMD production line:
picker&placer,
vapour solder oven,
automatic needle tester,
tests, repair

140 m² clean room
class 100 000 (measured 5000**)**

... **for batch production and R&D for hybrid micro-systems (packaging):**

e.g. vibration sensor,
micro-spectrometer,
electronic gas sensors,
ALICE, …

Task for transition radiation detector

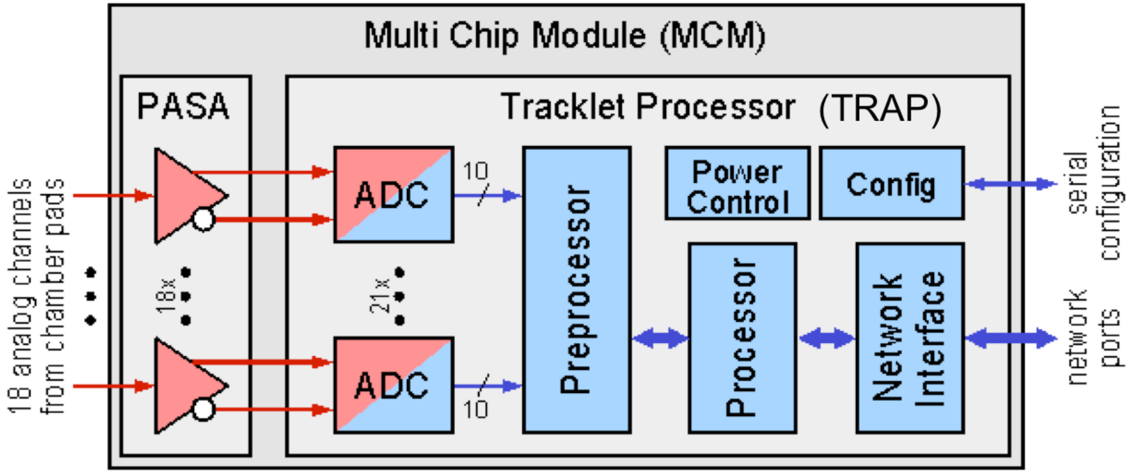
- **High data rate: 15.7 TBd**
- **$1.2*10^6$ data sources**
- **Tracking of up to 16 000 charged particles**
- Manageable connectivity -> **data reduction**

Chip farm at frontend

Packaging of chips as thin as possible

2 chips integrated in one Multi-Chip Module
serving 18 analogue channels
16 + 1 MCM's for one readout board

PASA=Pre- and Shaper-Amplifier



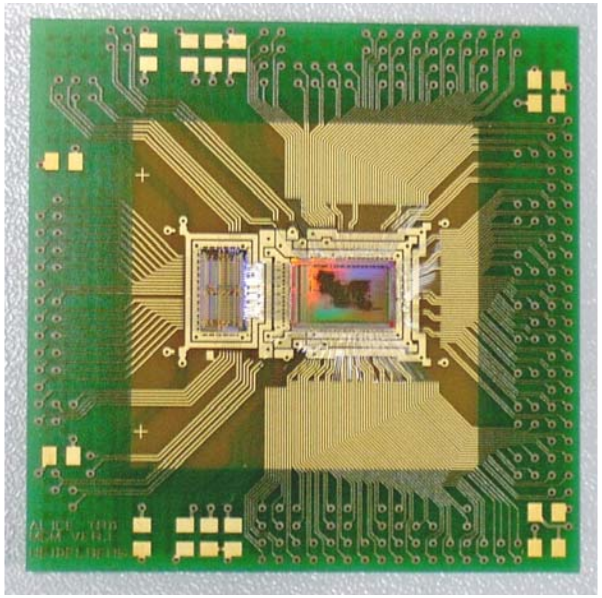
Where is the problem for packaging ???

- **65664 ball bonded MCM's**
- **Each MCM with 432 balls and 460 wire bonds,** 30 000 000 balls and 60 000 000 bonds
- **bonds connecting different height levels:**
  - chip - chip
  - chip - PCB
- **very thin (<1mm) printed circuit boards** for **MCM** and **read-out board**
- Should cost "nothing"

yield of production

warpage

Size 41∗41 mm^2



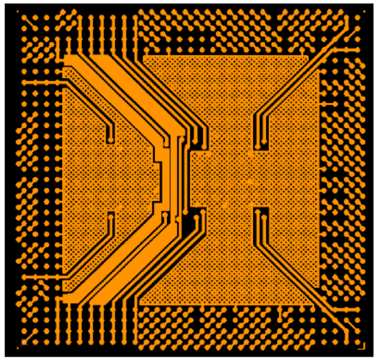
Processing steps for MCM

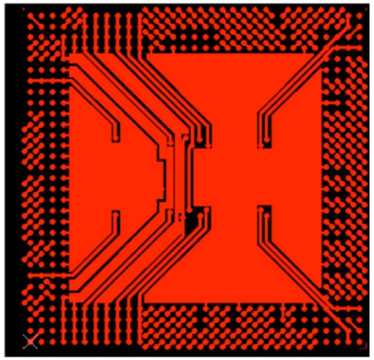
- Optimization of PCB parameters
- Die attachment
- Wire bonding
- Glob top
- Balling
- Quality control of balling
- Electr(on)ical tests of MCM’s

MCM: optimisation of PCB

Problem: as thin as possible and no warpage

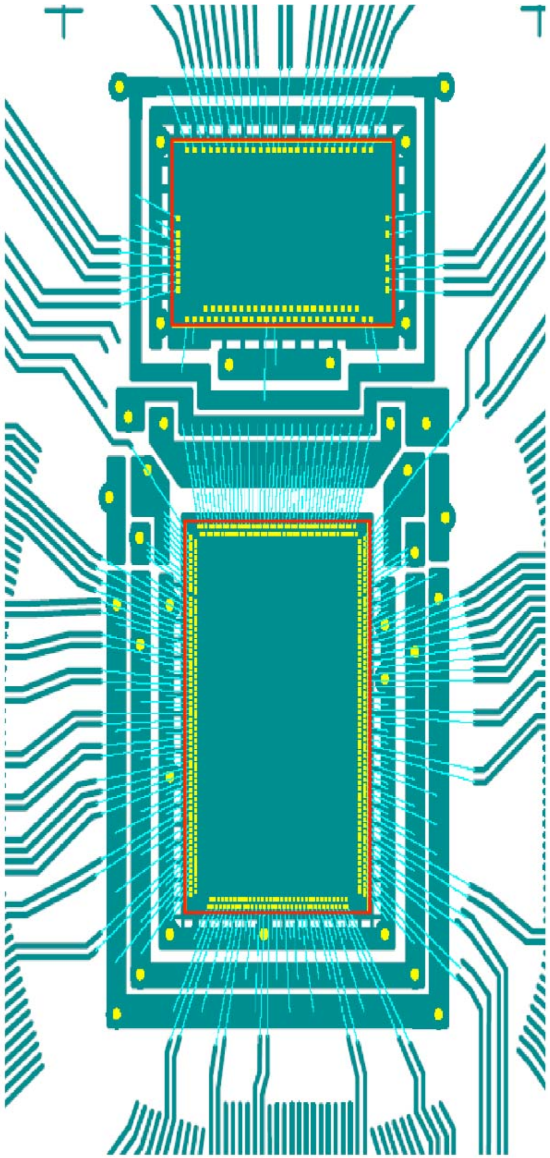
- **Normal material (FR4) has glass transition temperature of $T_g \approx 120°C$**
- **Curing the glob top needs 150°C**
- **Isola Duraver 117 has a T_g > 160°C**
- **Tests with Boards of 0.8 and 1.0 mm thickness**
- **meshed and solid version of ground layer**



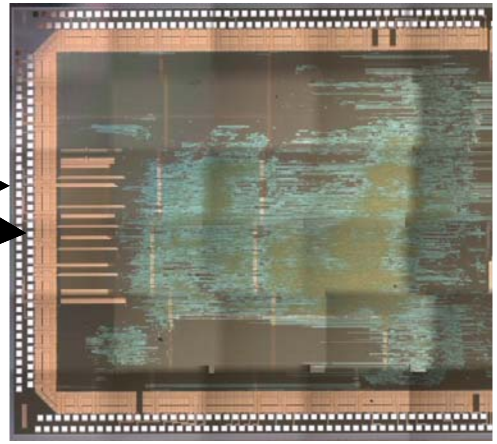


MCM: Die attachment

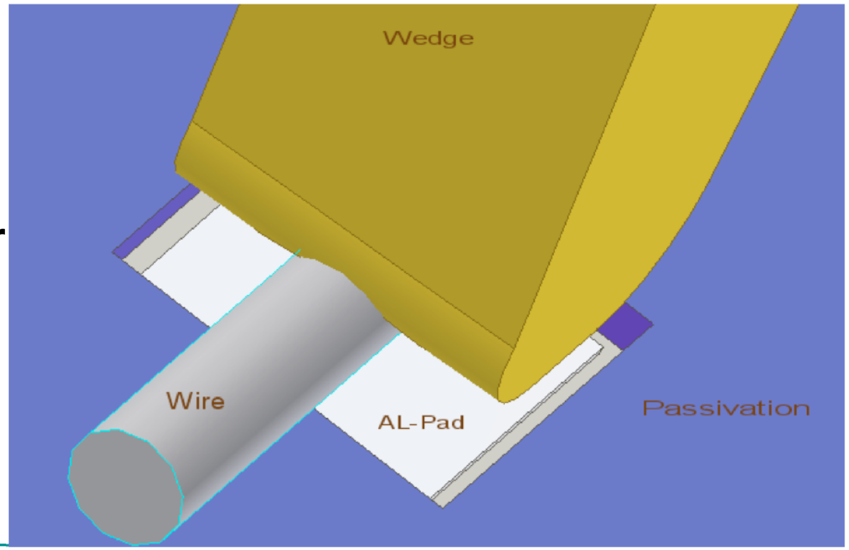
- **TRAP-Chip 7.4∗5.0 mm²**
  PASA-Chip 5.5∗3.4 mm²
- **Silver glue for attachment to ground**
- **both chips as near as possible together for cross links**
- **Problems:**
  - squeeze out of glue may give short circuits
  - Positioning of chips < ± 60 µm
  - warpage by curing **(20 min at 120°C)**
- **Solution (for 0.8 and 1 mm PCB):**
  - Screen printing - not dispensing glue
  - Definition of a critical distance between landing of chip and next printed wire (150 µm)
  - Best for warpage: meshed ground plane



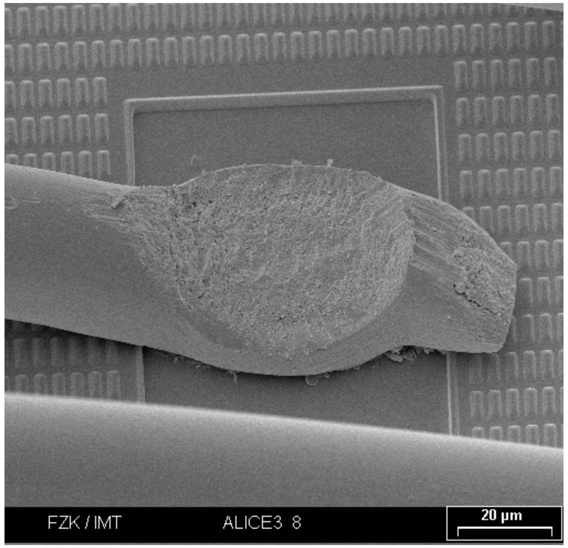
Wire bonding



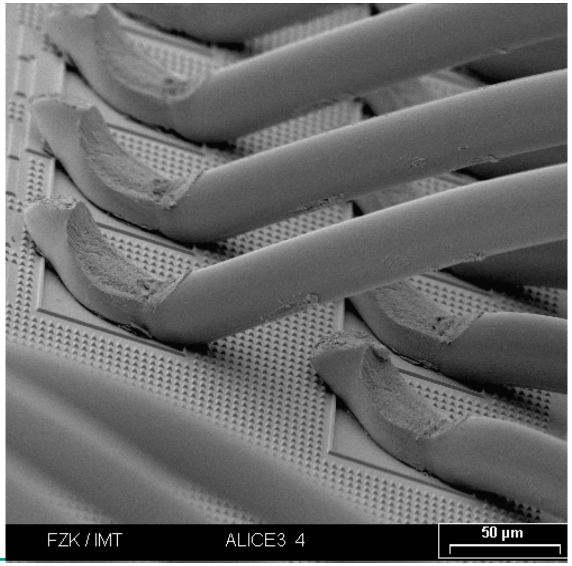
- **Bond pads of the chips 70 x 70 μm², pitch 110 μm, and staggered in 2 rows**
- **Caveats:**
  - **The wedge size have to fit to the size of the pad - otherwise passivation leads to poor joints**
  - **Position tolerance t (4σ) of bond head (t_{IPE} ≈ 6μm)**
  - **Select wire diameter w (22.5 - 25 μm)**
    optimal wire diameter:
    pad size - 2·t > bond length ≈ 2.4·w
  - **Tolerance of bond position may be larger at edges of bond field!!**



Wire bonding

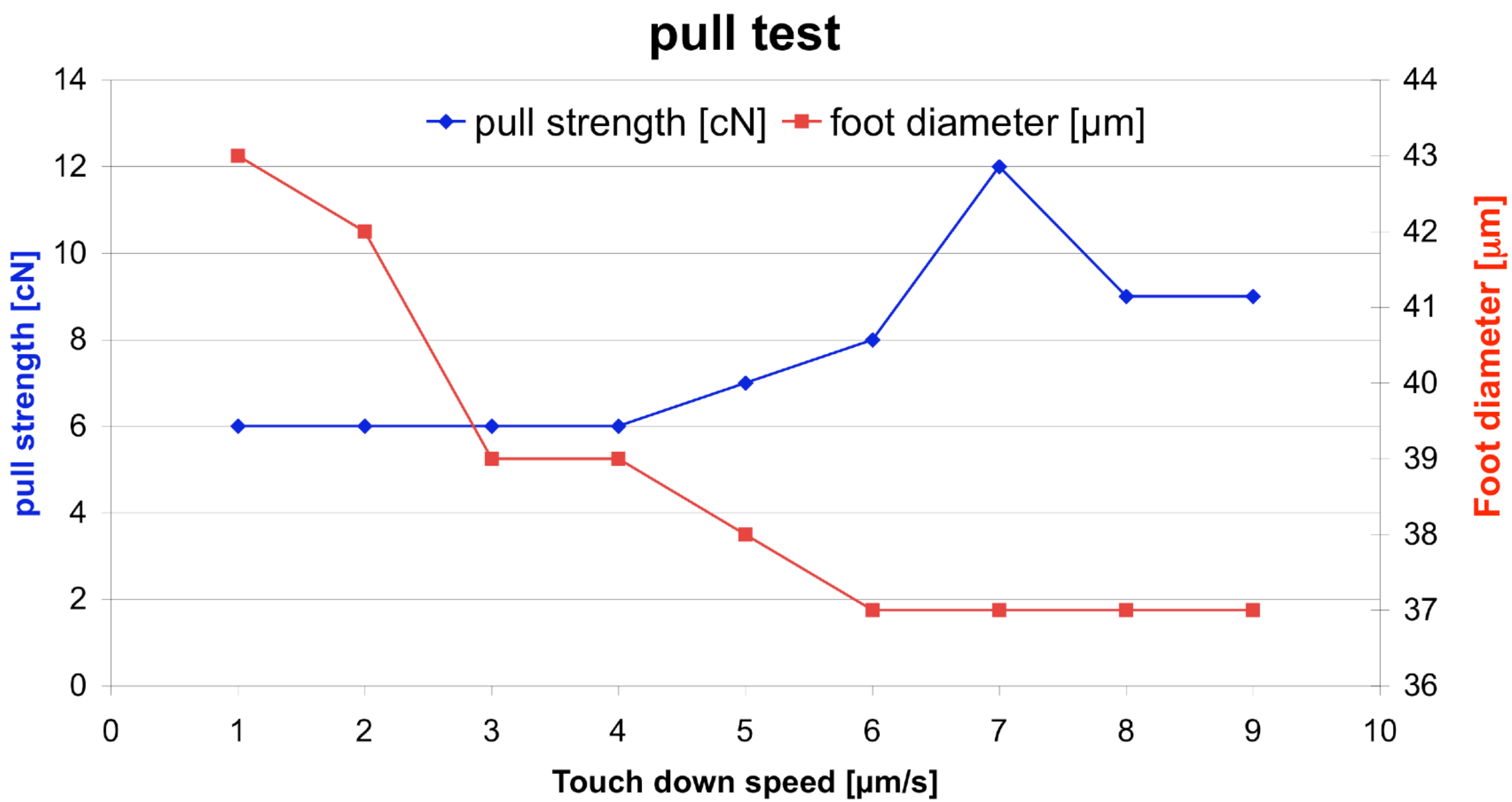


- **Some typical bonds on the TRAP chip**
- **Also exact double row bonding**
- **Many more parameters define the bond process:**
  - Speed of bond head at touch down
  - Used Ultra Sound power for bonding
  - Elasticity of bond pad support (PCB or Si)
  - Bond angle
  - Size of wire loop, . . .
- **Especially complicated for bonds over different heights: chip - chip, chip - PCB and different materials**
- **Individual optimisation is necessary!**
  - **New bond control:** measuring the bond resonance parameters and regulating the US-power!!!



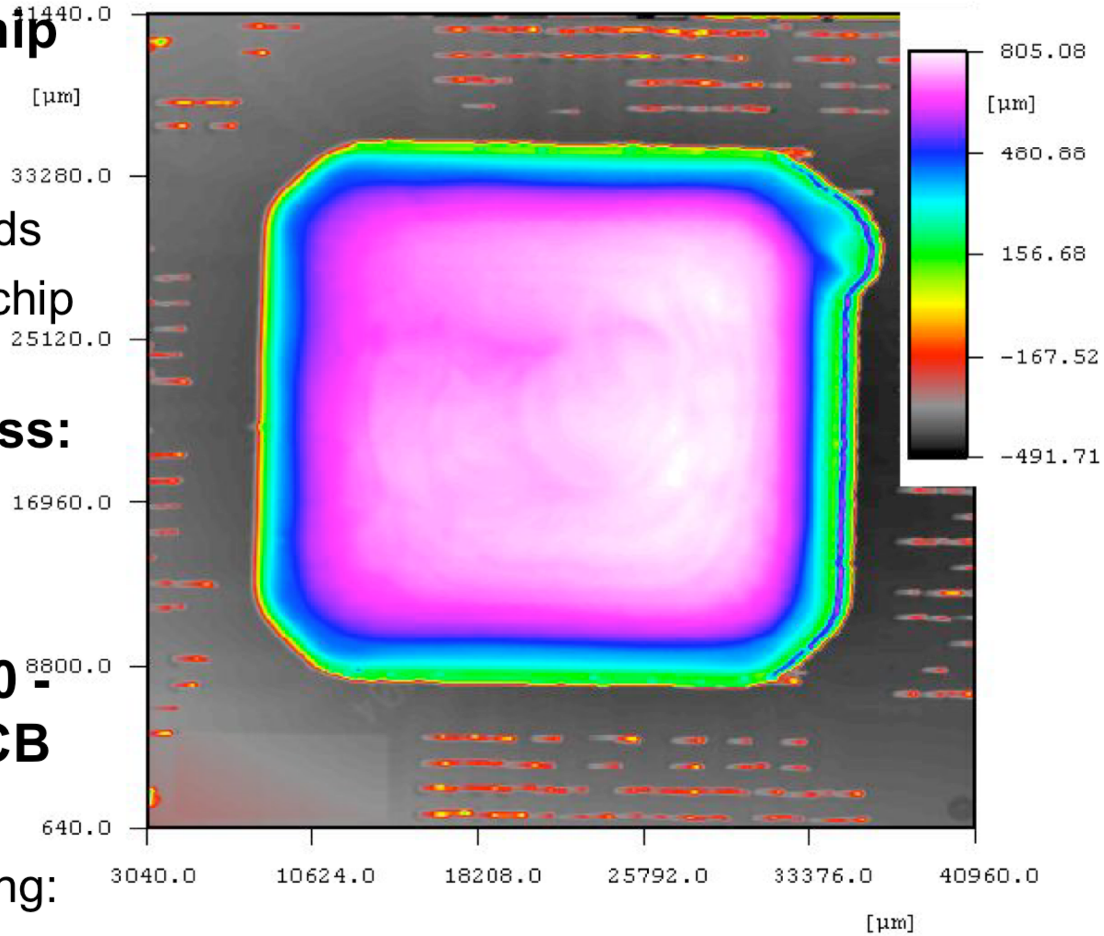
Destructive bond testing with pull tester

- **bond strength for TRAP chip and 25 μm Al bonds 10±2 cN**



MCM: Glob Top

- **Protecting the bonds and the chip**
  - Medium coefficient of thermal expansion (80 ppm)
  - but low E-modulus protecting bonds
  - small max. particle size (pitch on chip is 110 μm)
- **Recommended minimal thickness:**
  300 μm chip height +
  250 μm bond loop height +
  250 μm protective top layer
- **Problem warpage by curing (120 - 150 °C) -> layout changes on PCB**
  - Now warpage < 100 μm:
  - Could be compensated by soldering: reduces height of balls by 300 μm

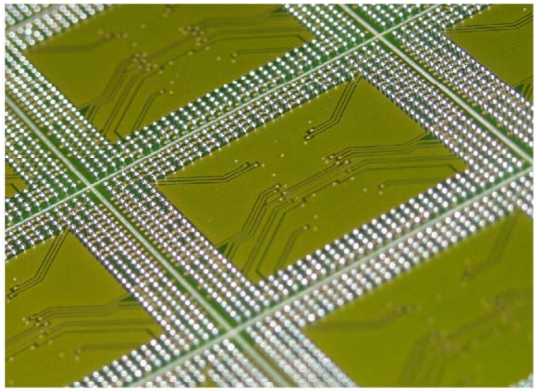


MCM: Balling

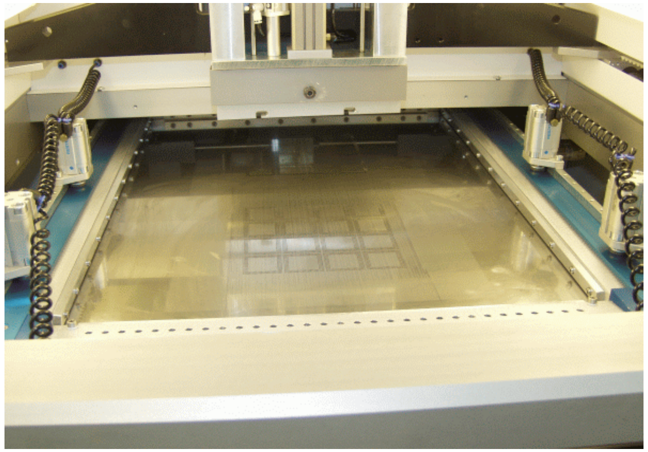
1. **Flux (Solder Paste)**
   - Screen (Stencil)
   - Pin transfer
   - Dispenser
   - Flux jet
2. **Ball placement**
   - Gravity transfer
   - Vacuum transfer
   - Solder jet
   - Screen paste
   - Dispense paste
3. **Inspection**
   - Ball count
   - Location
   - Quality
4. **Reflow**
   - IR oven
   - Vapor phase
   - Forced convection

– **Tested and rejected methods**

– **finally adopted method**

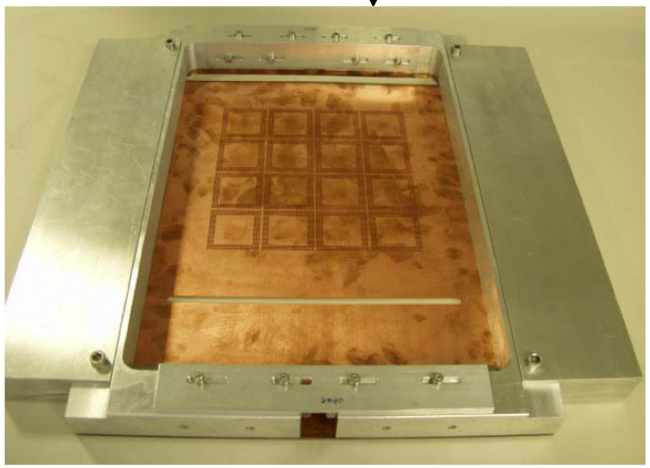


432 balls per MCM,
6912 balls per substrate



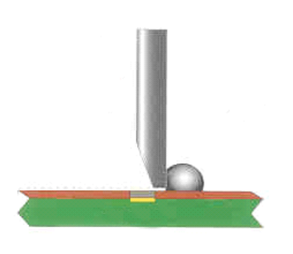
Stencil printer

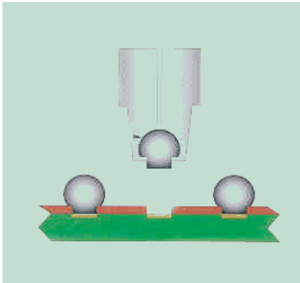
Stencil for ball transfer

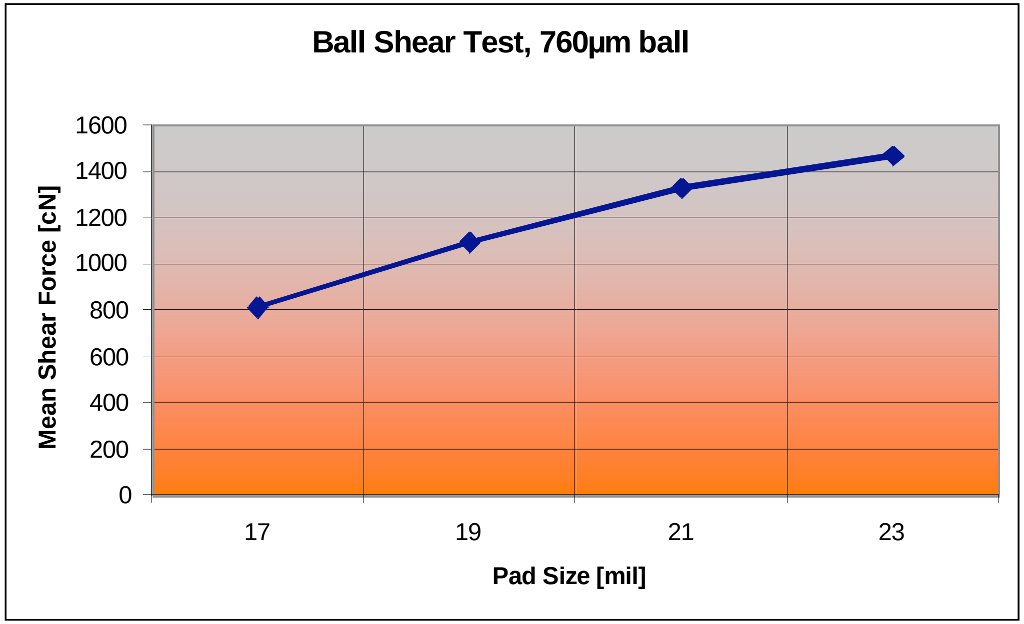


MCM: Quality test of Balling

- Problem at beginning: Low shear forces required to rip balls off



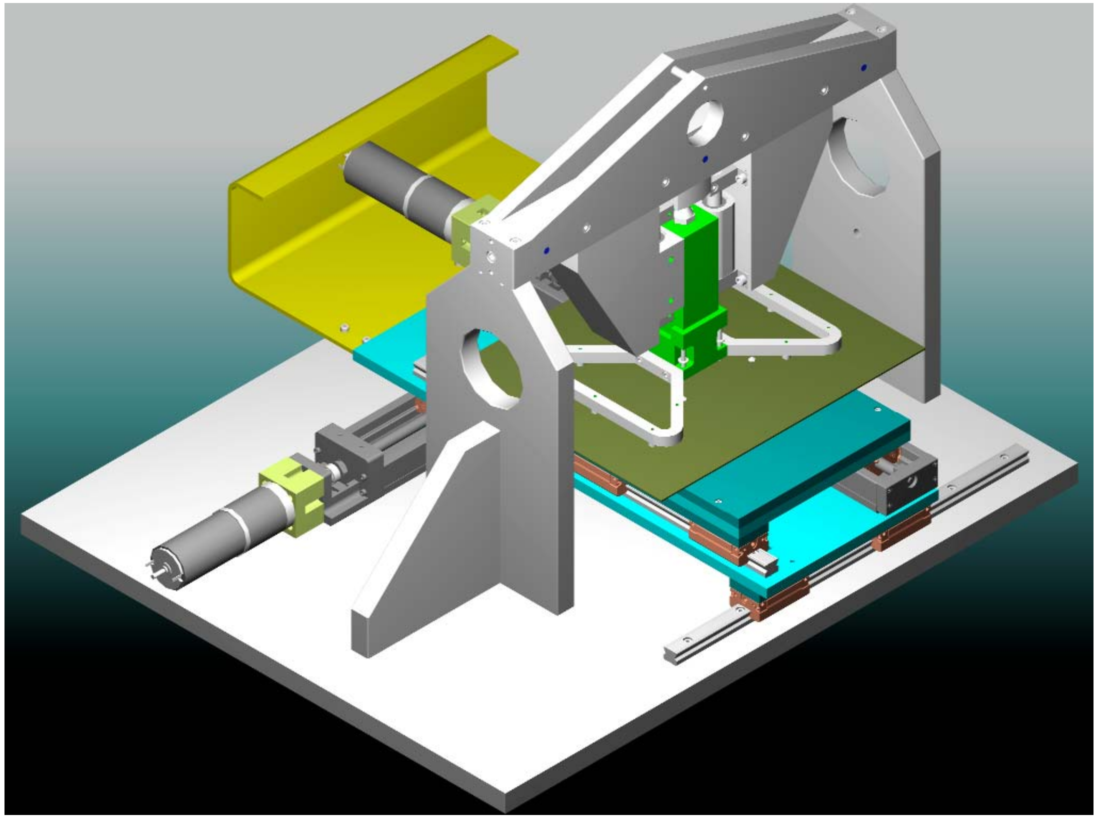




➡ Balls to small, new MCM and ROB layout with increased Pad Size

➡ solder reflow temperature profile and convection air flow !!! (vapor oven and IR-oven not suited for balling)

MCM electronically testing

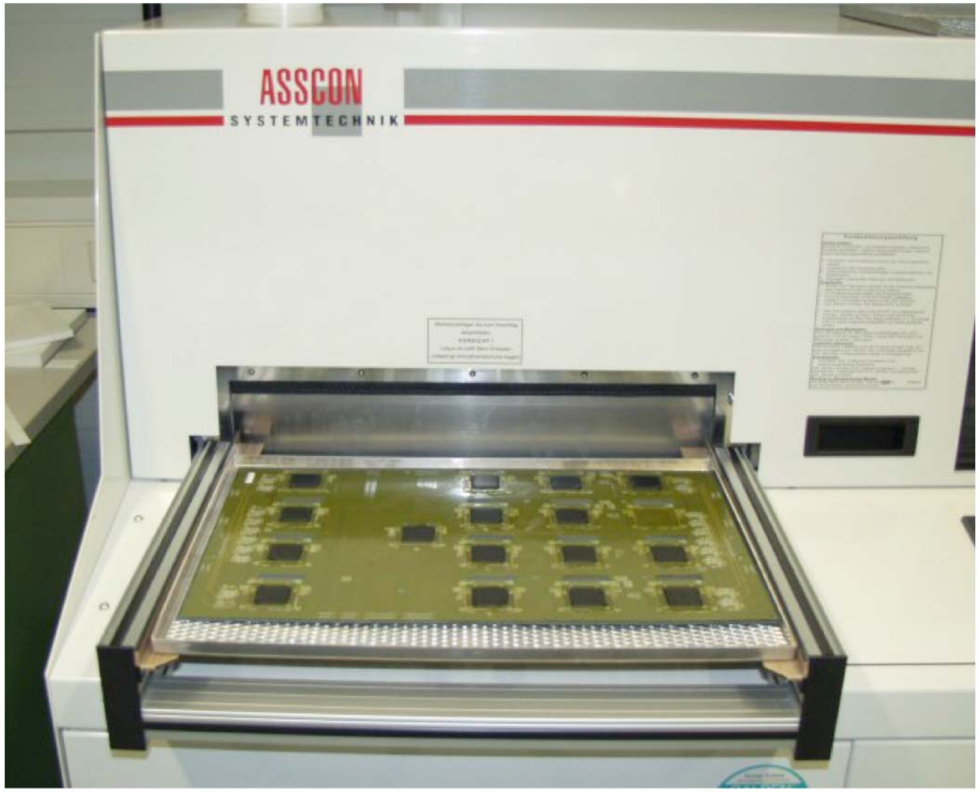


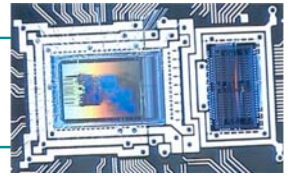
Development of an automatic test-station (finished last week):

- **Test of 16 MCM modules**
- **completely packaged**
- **incl. balls**

Readout board

- **500 ∗ 300 mm^2 and 0.8 - 1 mm thick, ev. new carbon filled PCB**
- **17 MCM's and 1000 passive components**
- **Very delicate handling**
- **Automatic quality test optically and electrically within a SPEA flying needle prober**
- **Electronic tests and burn-in tests are under preparation**





Conclusion

- **We have learned a lot - that was our intention**
  - All processes seems to be under control
  - But tests over large numbers (preproduction run) have to be done
  - Warpage was the critical question
- **Critical law of large numbers**
  - 60 000 000 bonds and 30 000 000 balls
  - What may be going wrong surely goes wrong
  - Disentangling in readout boards and MCM's helped:
    Only 916 bonds and 432 balls -> good yield achievable
- **Design of packaging have normally to be started with chip design**
  - Then the job would have been easier
  - Lower number of design loops