Radiation tests of key components of the ALICE TOF TDC Readout Module

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Abstract

The ALICE Time-of-Flight (TOF) system will be a large area (140 m^2) detector made by Multigap Resistive Plate Chambers (MRPC). The read-out will be performed by a VME TDC Readout Module (TRM) hosting each 30 High Performance TDC chips (HPTDC).

Radiation tests carried out at Zurich PSI with a 60 MeV proton beam line on key components of the TRM (FPGA, RAM, Flash memory, voltage regulators, microcontroller and others) are described, with an emphasis on the validation of the watchdog mechanisms of SEU events, as well as protection from latchups. In particular, an Altera Stratix (0.13 CMOS technology) was tested, as well as its internal CRC check mechanism for configuration bits, provided by the vendor. The HPTDC, already exposed at Louvain CRC on a proton beam line by a CMS group, was additionally tested at SIRAD facility at INFN Legnaro laboratories with heavy ions to fully characterise the SEU sensitivity as a function of the LET.

The combination of all measurements allowed a full assessment of expected SEU error rates inside TRM, validating all proposed components, with the noticeable exception of the Altera FPGA. A Flash based FPGA from Actel is now our baseline option.

I. INTRODUCTION

The Time-Of-Flight (TOF) detector of the ALICE experiment [1,2] has to provide particle identification information in the momentum range between 0.5 GeV/c and 2.5 GeV/c in the central region ($|\eta| \leq 1$) through precise time measurements of pulses induced by particles crossing the MRPCs. Time digitisation will be carried out by the HPTDC chip [3]. Over 20,000 HPTDC chips will be installed in the detector. Each Tdc Readout Module (TRM) card will house 30 chips. The conceptual design of TRM, board prototypes results and time resolution performances achieved have been presented elsewhere [4]. Preparing for final engineering and production, due in 2005/6, we conducted during 2004 devoted irradiation campaigns to validate all the components.

A. The TDC Readout Module

A logic block scheme of the TRM is shown in Fig. 1. The card, a VME slave card, will host 30 HPTDC, organised in two separate 32-bit parallel readout chains. A central FPGA will act as readout controller, event manager and implement also the VME interface (these three functions are separately shown in Fig. 1). To make easier maintenance and to match the Front End granularity, the HPTDCs will be mounted in 10 piggy-back cards, connected to both sides of a central motherboard. A central aluminium bar will guarantee the needed cooling of HPTDC.
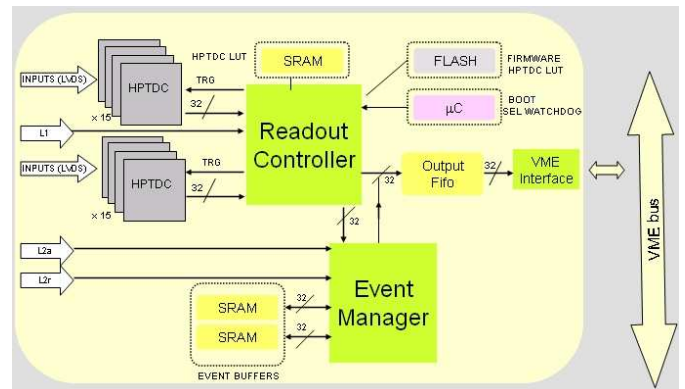

Figure 1: TRM logic blocks

After hit matching on L1 arrival, the FPGA will move matched hits from HPTDC readout FIFO to two coupled SRAM, that will mimic a dual port RAM. Finally an L2a signal will make available the requested event to the output FIFO.

Between L1 and L2, the FPGA will provide data packing and online data compensation for Integral Non Linearity (INL) of the HPTDC [3], accessing a LUT in SRAM. Flash memory will host a non-volatile copy of HPTDC LUT, as well as two copies of FPGA firmware, to allow FPGA remote programming. The microcontroller will act mainly as a latchup and SEU watchdog. It will additionally trace error conditions signalled by the HPTDCs (notably SEU auto-detections inside configuration bits) and to proper react through the JTAG interface of the chips.

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A DSP option, originally foreseen for data processing between L1 and L2, was dropped, fully exploiting FPGA capabilities. Key criteria selecting components to implement the discussed scheme are the possibility to remote upgrade the firmware and to be fault-tolerant and "SEU-aware" with respect to SEE radiation induced.

The TOF system will provide readout for 684 TRM cards, housed in 72 custom 12 slots VME crates.

B. The HPTDC

The TRM is based on a High Performance TDC (HPTDC) ASIC [3], developed by CERN/EP Microelectronic group for LHC applications, with multi-hit and multi-event capabilities. The ASIC provides relative time measurement of each hit at external trigger arrival. The time digitization is based on a clock synchronous counter and a DLL interpolator. The external 40 MHz clock is internally multiplied by a PLL to feed properly the DLL to reach the required resolution. The HPTDC has a 647 configuration bits register, plus a 40 control bits register, accessible through its JTAG interface. Digitised hits are stored in four L1 buffers, 256 hits deep and shared by 2 channels each. Matched hits with the external trigger are moved to a readout FIFO, 256 hits deep. The total amount of internal memories is 5.1 kB.

C. The ALICE/TOF radiation environment

The TRM will operate in a moderate hostile environment for what concerns total levels of radiation. A total dose of 1.2 Gy is actually expected in 10 years, with a total charged hadrons and neutron fluence of $2.1 \cdot 10^9$ cm^{-2} with energy above 20 MeV [4]. If damages for total integrated dose are likely to be negligible, protections for latchups are needed, as well as an adequate prediction of SEU error rates. The maximum flux of charged hadrons and neutrons above 20 MeV will occur in ALICE/TOF during Pb-Pb collisions and it was estimated to be 89 Hz/cm^2[5].

We planned an irradiation campaign using proton beams to test the components, excluding the HPTDC, used in the TRM, even if irradiation data for some of these devices are already available. Obviously among RAM and Flash memories and few other components like voltage regulators and limited current p-switch, we focused this test on the candidate FPGA, an Altera Stratix. Realized in 0.13 CMOS technology, this device provides built-in mechanism to check upsets in its configuration bits. At the same time, even if already qualified for space applications, the microcontroller chosen (an Atmel ATMEGA16) to act a latchup watchdog and boot controller needed to be tested carefully. This test is described in section II of this paper.

The HPTDC was not implemented in a technology guaranteed to be radiation hard and SEU insensitive, nevertheless it has self-checking built-in mechanisms enabling it to auto-detect SEU occurrences. The CMS group, which is using the HPTDC for readout of muon barrel drift chambers, tested at Louvain CRC facility the HPTDC for SEU, irradiating 8 HPTDC with 60 MeV protons for a total fluence of $5 \cdot 10^{10}$ cm^2. They registered just one SEU. Extrapolating their measurement [7], taking into account the different radiation levels and the number of HPTDC used, we expect a total rate of 2.4 SEU per day in the whole detector. Due to the large amount of HPTDC used we wanted to precisely characterize the SEU threshold of the device. We therefore additionally planned an irradiation campaign with heavy ions at SIRAD facility [8] at INFN Legnaro Laboratories, complementing the existing measurement. This test is described in section III of this paper.

II. RADIATION TESTS AT PSI

The test board used for this test (shown in Fig. 2 as block diagram and during the irradiation in Fig. 3) was designed to contain all the components to be housed in the central main board of the TRM. A complete list of the tested components is given in Table 1.

Table 1: Components irradiated at PSI

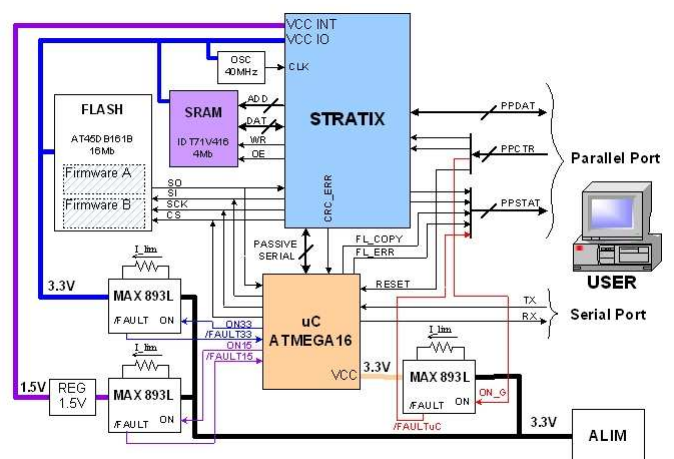| Component	Functionality
EP1S20F780	FPGA
IDT71V416S	RAM
ATMEGA16	Microcontroller
AT45DB161B	Flash memory
MAX893L	Current limited p-switch
ADP3339AKC-1.5/2.5	Low drop voltage regulator
Statek CXO3M	Clock

Figure 2: Block diagram of test board used at PSI

We connected the FAULT and ON signals of the MAX893L to the microcontroller, which was therefore responsible to handle any latch-up. Additionally a latchup protection was inserted to protect the microcontroller itself. The Altera Stratix CRC_ERROR pin was finally connected again to microprocessor. When the FPGA asserted that pin, the micro provided to reboot the FPGA: any error condition catch by the micro was reported through an RS232 interface. When a fault condition is asserted by the p-switch, the

microcontroller provides to switch off and then on the relevant component, checking the fault is cancelled. Moreover, through a parallel port interface, we monitored the internal status, as well as RAM, Flash and internal memories of the FPGA. We used 62% of internal memory resources of the FPGA (1 Mbit of RAM). The design implemented in the FPGA, besides the needed I/O interface, included a large shift register (4 kbit deep), monitored for internal logic error.
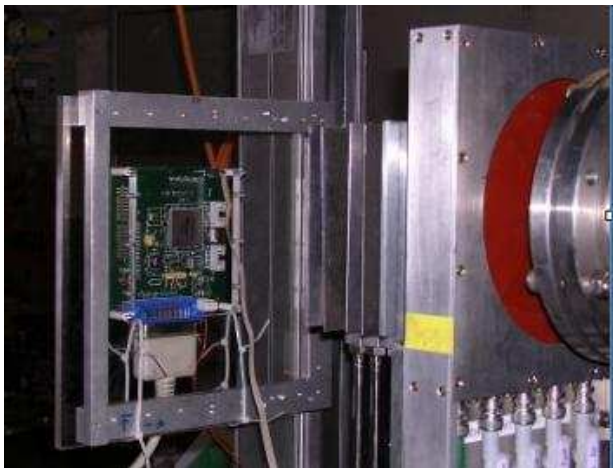

Figure 3: The test board at PSI

Two copies of the FPGA firmware were written into Flash memory and constantly monitored for upset (through a CRC check) by the microcontroller. Altogether the test board implemented all the fault tolerant mechanism and recovery strategies we planned to deploy on the TRM.

The irradiation was primarily done using 60 MeV protons. A check of the cross section behaviour at lower energies was however carried out, even if the lower energy point (no SEU observed at 10 MeV) is likely to be dominated by the metallic package shielding and by the Coulombian barrier screening. The main result for the configuration bits of the FPGA is shown in Fig. 4.
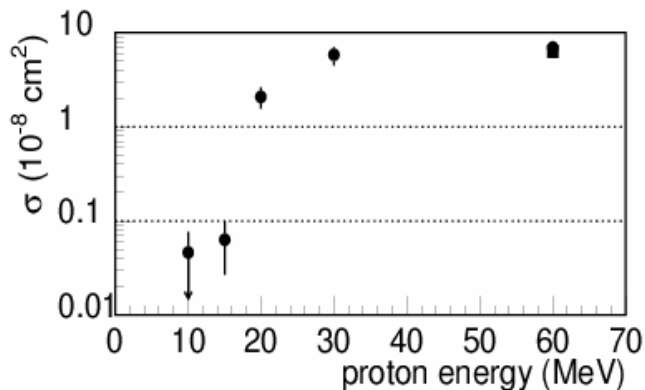

Figure 4: Device cross section for the Altera Stratix (see text for explanation of the square point at 60 MeV)

A global cross section for the device of $6.5 \ 10^{-8} \ cm^2$ has been obtained using two independent methods. In one case we stopped the irradiation immediately after the CRC_ERROR was asserted (square point in Fig. 4). Reducing enough the beam intensity ($\approx 5 \cdot 10^5$ Hz/cm^2), we then run continuously the device (that is we did the reboot under irradiation but with a very low probability to observe a SEU during boot). This method is reported with full circles in Fig. 4. As can be seen, we found the two methods gave very similar result, once taken into account the dead time during the boot phase. The cross sections expressed in cm^2/bit for the memories tested are shown in table 2. It is worthwhile to note the cross section measured for the Stratix is reasonably consistent with results obtained for SRAM circuits realized with commercial 0.13 CMOS technology [9]. Moreover, exploiting the configuration check provided by the vendor of the device, the measurement corresponds to an effective and complete monitor of all the configuration bits.

Table 2: SEU cross sections for tested devices

Component	σ (cm^2/bit)
EP1S20F780 (conf.)	$1.1 \ 10^{-14}$
EP1S20F780 (mem.)	$3.4 \ 10^{-14}$
IDT71V416	$8.5 \ 10^{-15}$
AT45DB161B	$<10^{-19}$

No latchups have been observed in any of the devices under test. We didn't observe also any SEE in Flash memories and in the ATMEGA16. All the devices were irradiated up to a total dose of 14 krad. Being the microcontroller the main controller of the card, it was additionally irradiated up to 20 krad, without recording any error condition.

III.   HEAVY IONS IRRADIATION OF THE HPTDC

The SIRAD facility provides ion species with kinetic energies ranging from 30 MeV (H) to 334 MeV (Au). The corresponding surface LET spans from 0.015 MeV cm^2/mg to 80 MeV cm^2/mg. On the basis of previous irradiation data of memories in 0.25 CMOS technology, we selected LET values from 3.9 to 41.7 MeV cm^2/mg. Due to the ion energies available at SIRAD, the HPTDC was decapsulated and mounted in a test socket, as shown in Fig. 5.
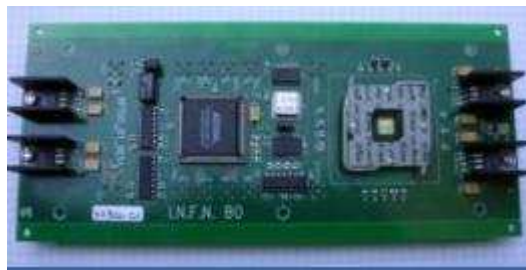

Figure 5: Test card used at SIRAD. The decapsulated HPTDC is visible on the right.

The test card provided access to the HPTDC through its JTAG interface using an Altera MAX CPLD. We handled the I/O through 10 LEMO connectors mounted into the back side of the card. Even in this case a MAX893L protected the irradiated HPTDC, being the FAULT and ON signals managed through the CPLD.

We irradiated the chip for each LET in three different setups: (a) no hit stored in internal buffers; (b) half readout FIFO filled (128 hit stored); (c) all L1 buffers and readout FIFO full (1280 hits stored), varying the beam intensity in such a way to have a SEU occurrence in a time interval much larger than our periodic check of the configuration (every 100 ms). Readout FIFO and L1 buffers parity error can be detected only when reading back data: data were read back every 10 seconds. No latchups have been detected. The total integrated dose by the device was 4.1 krad.

The global cross section measured for a configuration upset of the HPTDC is shown in Fig. 6. This curve includes also errors detected in state machine logic, not only in configuration bits, and this contribution is shown with the lower points.
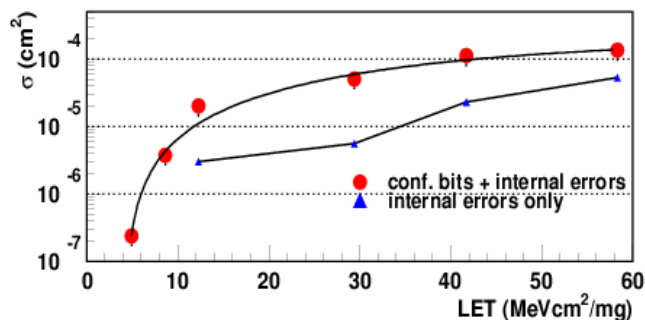

Figure 6: Global configuration upset cross section for the HPTDC. The contribution from internal logic error is also shown.

A Weibull fit using the usual formula

$$\sigma = \sigma_{sat}\left\{1 - \exp\left[-\left(\frac{LET - LET_{th}}{W}\right)^S\right]\right\}$$

is also shown. The fit for the configuration bits only gave $\sigma_{sat}=1.3 \cdot 10^{-7}$ cm^2/bit, LET_{th}= 4.1 MeVcm^2/mg, W=27 MeVcm^2/mg, S=1.7. These values are in good agreement with values measured for 0.25 CMOS memories and shift registers as in [10].
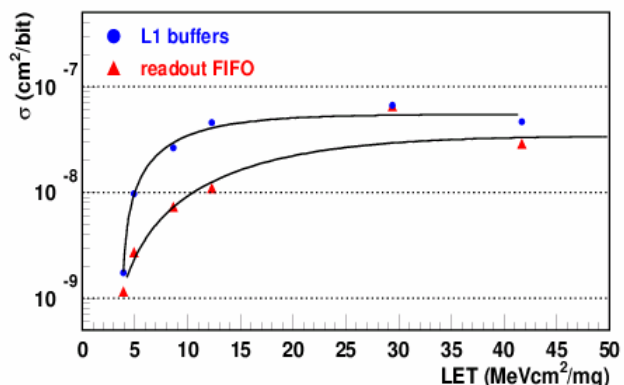

Figure 7: SEU Cross sections for HPTDC internal memories.

Fig. 7 shows the result for the L1 buffers and for the readout FIFO separately. Using the procedure described in [11] and the Weibull fit values, we estimated a cross-section for protons at 60 MeV. The result for the four discussed components of the HPTDC is given in Table 3.

Table 3: SEU cross sections (estimated for proton at 60 MeV) for each HPTDC component

Component	σ (cm^2/bit)
Configuration/control bits	$3.8 \ 10^{-15}$
Readout FIFO	$6.7 \ 10^{-15}$
L1 buffers	$2.4 \ 10^{-14}$
Global	$3.0 \ 10^{-12}$ (cm^2)

IV. ERROR RATE ESTIMATIONS

From the obtained cross sections, it is straightforward to obtain error rate estimations for the different components inside TRM, multiplying them for the abovementioned maximum foreseen rate of neutrons and charged hadrons above 20 MeV (100 Hz/cm^2 including some safety factors). However it should be noted that for some memories (as the HPTDC L1 buffers and readout FIFOs as well as the TRM internal event buffers) they are dependent also from L1/L2 latencies, L1 rate, readout time and occupancy inside in the detectors. We computed these error rates under conservative assumptions (L1 = 1 KHz, TOF occupancy at 30%). They are presented in Table 3, for one card and within the whole system in term of minimum time between failures (MTBF).

Table 4: MTBF for different TRM components

Component	MTBF/TRM	MTBF/TOF
Stratix (conf)	43 hours	3.8 min
INL LUT	6.8 days	14.3 min
Event buffer	2.9 years	2300 min
HPTDC (conf)	3.4 years	1.8 days
L1 buffers	>400 years	260 days
Readout FIFO	>1600 years	800 days

Three main results are achieved:

1) The error rate in the whole system for the Altera Stratix is clearly unacceptable;

2) Despite the large number of chips deployed, the error rate inside HPTDC is well under control. During ALICE life, some board will never experiment SEU inside HPDTC internal memories;

3) Excluding the FPGA, the more frequent upset source will come from the INL LUT for the HPTDC.

V. CONCLUSIONS AND OUTLOOK

During the 2004 irradiation campaign, we successfully validated almost all the proposed components for the ALICE TOF Tdc Readout Module, including memories (RAM and Flash), micro controller, clock, voltage regulator and limited current p-switch. A detailed analysis showed that most frequent upset will occur in HPTDC look-up tables. Adequate firmware is under development to trace the upset and force a reload of the LUT from the Flash memory.

The cross-section measured for the tested FPGA is, as far as we know, one of the few existing for Altera 0.13 devices. The CRC control mechanism in Altera Stratix worked very well. Depending on system dimension, radiation level and application, the use of this device, coupled with a SEU quasi-immune device for boot and monitor, as our micro or a CPLD, it is a suitable scheme for LHC applications.

Unfortunately as the numbers discussed in section IV showed, this is not the case for the ALICE/TOF. Error rate is clearly too high and we are currently moving our design to an Actel ProAsic Plus, which are substantially immune to SEU [12]. Even if such a solution slightly complicates the design to handle the remote programming of the card (and also additional power supply has to be provided), we will certainly gain a greater robustness of the system with respect to SEU.

The irradiation with heavy ions of HPTDC gave results in nice agreement with existing data (irradiation with protons), allowing also a test of internal memory buffers. This error rate in the whole system is well under control and, as expected, the upset in configuration bits is the dominating error source.

A global estimation of TRM SEU rate in all its components has been obtained.

VI. REFERENCES

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