Radiation tolerance tests for key components of the ALICE TOF Tdc readout module

1. The TDC module of ALICE/TOF
2. Irradiation at PSI of Tdc Readout Module component candidates (including an Altera Stratix FPGA)
3. Irradiation with heavy ions at Legnaro of HPTDC
4. Error rates
5. Outlook

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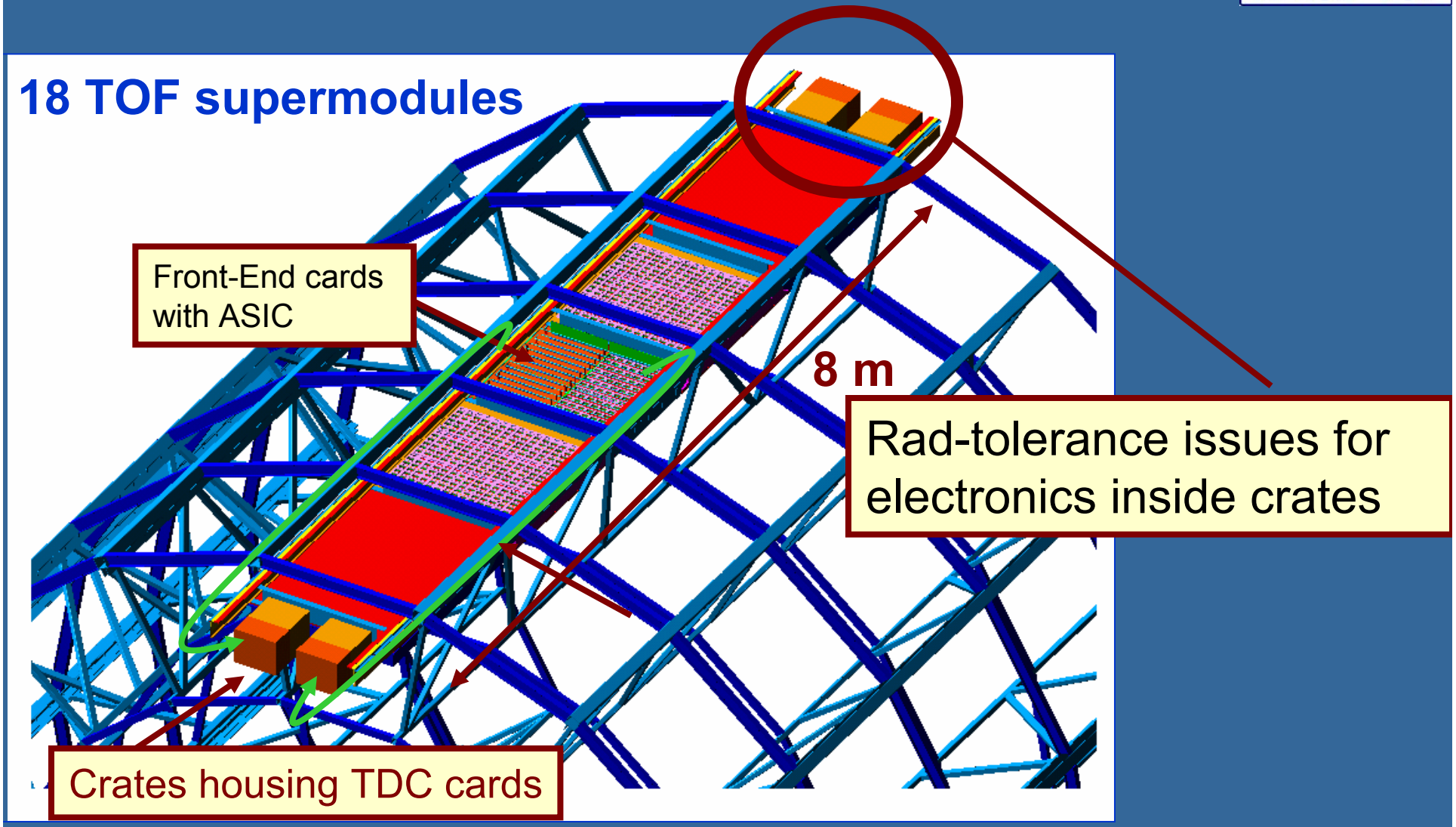
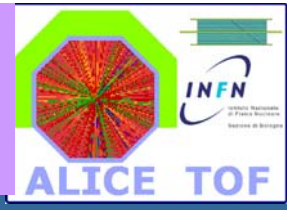
INFN/Bologna and CAEN

TOF overview



Radiation levels



Radiation levels expected at ALICE/TOF:

1.2 Gy/10 years (TID)

Total neutron fluence (>20 MeV): 1.6 10^9 /cm^2/10 years.

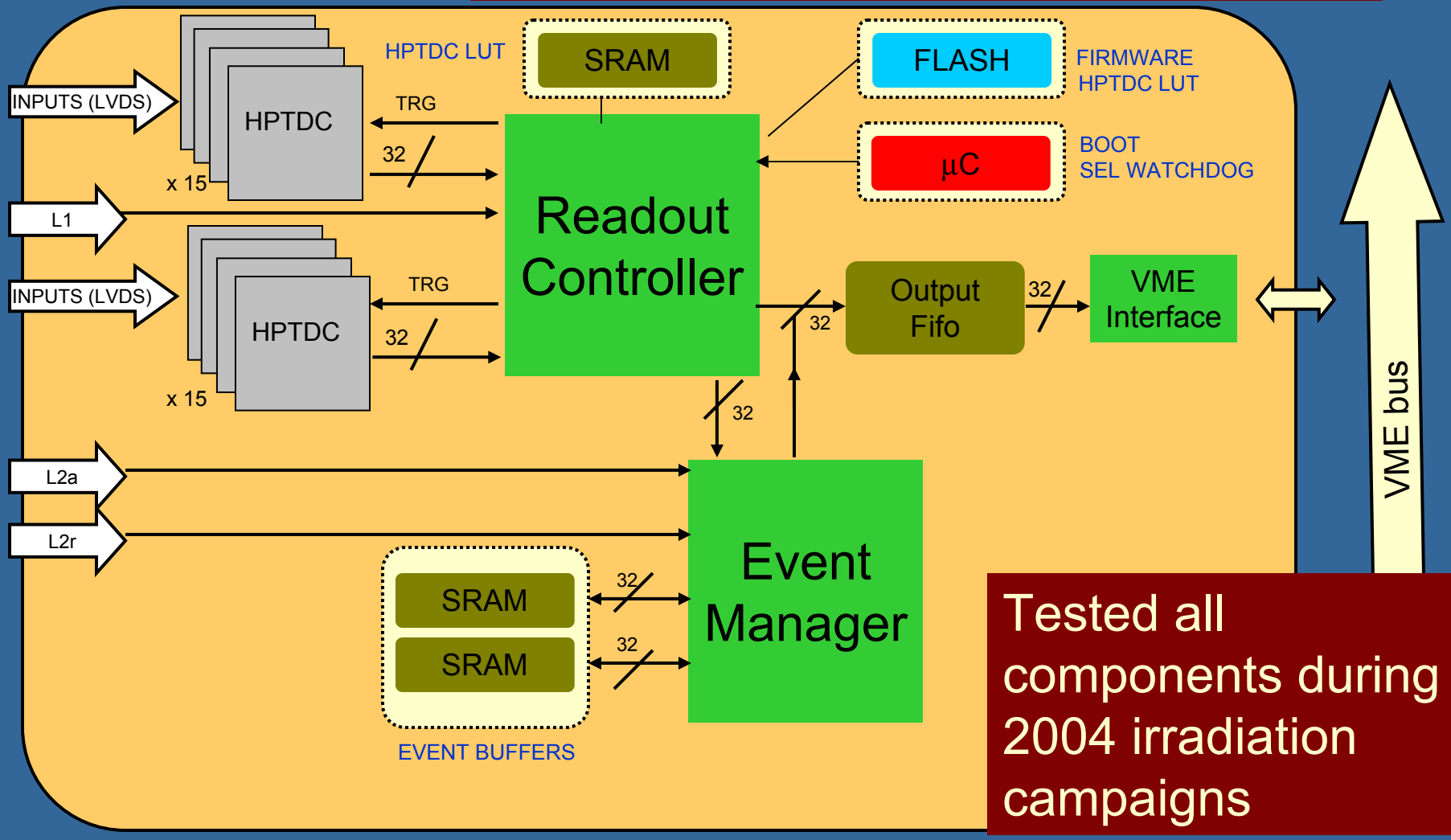
Total charged hadrons (>20 MeV): 5.3 10^8 /cm^2/10 years.

89 Hz/cm^2 expected in PbPb MB events (charged hadrons+neutrons > 20 MeV).

For ALICE/TOF careful design needed to handle SEU,
Degradation for TID effects neglectable.
Latchup protections needed.

TRM conceptual design

684 Tdc Readout Module inside crates



Tested all components during 2004 irradiation campaigns

Functionalities implemented by an FPGA

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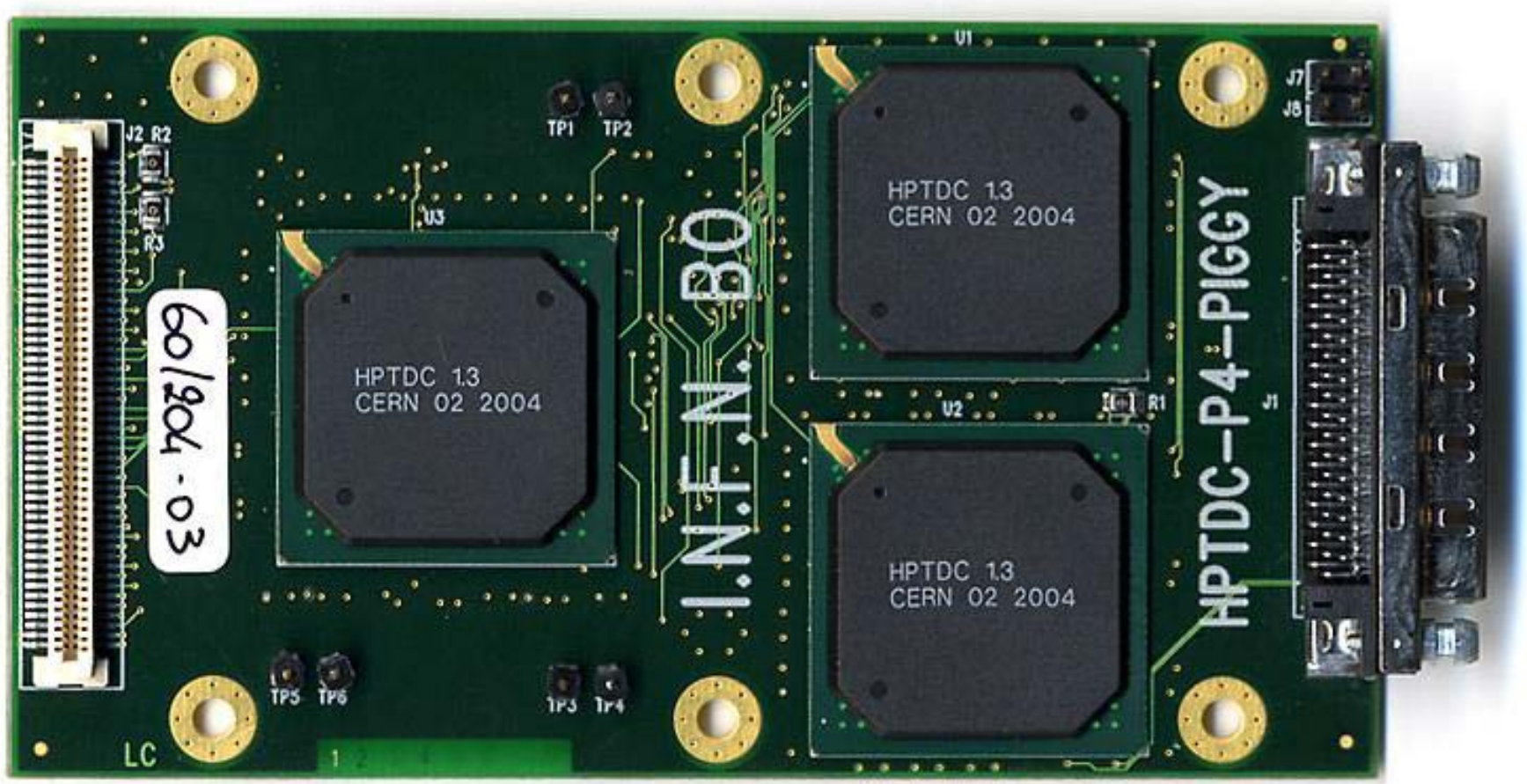
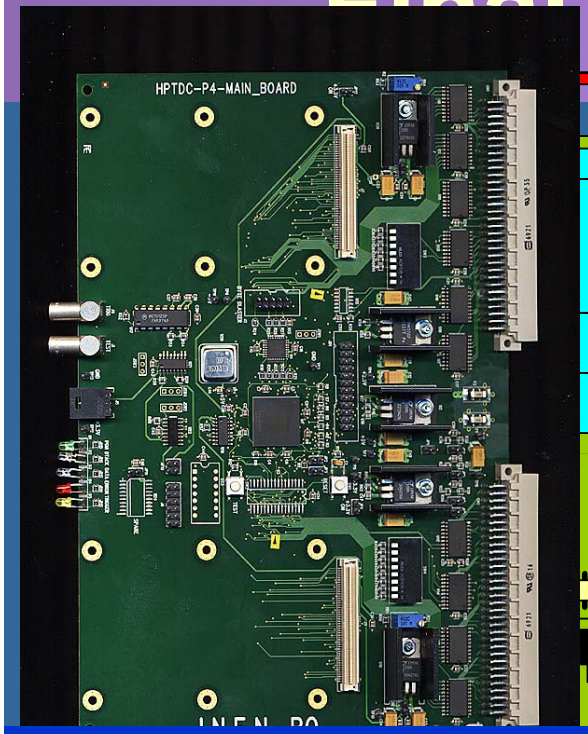
Final TRM layout

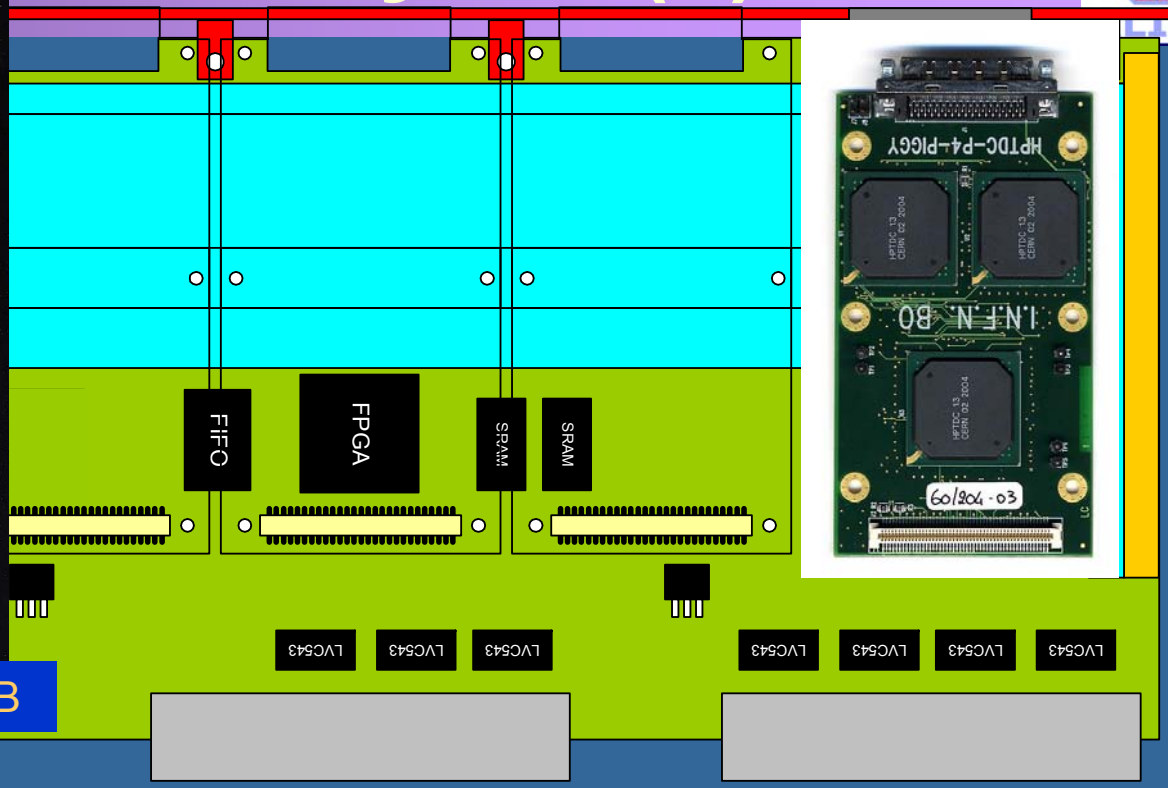


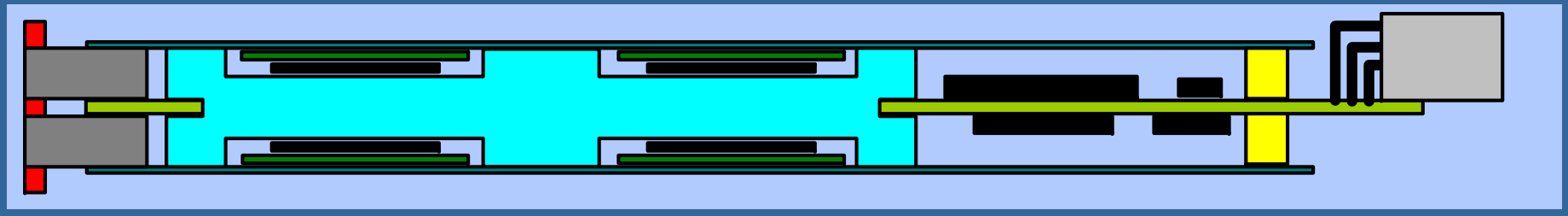
HPTDC mounted on 24 ch piggy back

Final TRM layout (2)



6U MB prototype housing 2 PB





5 piggyback cards per side, 1 central PCB for FPGAs and memories, central aluminium bar for heat dissipation

Radiation tolerance test

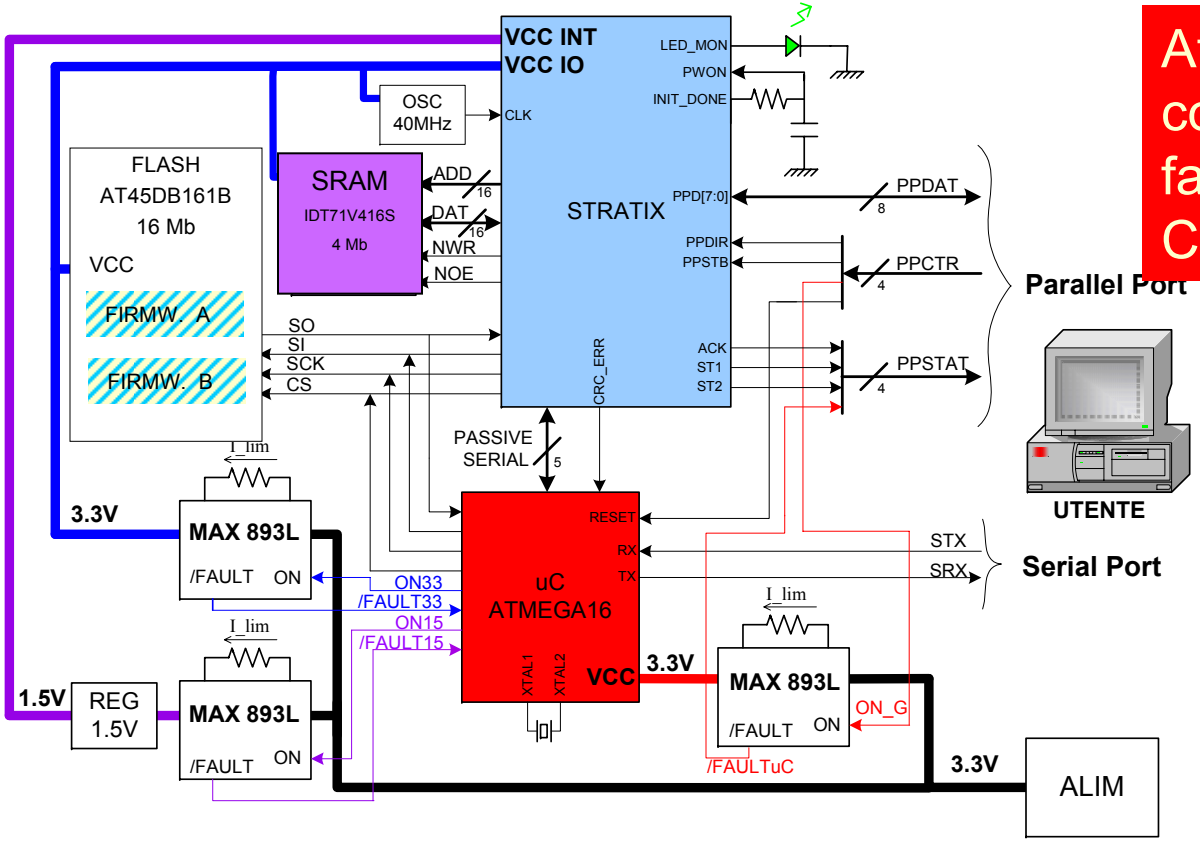
Tested components
- Altera Stratix EP1S20F780
- IDT RAM IDT71V416
- Atmel μC ATMEGA16
- Atmel Flash AT45DB161B
- MAX893L
- ADP3339AKC-1.5/2.5
- Clock Statek CXO3M

Test at PSI (Zurich)
June 2004

Test card for all (except HPTDC) components foreseen for TRM.
Validation test of latchup/SEU error recovery strategy
Beam: protons @ 60 MeV

Radiation tolerance board

Altera Stratix (and Cyclone) feature: real-time monitoring of configuration bits: a clear procedure to establish configuration changed (effective SEFI monitor)

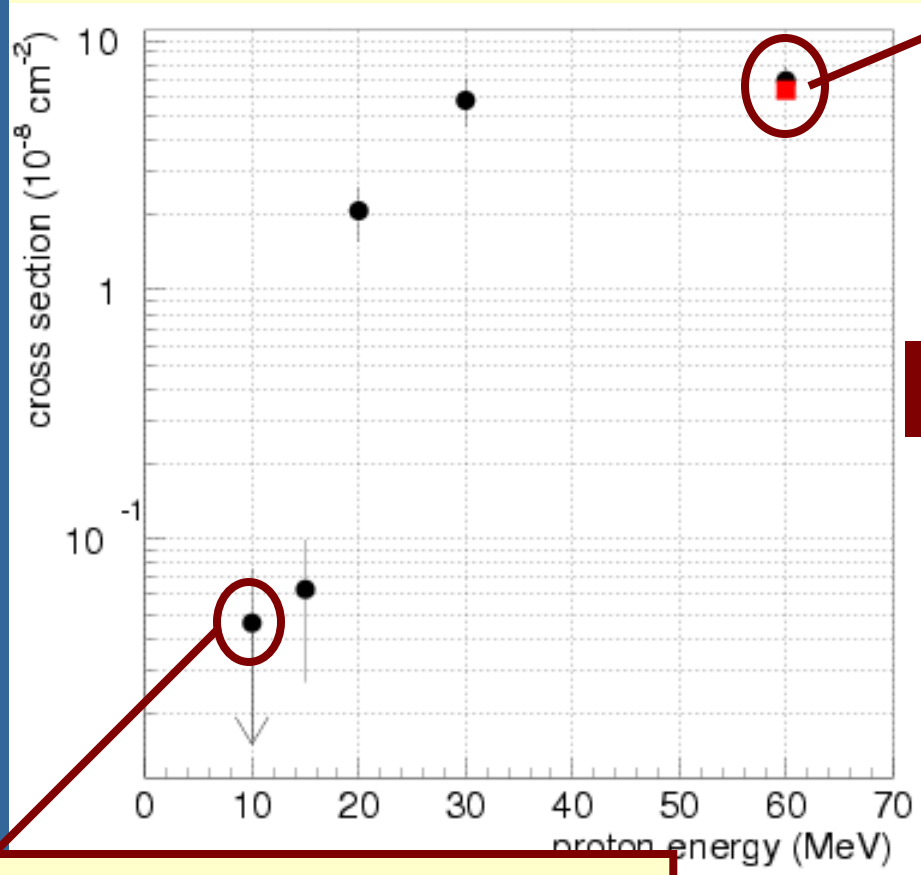


Atmel µC acts as controller of power fault (latchups) + CRC_ERROR pin

Monitor of errors in SRAM, FPGA internal memory + shift register logic check

Stratix results

ALTERA STRATIX EP1S20 (configuration upset)



Used two indipendent methods to estimate cross sections

$\sigma = (6.5 \pm 0.2\ (stat))\ 10^{-8}\ cm^2$

metallic package + Coulombian barrier

Reasonably consistent with existing results for 0.13 CMOS SRAM (Anelli et al. @RADECS 2003)
$O(\sigma) \approx 10^{-14}\ cm^2/bit$

SRAM and other...

Device	DCS (cm^2)	DCS/bit (cm^2/bit)
STRATIX (EP1S20)	$6.5\ 10^{-8}$	$1.1\ 10^{-14}$
STRATIX (INTMEM)	$1.8\ 10^{-8}$	$3.4\ 10^{-14}$
FLASH (AT45DB161B)	$< 0.9\ 10^{-12}$	$< 10^{-19}$
ATMEL µC (ATMEGA 16)	$< 0.9\ 10^{-12}$	
SRAM (IDT71V416S)	$3.6\ 10^{-8}$	$8.5\ 10^{-15}$
Other (clock, voltage regulators,..)	No damage up to 14 krad	

No latchup observed. TID = 14 krad.

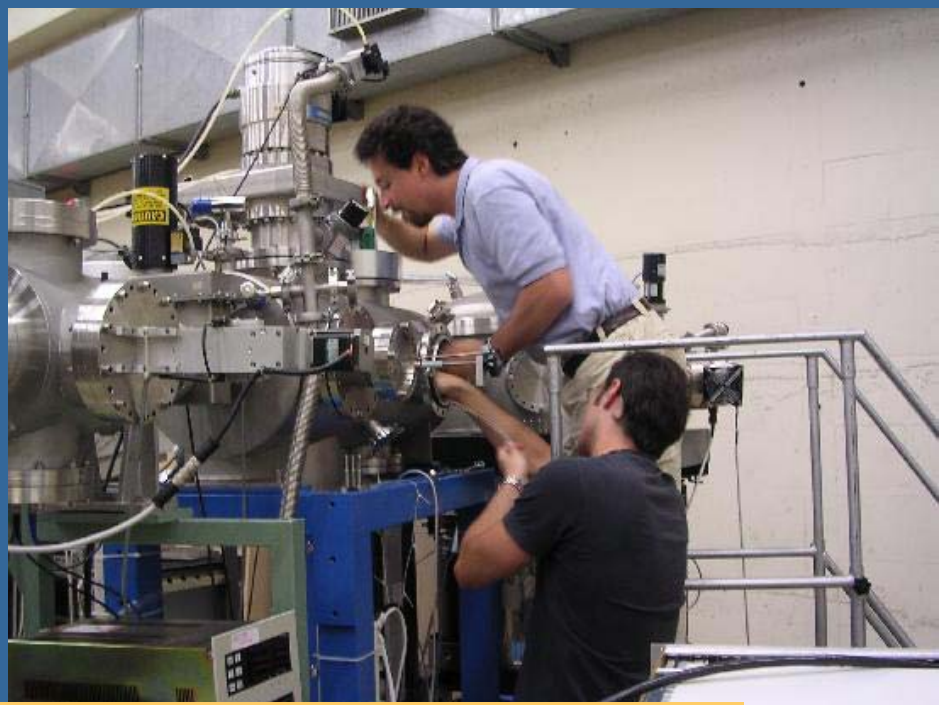
HPTDC irradiation at Legnaro

SIRAD facility devoted to irradiation with heavy ions (ions available for 1 MeVcm^2/mg<LET < 80 MeVcm^2/mg) at INFN Legnaro Labs.

20520 HPTDCs to be deployed on ALICE/TOF.

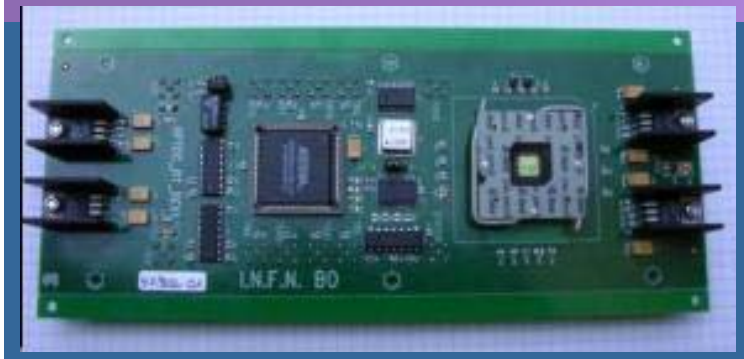
CMS measurement on HPTDC:(8 HPTDC irradiated with 5 10^{10} protons/cm^2 @ 60 MeV, no SEL detected, just 1 SEU):

Extrapolation to TOF: MTBF 2.4 days in the whole detector

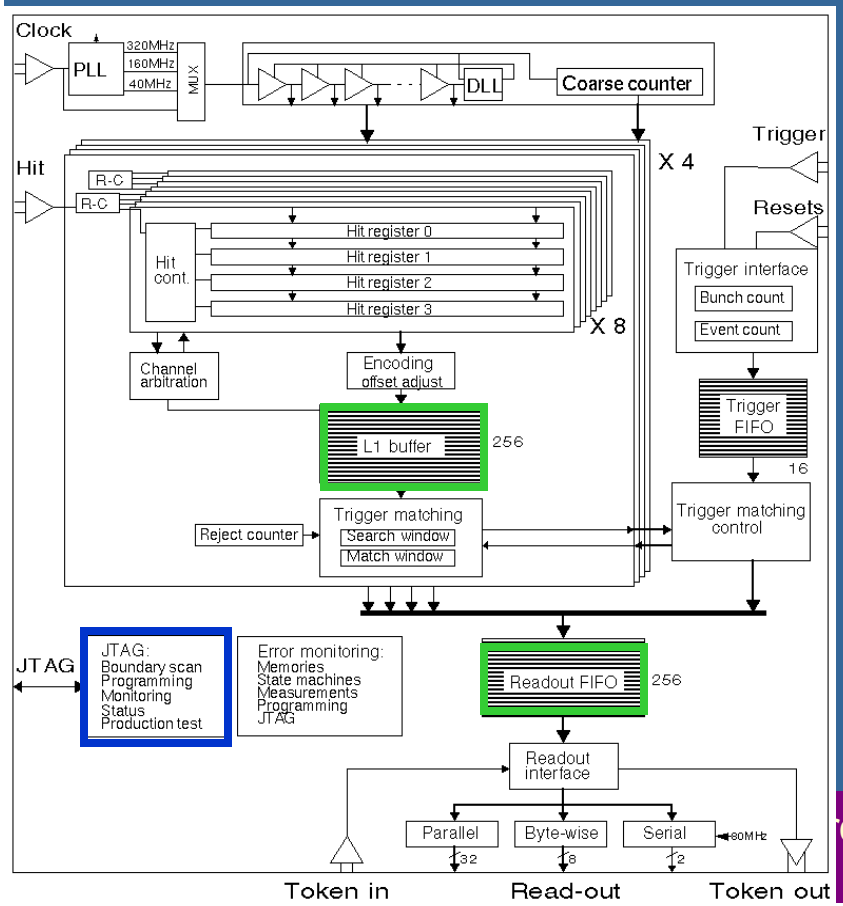


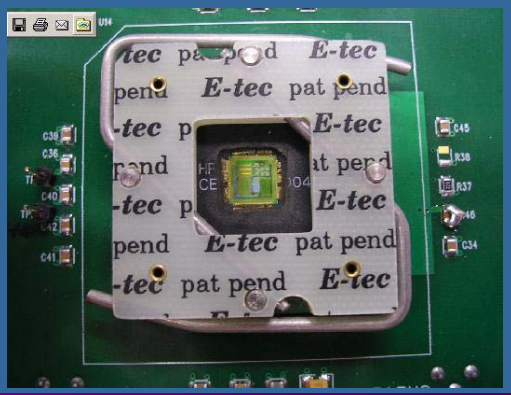
Measurement with heavy ions to check previous measurement and characterize SEU cross sections of internal registers and memories as a function of LET

HPTDC test board



Read-out via JTAG interface
Upset monitoring via JTAG (built-in feature of HPTDC)
687 bits of configuration
40 Kb of internal memory
Latchup monitor
Decapsulation needed





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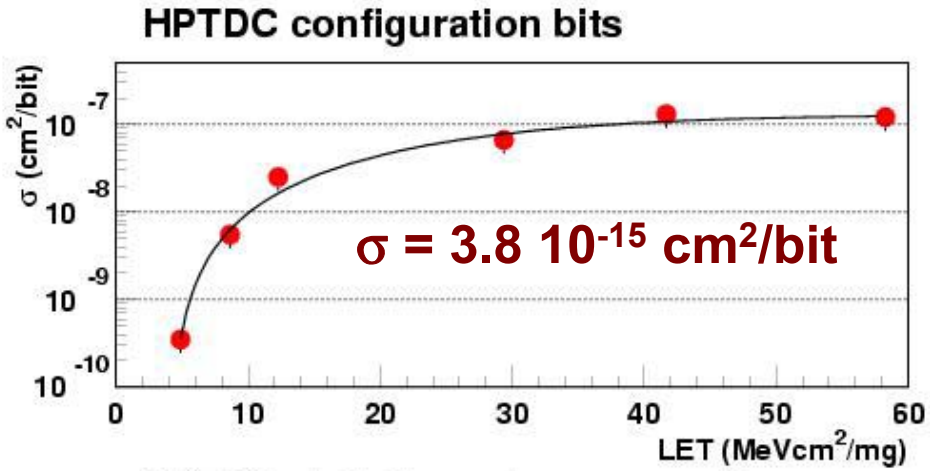
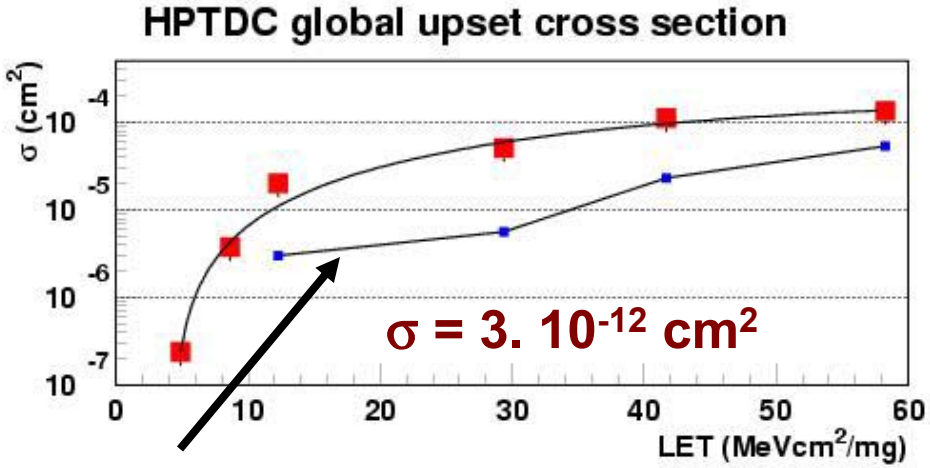
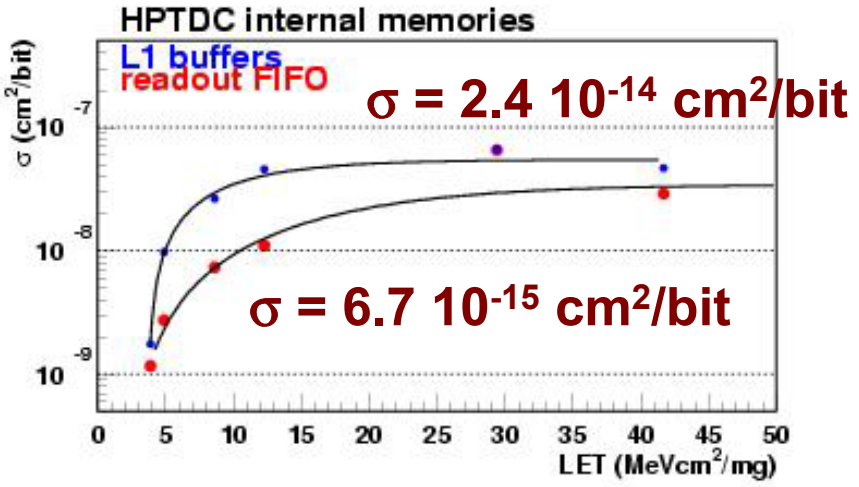
HPTDC irradiation results



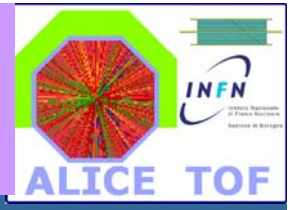


Contribution from state machine errors



Weibull fits + conversion to a cross-section for 60 MeV proton irradiation (M. Huthinen and F. Faccio, NIMA450, 155(2000))

Error rates at ALICE/TOF



$$E_r\,(h^{-1}) = \phi\,(part/cm^2/s)\; s\,(cm^2)\; 3600\,(s/h)\; n_d$$

100 Hz
Current simulation: 89 Hz
(possible geometrical overestimation 30%)

board (n_d= 1),
crate (n_d= 10)
TOF (n_d=684)

MTBF: Minimum Time Between Failure = 1 / E_r

SEU Error rates for TRM (1)

Device	σ (cm^2)	TRM(h^{-1})	CRATE (h^{-1})	TOF (h^{-1})	MTBF (min)
STRATIX CONF	$6.5\ 10^{-8}$	0.023	0.23	15.7	3.8
SRAM (HPTDC LUT 1.97 Mbit)	$1.7\ 10^{-8}$	0.006	0.06	4.2	14.3
SRAM (event buffers 4.0 Mbit)	$3.6\ 10^{-8}$	6.3E-7	6.3E-6	4.3E-4	2300

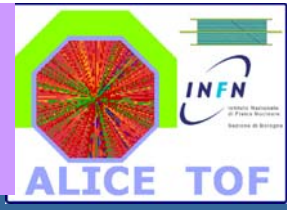
- ✓ MTBF for Stratix too small, moving to Actel
- ✓ HPTDC LUT: parity check implemented with correction + ask reload from Flash
- ✓ Error rates in event buffers depends on L1 rate, L2 latency + TOF occupancy. Error rates here are for L1=1 KHz , 30% TOF occupancy (exp. 15%)). CRC check will be implemented.

SEU error rate for TRM (2)

HPTDC Components	σ (cm^2)	TRM(h^{-1})	CRATE (h^{-1})	TOF (h^{-1})	MTBF (day)
CONF	$3\ 10^{-12}$	$3.2\ 10^{-5}$	$3.2\ 10^{-5}$	$2.3\ 10^{-2}$	1.8
READOUT FIFO (8Kb)	$5.4\ 10^{-11}$	$7.2\ 10^{-8}$	$7.2\ 10^{-7}$	$5.2\ 10^{-5}$	800
L1 BUFFER (8Kbx4)	$7.9\ 10^{-10}$	$2.2\ 10^{-7}$	$2.2\ 10^{-6}$	$1.6\ 10^{-4}$	260

- As expected error rate for configuration dominant
- Nice agreement with CMS previous measurement
- Error rates for readout fifo and L1 buffers are dependent also on L1 latency, read-out time, TOF occupancy and L1 rate (here assumed 30% occ. + 1KHz for L1)

Conclusions and outlook



•SRAM, μC, clock, voltage regulator, Flash and HPTDC: OK
Firmware to check SEU for Flash, SRAM (LUT for HPTDC and event buffers) under development.

•Irradiations with heavy ions of HPTDC gave results in nice agreement with existing data (irradiation with protons), internal memory tested. HPTDC error rate ok.

•A global estimation of TRM SEU upset rate (and in all its components has been obtained.

The CRC control mechanism in Altera Stratix works very well. Depending on system dimension, radiation level and application, it is a suitable option for LHC applications.

Unfortunately this is not the case for ALICE/TOF. Error rate is too high (at least for TRM and DRM). **New choice: Actel ProAsic Plus APA600**.

Conclusions and outlook (2)

We will provide V_{pp} = 16.2 V and V_{pn}=-13.5 V in crate backplane (use ± 12V VME lines) to allow remote programming. Porting to Actel under way.

For other VME modules (DRM: data readout; LTM trigger) similar design and choice of components (SRAM, FLASH, μC, choice of FPGA, ...).

Many thanks for their help and support to A. Candelori (SIRAD), H. Wojtek (PSI) and F. Faccio (CERN)