Analog Design in ULSI CMOS Processes

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Outline

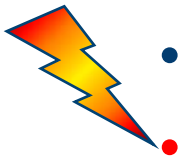
- Motivation
- How scaling works for devices and interconnections
- Scaling impact on the transistor performance
- Scaling impact on analog circuits performance
- Noise in mixed-mode integrated circuits
- ULSI processes: which options for analog?
- Conclusions

Motivation

- The microelectronics industry is moving to ULSI CMOS processes, and we have interest to follow the trend because of:
  - Technology availability issues
  - Clear advantages for digital designs
  - Improved radiation tolerance
- The performance of detector electronics for future High Energy Physics experiments will still be strictly related to the analog front-end

What are the advantages and disadvantages of using a process in the 180 – 100 nm range for analog design? What do we gain? And what do we loose? And are there new problems and phenomena which have to be considered?

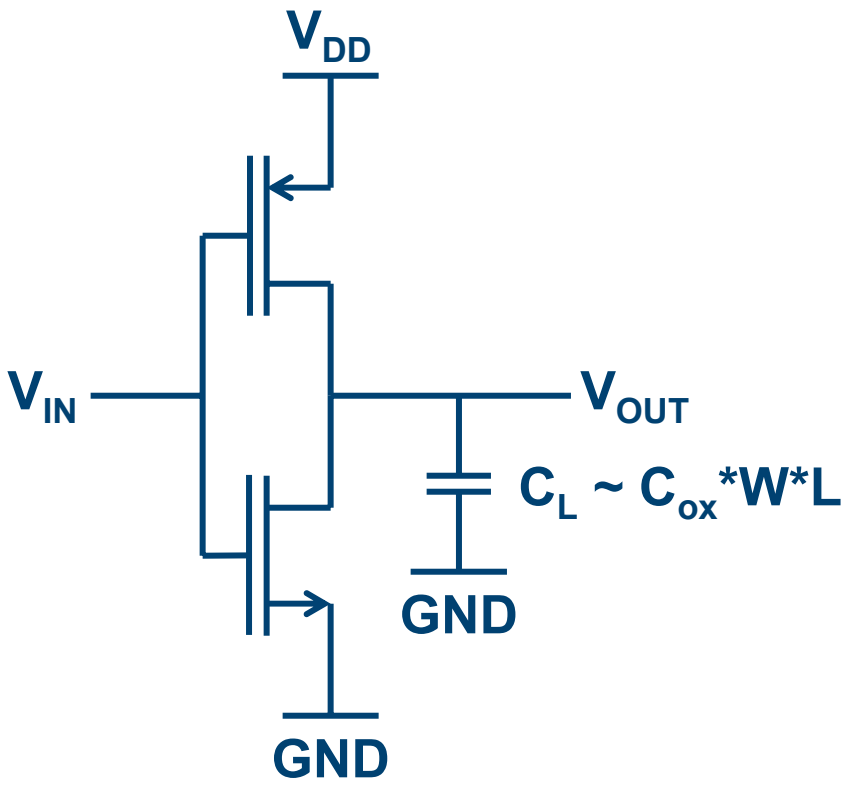
Outline



- Motivation
- How scaling works for devices and interconnections
  - Why scaling ?
  - Transistor scaling
  - Interconnection scaling
- Scaling impact on the transistor performance
- Scaling impact on analog circuits performance
- Noise in mixed-mode integrated circuits
- ULSI processes: which options for analog?
- Conclusions

Why scaling ?

Example: CMOS inverter



$$P_{static} = I_{leakage} \cdot V_{DD}$$

$$P_{dynamic} = C_L \cdot V_{DD}^2 \cdot f$$

$$PDP = C_L \cdot V_{DD}^2$$

Power-delay product

t_{ox} ↓ V_{DD} ↓ C_L ↓

Scaling improves density, speed and power consumption of digital circuits

Offer for digital in a 130 nm node

- **more than 200.000 gates per mm^2**
- **speed > 1 GHz**
- **power gate dissipation < 4 nW / MHz @ 1.2 V**
- **8 metal levels, all copper, low K (FSG or BlackDiamond™)**
- **pitches: M1 0.34 μm, M2 to M7 0.41 μm, M8 0.9 μm**
- **embedded memory (single transistor, SRAM, Non-volatile)**

VERY GOOD FOR System-on-Chip

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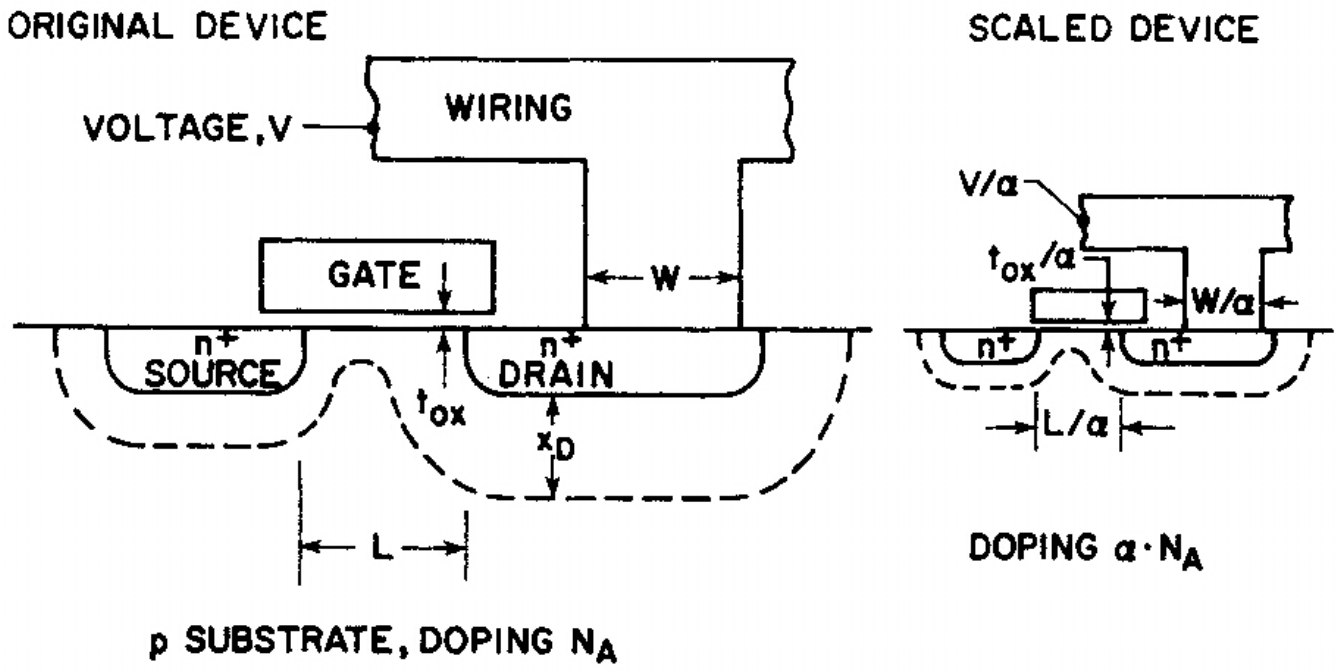
Constant field scaling

The aim of constant field scaling is to reduce the device dimensions (to improve the circuit performance) without introducing effects which could disturb the good operation of the device.



$\alpha > 1$

B. Davari et al., "CMOS Scaling for High Performance and Low Power - The Next Ten Years", *Proc. of the IEEE*, vol. 87, no. 4, Apr. 1999, pp. 659-667.

Constant field scaling (2)

Summary of the scaling factors for several quantities

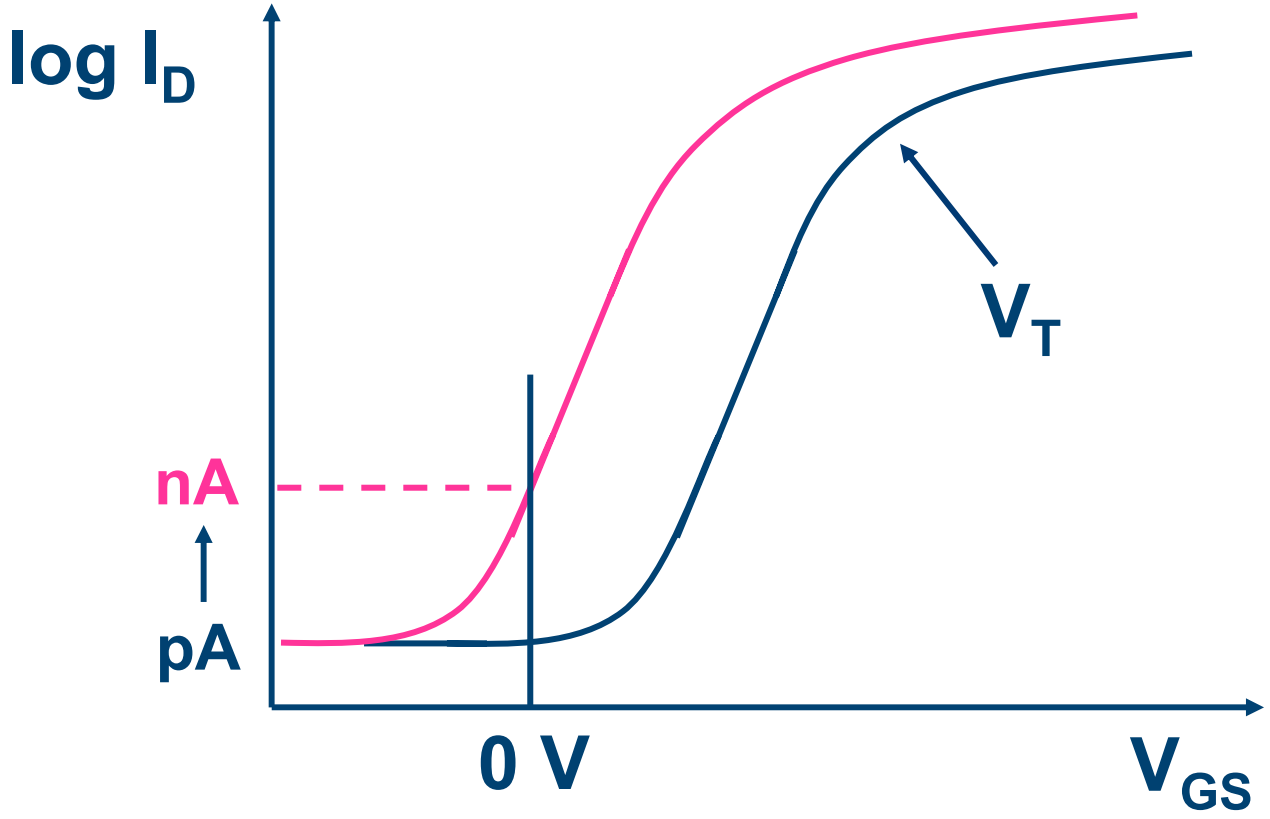
Quantity	Scaling Factor	Quantity	Scaling factor
Device dimensions (L, W, t_{ox}, x_D)	$1/\alpha$	Capacitances	$1/\alpha$
Area	$1/\alpha^2$	Capacitances per unit area	α
Devices per unit of chip area (density)	α^2	Charges	$1/\alpha^2$
Doping concentration (N_A)	α	Charges per unit area	1
Bias voltages and V_T	$1/\alpha$	Electric field intensity	1
Bias currents	$1/\alpha$	Body effect coefficient (γ)	$1/\sqrt{\alpha}$
Power dissipation for a given circuit	$1/\alpha^2$	Transistor transit time (τ)	$1/\alpha$
Power dissipation per unit of chip area	1	Transistor power-delay product	$1/\alpha^3$

$\alpha > 1$

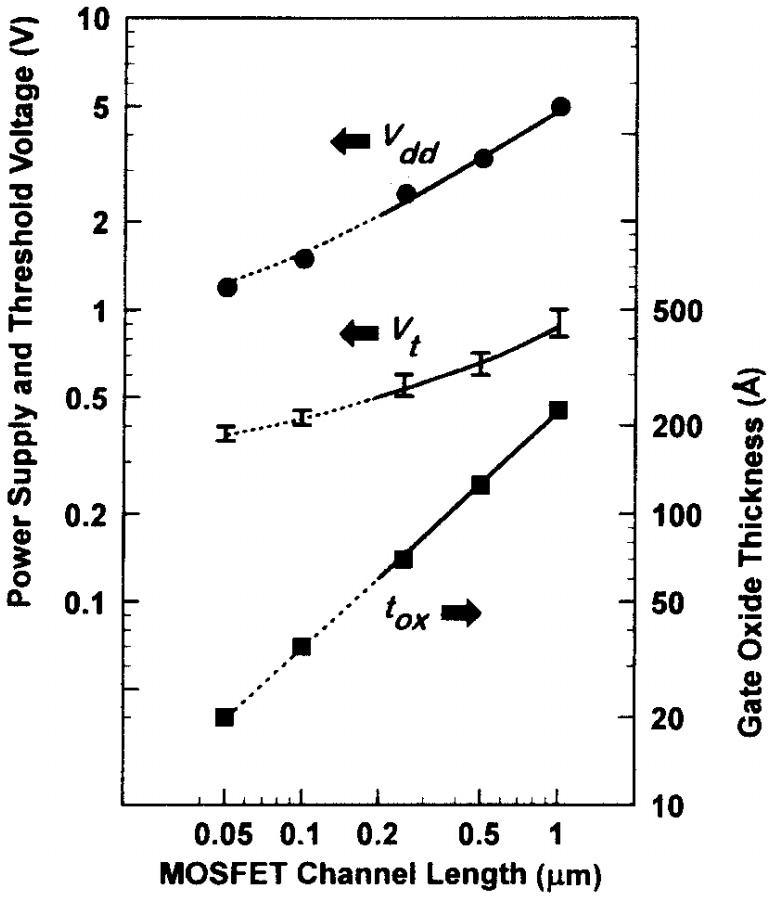
$$C_{ox} = \frac{\varepsilon_{SiO_2}}{t_{ox}}$$

Constant field scaling problem

Subthreshold slope and width of the moderate inversion region do not scale. This can have a devastating impact on the static power consumption of a digital circuit.



Generalized scaling

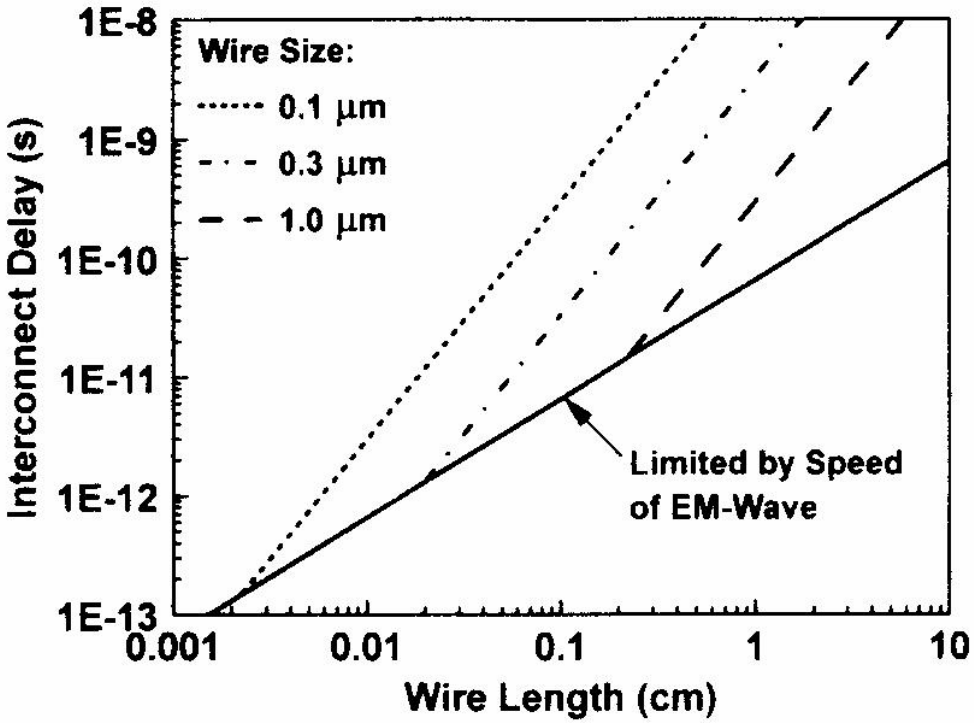


- The dimensions in the device scale as in the *constant field* scaling
- V_{dd} scales to have reasonable electric fields in the device, but slower than t_{ox}, to have an useful voltage swing for the signals
- The doping levels are adjusted to have the correct depletion region widths
- To limit the subthreshold currents, V_T scales more slowly than V_{dd}

Y. Taur et al., "CMOS Scaling into the Nanometer Regime", *Proc. of the IEEE*, vol. 85, no. 4, Apr. 1997, pp. 486-504.
Y. Taur and T. H. Ning, *Fundamentals of Modern VLSI Devices*, Cambridge University Press, 1998, p. 186.

Scaling of interconnections

An accurate scaling of the interconnections is needed as well, so that we can profit at the circuit level of the improvements made at the device level. Interconnections are becoming more and more important in modern technologies because the delay they introduce is becoming comparable with the switching time of the digital circuits.

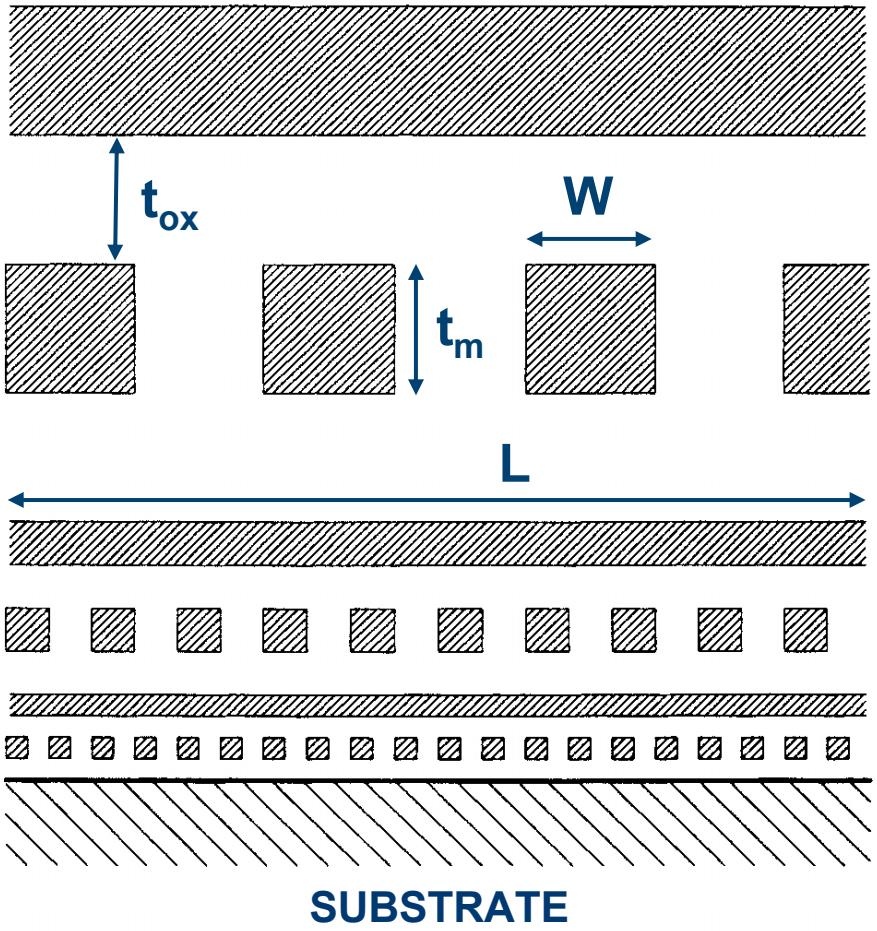


Wires with square section

Y. Taur et al., "CMOS Scaling into the Nanometer Regime", *Proceedings of the IEEE*, vol. 85, no. 4, Apr. 1997, pp. 486-504.
T. N. Theis, "The future of interconnection technology", *IBM Journal of Research and Development*, vol. 44, no. 3, May 2000, pp. 379-390.

“Reverse” scaling

The scaling method is different from the one applied to devices



If W, L, t_m and t_{ox} are decreased by α

- **Current density increases by α**
- **R increases by α, C decreases by α**
- **RC (delay) does not scale!!!**

In practice, wires dimensions are reduced only for local interconnections (but not t_m). At the chip scale, t_m and t_{ox} are increased (reverse scaling).

G. A. Sai-Halasz, "Performance trends in high-end processors", *Proceedings of the IEEE*, vol. 83, no. 1, January 1995, pp. 20-36.

Hierarchical scaling

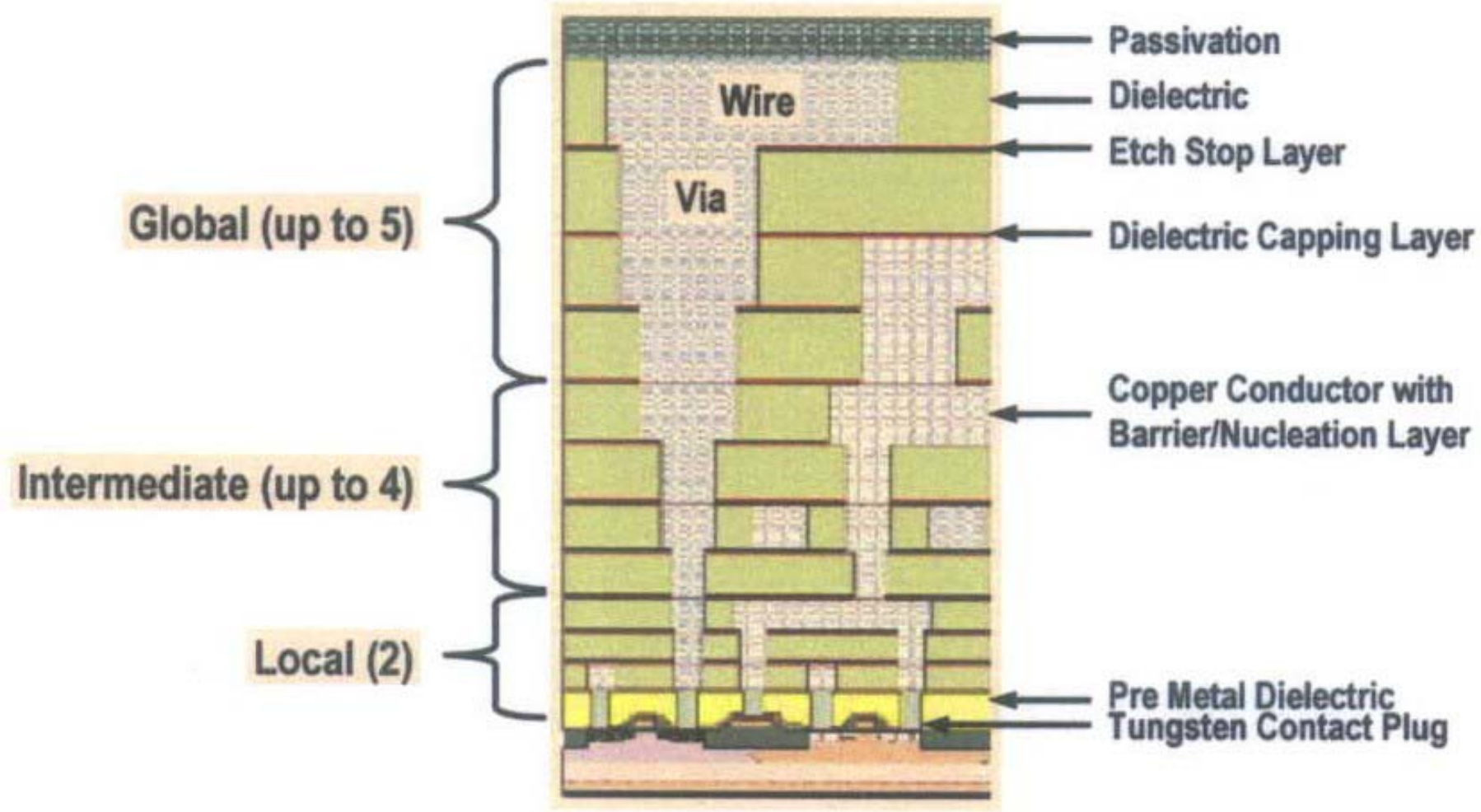
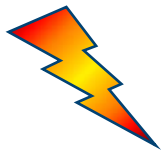


Figure 36 Cross-section of Hierarchical Scaling

The International Technology Roadmap for Semiconductors (2001 Edition)

Outline

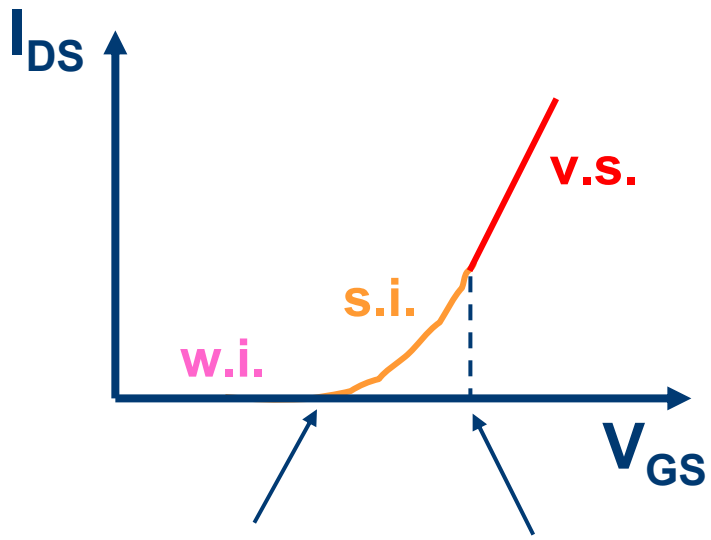


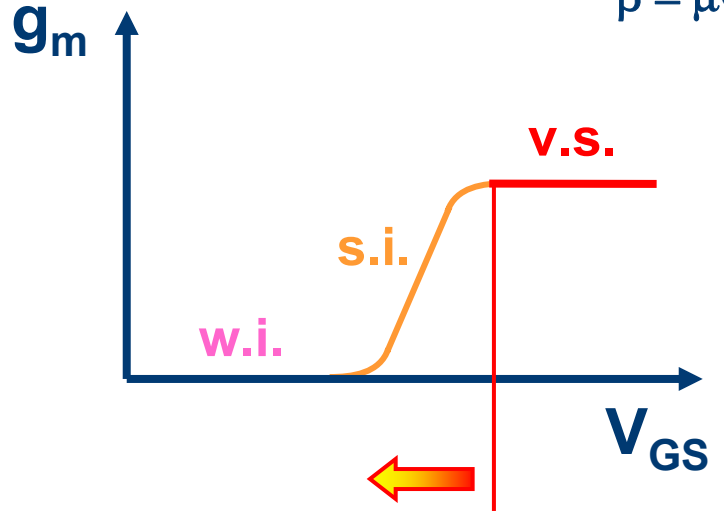
- Motivation
- How scaling works for devices and interconnections
- Scaling impact on the transistor performance
  - Weak inversion, strong inversion, velocity saturation
  - Transistor intrinsic gain
  - Gate leakage and noise
- Scaling impact on analog circuits performance
- Noise in mixed-mode integrated circuits
- ULSI processes: which options for analog?
- Conclusions

From weak inversion to velocity saturation

Weak inversion (w.i.)	$I_{DS\_w.i.} = I_{D0}\frac{W}{L}e^{\frac{V_{GS}}{n\phi_t}}$	$g_{m\_w.i.} = \frac{I_{DS}}{n\phi_t}$
Strong inversion (s.i.)	$I_{DS\_s.i.} = \frac{\beta}{2n}(V_{GS} - V_T)^2$	$g_{m\_s.i.} = \sqrt{2\frac{\beta}{n}I_{DS}}$
Velocity saturation (v.s.)	$I_{DS\_v.s.} = WC_{ox}v_{sat}(V_{GS} - V_T)$	$g_{m\_v.s.} = WC_{ox}v_{sat}$

$$\beta = \mu C_{ox}\frac{W}{L}$$



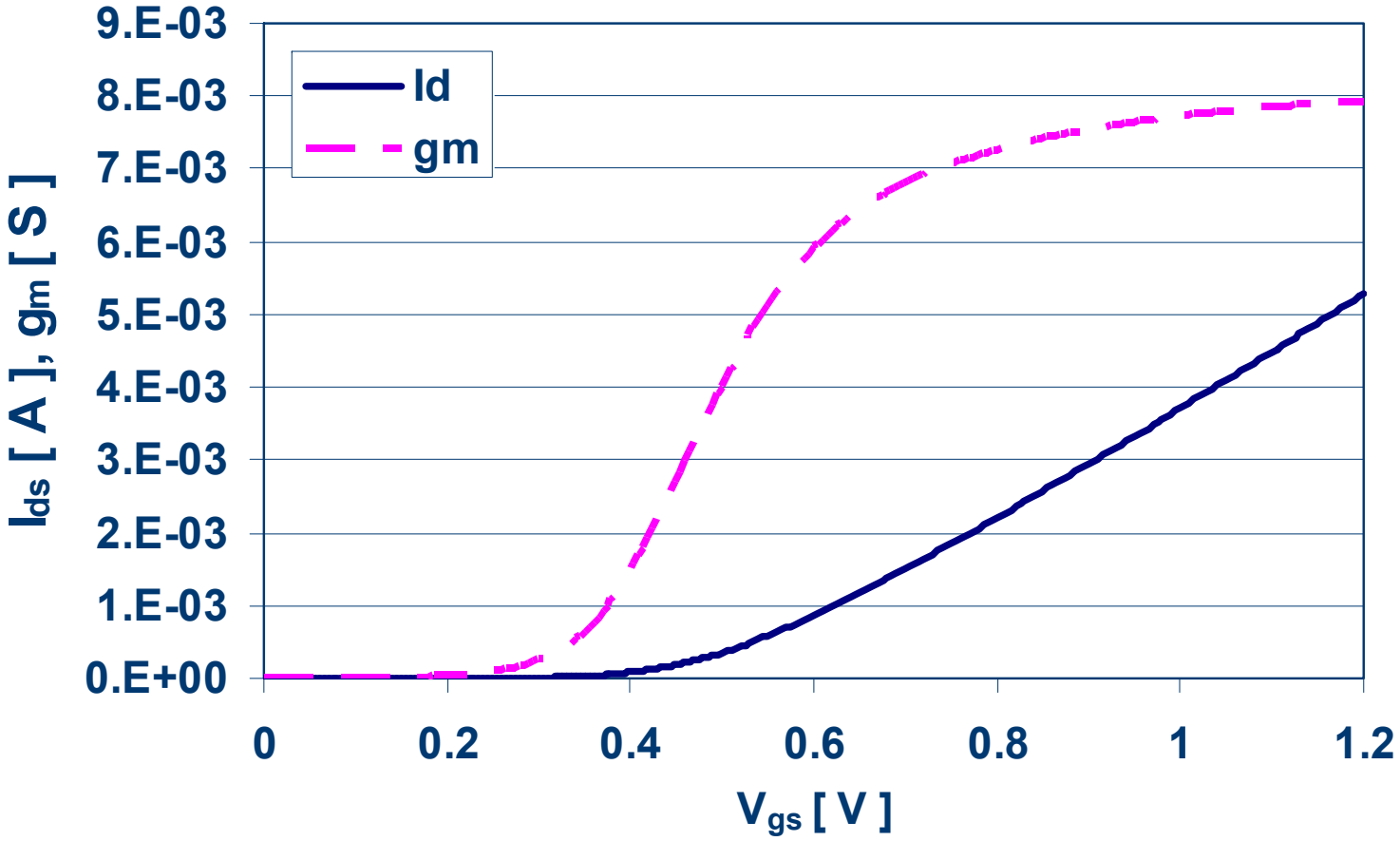


$V_{w.i.\_to\_s.i.} = 2n\phi_t$ $\quad V_{s.i.\_to\_v.s.} = 2nL\frac{v_{sat}}{\mu}$

$V_{s.i.\_to\_v.s.}$ decreases with scaling!!!

Measurement example

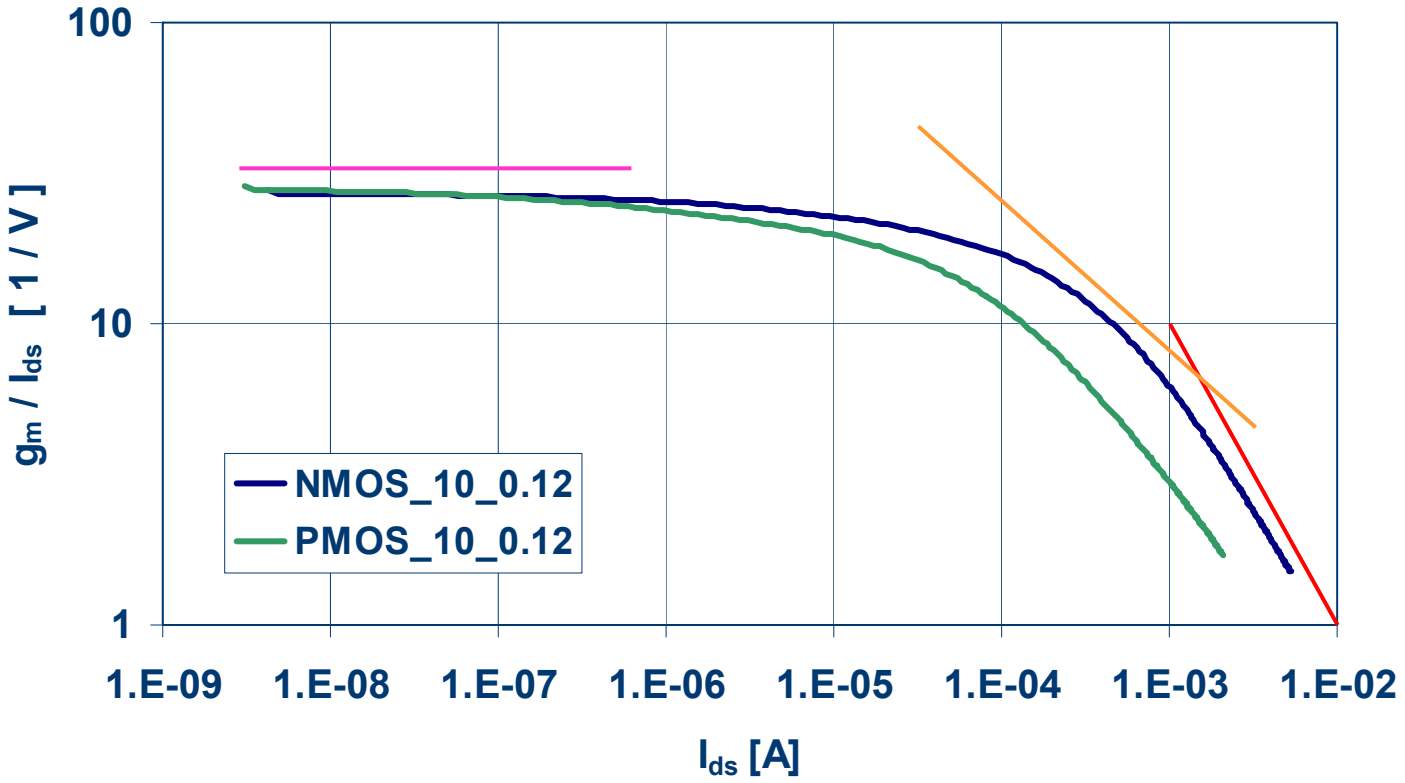
NMOS, W = 10 μm, L = 0.12 μm



V_{DS} = 1.2 V, V_{GS} swept from 0 V to 1.2 V

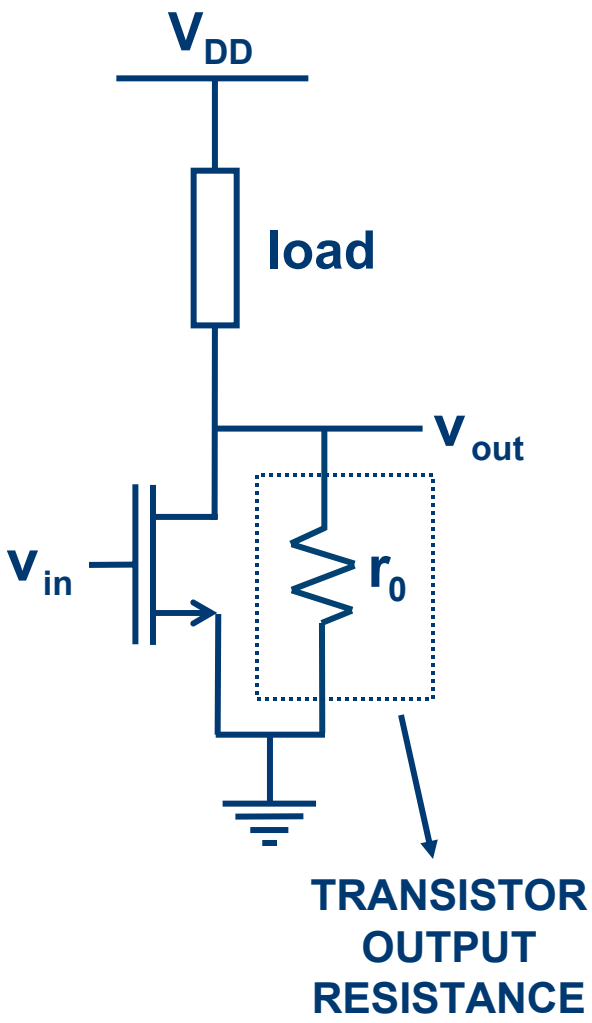
Measurement example (2)

$$\left(\frac{g_m}{I_{DS}}\right)_{w.i.} = \frac{1}{n\phi_t} \qquad \left(\frac{g_m}{I_{DS}}\right)_{s.i.} = \sqrt{2\frac{\beta}{n}\frac{1}{I_{DS}}} \qquad \left(\frac{g_m}{I_{DS}}\right)_{v.s.} = \frac{WC_{ox}v_{sat}}{I_{DS}}$$



V_{DS} = 1.2 V, V_{GS} swept from 0 V to 1.2 V

Intrinsic gain $g_m * r_0$



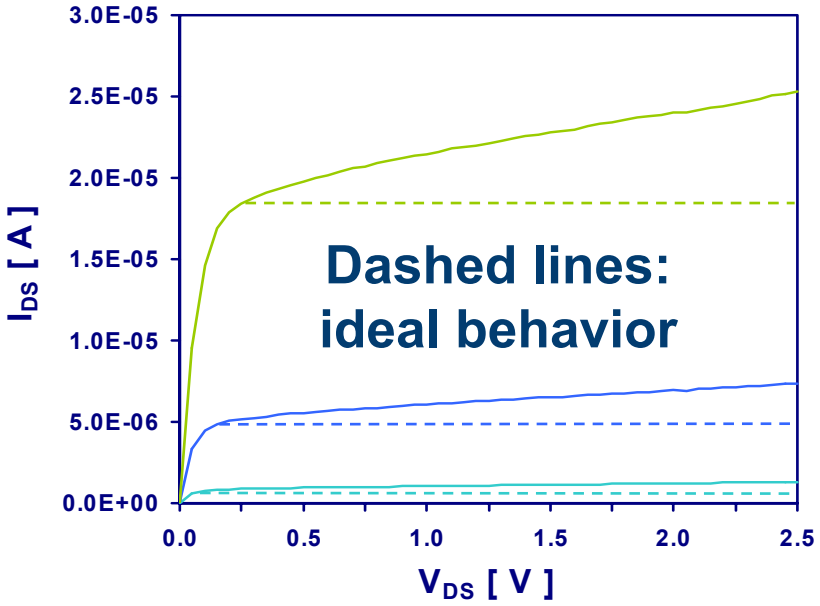
$$v_{out} = v_{in} \cdot g_m \cdot \frac{r_0 r_{load}}{r_0 + r_{load}}$$

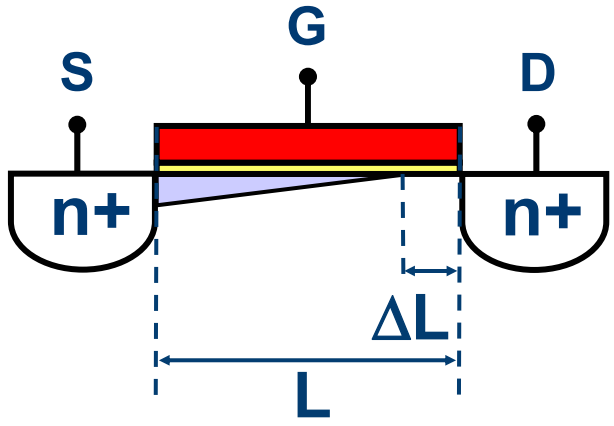
$$\text{Gain} = \frac{v_{out}}{v_{in}} = g_m \cdot \frac{r_0 r_{load}}{r_0 + r_{load}}$$

Gain → $g_m r_0$ when $r_{load} \rightarrow \infty$

The quantity $g_m r_0$ is called intrinsic gain of the transistor. It represents the maximum gain obtainable from a single transistor, and it is a very useful figure of merit in analog design.

Output resistance





$$I_{DS} = \frac{\beta}{2n}(V_{GS} - V_T)^2(1 + \lambda V_{DS})$$

$$g_{out} = \frac{\partial I_{DS}}{\partial V_{DS}} = \lambda \cdot I_{DS\_SAT}$$

$$r_0 = \frac{1}{g_{out}} = \frac{1}{\lambda \cdot I_{DS\_SAT}} = \frac{V_E \cdot L}{I_{DS\_SAT}}$$

$$\lambda = \frac{1}{V_{DS} - V_{DS\_SAT}} \cdot \frac{\Delta L}{L - \Delta L} \approx \frac{1}{V_{DS} - V_{DS\_SAT}} \cdot \frac{\Delta L}{L}$$

Scaling impact on the intrinsic gain

$$\lambda \approx \frac{1}{V_{DS} - V_{DS\_SAT}} \cdot \frac{\Delta L}{L} \qquad \Delta L \approx \sqrt{\frac{2\varepsilon_{Si}}{qN_a}(V_{DS} - V_{DS\_SAT})}$$

$$g_{out} = \lambda \cdot I_{DS\_SAT} \qquad r_0 = \frac{1}{g_{out}} = \frac{1}{\lambda \cdot I_{DS\_SAT}} \qquad \text{Intrinsic Gain} = g_m \cdot r_0$$

Supposing to have constant field scaling for the technology, we obtain:

W	L	β	V_{GS}-V_T	g_m	V_{DS}	ΔL	λ	I_{DS_SAT}	g_{out}	r_o	$g_m r_0$
1/α	1/α	α	1/α	1	1/α	1/α	α	1/α	1	1	1
1	1/α	α^2	1/α	α	1/α	1/α	α	1	α	1/α	1
1/α	1	1	1/α	1/α	1/α	1/α	1	$1/\alpha^2$	α^2	α	α
1	1	α	1/α	1	1/α	1/α	1	1/α	1/α	α	α
α	1/α	α^3	1/α	α^2	1/α	1/α	α	α	α^2	$1/\alpha^2$	1

Scaling impact on the intrinsic gain (2)

The intrinsic gain is proportional to "α*L": if L is kept constant g_m*r_0 increases by the scaling factor, if L is decreased by α then g_m*r_0 stays constant.

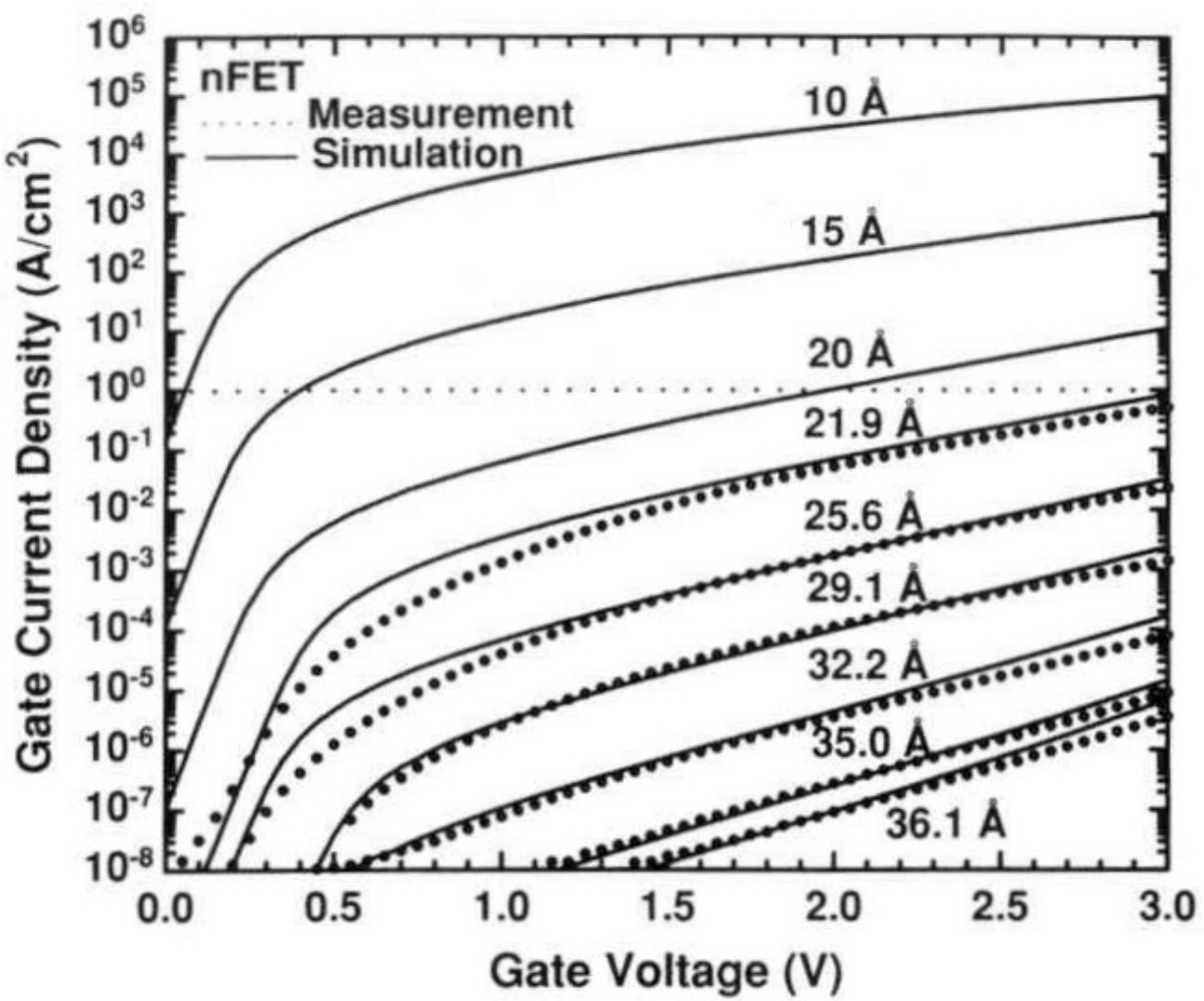
$$g_m * r_0 \propto \alpha * L$$

This result is based on the following assumptions:

1. **We consider Channel Length Modulation and not Drain Induced Barrier Lowering**
2. **The transistor is working in Strong Inversion**
3. **We applied the Constant Field Scaling rules**

It can be shown that the result obtained is true even dropping the assumptions above

Gate leakage current



Implications:

Static power consumption for digital circuits and shot noise for analog

D. J. Frank et al., "Device Scaling Limits of Si MOSFETs and Their Application Dependencies", *Proc. IEEE*, vol. 89, no. 3, March 2001, pp. 259-288.

Scaling impact on noise

$$\frac{\overline{v_{in}^2}}{\Delta f} = 4kTn\gamma\frac{1}{g_m} + \frac{K_a}{C_{ox}WL}\frac{1}{f^{\alpha}}$$

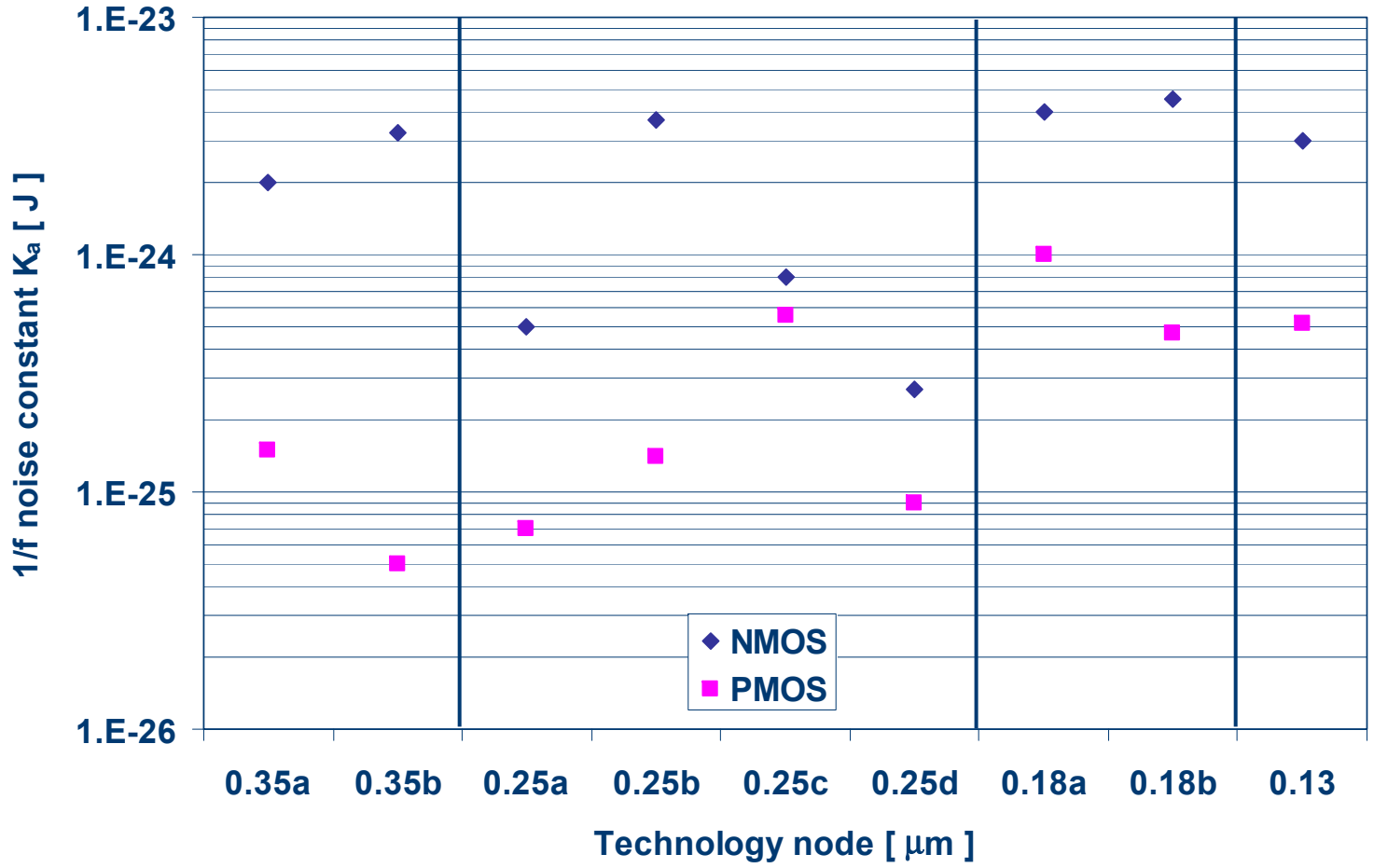
$$g_m = \sqrt{\frac{2}{n}\mu C_{ox}\frac{W}{L}I_{DS}} \qquad C_{ox} = \frac{\varepsilon_{SiO_2}}{t_{ox}}$$

$t_{ox} \downarrow \quad C_{ox} \uparrow \quad g_m \uparrow$

White noise: keeping the same W/L ratio and the same current, we have an improvement in the noise since C_{ox} (and therefore g_m) increases with scaling.

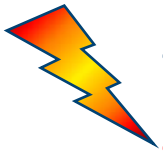
1/f noise: if we suppose that the constant K_a does not change with scaling, we have an improvement in the noise if we keep the same device area (WL). Data taken from the Roadmap foresee that K_a will remain more or less constant even for the most advanced CMOS processes. This must, of course, be verified…

1/f noise constant K_a



Data taken from the literature except from the 0.13 μm node and one of the 0.25 μm node points, which are our measurements

Outline



- Motivation
- How scaling works for devices and interconnections
- Scaling impact on the transistor performance
- Scaling impact on analog circuits performance
  - Signal to Noise Ratio (SNR)
  - Analog power consumption
  - Low voltage issues
- Noise in mixed-mode integrated circuits
- ULSI processes: which options for analog?
- Conclusions

Scaling impact on power, speed, SNR

$$PWR = I_{DS} \cdot V_{DD}$$

$$\overline{v_{n\_white}^2} = 4kTn\gamma\frac{1}{g_m}$$

$$SNR_w = \frac{V_{DD}}{\sqrt{v_{n\_white}^2}}$$

Assuming constant field scaling and strong inversion:

W	L	β	I_{DS}	PWR	C_{ox}*W*L	Q	Δt = Q/I	$\sqrt{v_{n\_white}^2}$	SNR_w
$1/\alpha$	$1/\alpha$	α	$1/\alpha$	$1/\alpha^2$	$1/\alpha$	$1/\alpha^2$	$1/\alpha$	1	$1/\alpha$
1	$1/\alpha$	α^2	1	$1/\alpha$	1	$1/\alpha$	$1/\alpha$	$1/\alpha^{1/2}$	$1/\alpha^{1/2}$
$1/\alpha$	1	1	$1/\alpha^2$	$1/\alpha^3$	1	$1/\alpha$	α	$\alpha^{1/2}$	$1/\alpha^{3/2}$
1	1	α	$1/\alpha$	$1/\alpha^2$	α	1	α	1	$1/\alpha$
α	$1/\alpha$	α^3	α	1	α	1	$1/\alpha$	$1/\alpha$	1

To maintain the same SNR we do not gain in Power !!!

Analog power consumption

Min. power consumption for class A analog circuits:

$$P_{min} = 8\,\pi\,kT \cdot SNR \cdot f_{sig} \cdot \frac{V_{DD}}{V_{DD} - \Delta V}$$

ΔV is the fraction of the V_{DD} not used for signal swing

Optimal analog power/performance trade-off for 0.35 - 0.25 μm technologies

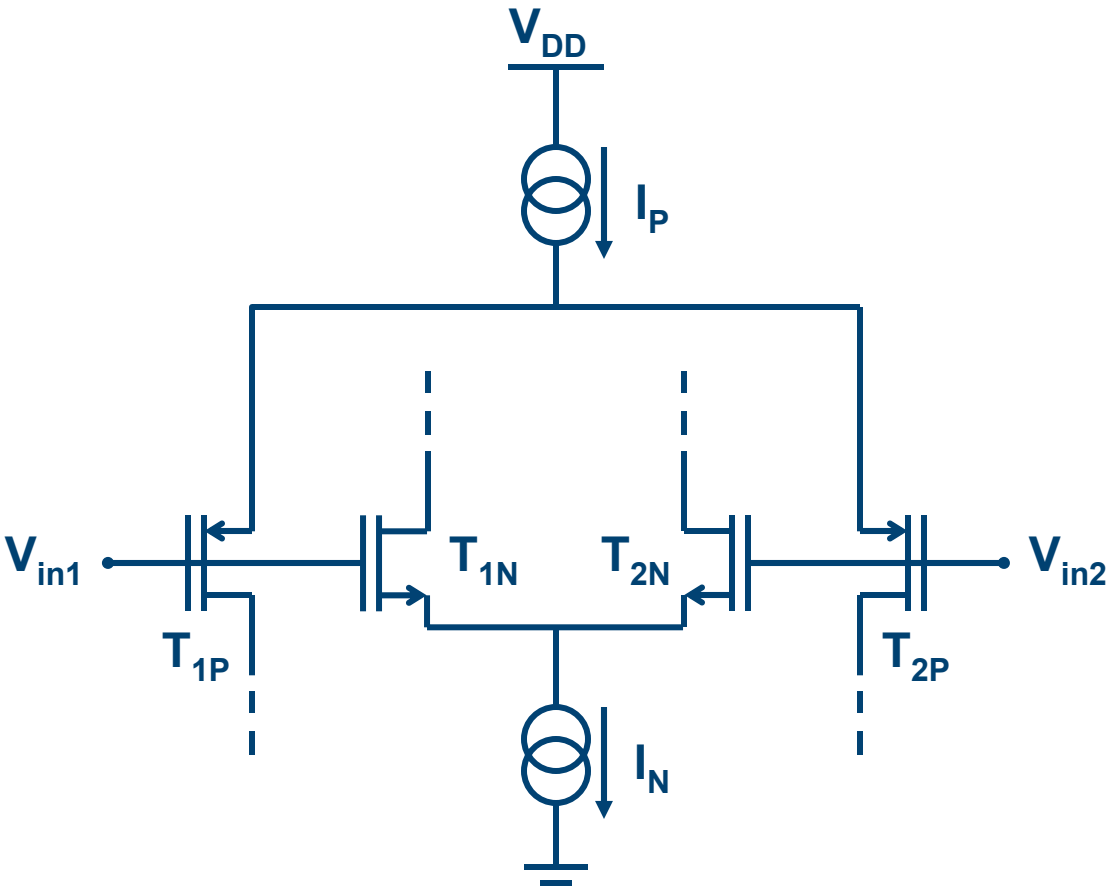
A.-J. Annema, "Analog Circuit Performance and Process Scaling", *IEEE Transactions on Circuit and System II*, vol. 46, no. 6, June 1999, pp. 711-725.

Low voltage issues

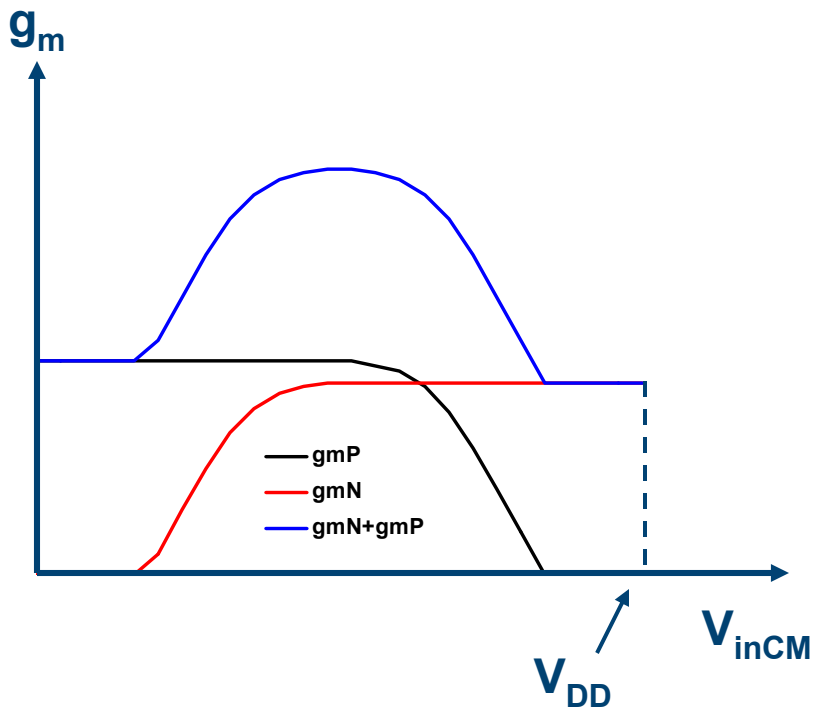
- **Use rail-to-rail input stages**
- **Low V_{DS_SAT} → Big transistors → Low speed**
- **Use low-V_T or 0-V_T transistors**
- **Use multi-gain systems to have high dynamic range**
- **Use devices in W.I. (low V_{DS_SAT} and high g_m/I_D)**
- **Use current-mode architectures**
- **Use bulk-driven MOS**
- **If very low-power is needed, this can also be obtained at the system level**

Rail-to-rail input stage

In all the solutions that we have seen up to now, the common-mode input voltage range is about V_{DD} - V_{GS} – V_{DS_SAT}. This can cause some problems, especially if we want to use the op amp as a buffer or if the power supply voltage is quite low.



This solution has the drawback of having a variable total transconductance



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  - Digital noise
  - Substrate noise
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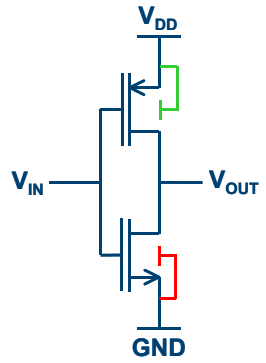
Digital noise in mixed-signal ICs

Integrating analog blocks on the same chip with digital circuits can have some serious implications on the overall performance of the circuit, due to the influence of the "noisy" digital part on the "sensitive" analog part of the chip.

The switching noise originated from the digital circuits can be coupled in the analog part through:

- **The power and ground lines**
- **The parasitic capacitances between interconnection lines**
- **The common substrate**



The substrate noise problem is the most difficult to solve.

• A. Samavedam et al., "A Scalable Substrate Noise Coupling Model for Design of Mixed-Signal IC's", *IEEE JSSC*, vol. 35, no. 6, June 2000, pp. 895-904.
• N. K. Verghese and D. J. Allstot, "Computer-Aided Design Considerations for Mixed-Signal Coupling in RF Integrated Circuits", *IEEE JSSC*, vol. 33, no. 3, March 1998, pp. 314-323.
• M. Ingels and M. S. J. Steyaert, "Design Strategies and Decoupling Techniques for Reducing the Effects of Electrical Interference in Mixed-Mode IC's", *IEEE Journal of Solid-State Circuits*, vol. 32, no. 7, July 1997, pp. 1136-1141.

Noise reduction techniques

- Quiet the Talker. Examples (if at all possible !!!):
  - Avoid switching large transient supply current
  - Reduce chip I/O driver generated noise
  - Maximize number of chip power pads and use on-chip decoupling
- Isolate the Listener. Examples:
  - Use on-chip shielding
  - Separate chip power connections for noisy and sensitive circuits
  - Other techniques depend on the type of substrate. See next slide
- Close the Listener's ears. Examples:
  - Design for high CMRR and PSRR
  - Use minimum required bandwidth
  - Use differential circuit architectures
  - Pay a lot of attention to the layout

•N. K. Verghese, T. J. Schmerbeck and D. J. Allstot, "Simulations Techniques and Solutions for Mixed-Signal Coupling in Integrated Circuits", Kluwer Academic Publishers, Boston, 1994.

Different types of substrates

There are mainly two types of wafers:

1. **Lightly doped wafers: “high” resistivity, in the order of 10 Ω-cm.**

2. **Heavily doped wafers: usually made up by a “low” resitivity bulk (~ 10 mΩ/cm) with a “high” resistivity epitaxial layer on top.**

TSMC, UMC, IBM and STM (below 180 nm) offer type 1

Substrate noise reduction techniques

- In the case of a lightly doped substrate we can:
  - Use guard rings around the sensitive circuits to isolate them from the noisy circuits. Guard rings (biased separately) can also be used around the noisy circuits
  - Separate the sensitive and the noisy circuits
- For a heavily doped substrate, the above mentioned techniques are not very effective. The best option in this case is to have a good backside contact to have a low impedance connection to ground.
- In both cases, but especially with heavily doped substrates, it is a good idea to separate the ground contact from the substrate contact in the digital logic cells, to avoid to inject the digital switching current directly into the substrate.

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Available features and devices

- Shallow Trench Isolation (STI)
- Cobalt salicided N^+ and P^+ polysilicon and diffusions
- Low K dielectrics for interconnections
- Vertical Parallel Plate (VPP) capacitors and MOS varactors

Options:

- Multiple gate oxide thicknesses (→ supply voltages)
- Several different metal options
- Resistors: diffusion, poly, metal
- Triple well NMOS
- Low-V_T, High-V_T, Zero-V_T devices (thin and thick oxides)
- Metal-to-metal capacitors
- Electronic fuses
- Inductors

Conclusions

- The future of analog design in deep submicron processes in the 180 nm – 100 nm range looks quite promising. But it will not be straightforward for analog circuit to have the required SNR and speed without increasing the power dissipation.
- For analog applications in which speed and density are important, scaling can be very beneficial.
- It is clear that scaling brings some very important benefits for digital circuits. Digital circuits are profiting more from scaling than analog circuits. Example: in a mm^2 we can fit 200.000 gates running at 1 GHz and dissipating 0.8 W, or we could fit a full ARM microprocessor.
- This suggests that, within an ASIC, the position of the ideal separation line between analog and digital circuitry will have to be reconsidered.
- The problem of the substrate noise will have to be studied in detail.

Acknowledgements

I would like to especially thank:

- The conference organizers for giving me the opportunity to give this talk
- Federico Faccio and Alessandro Marchioro for many useful comments
- Alessandro La Rosa for the 0.13 μm noise measurements
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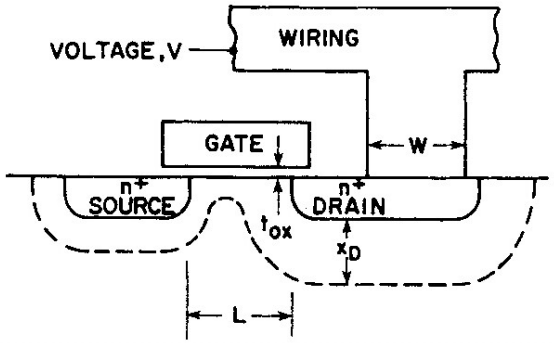
- Gianluigi De Geronimo, Paul O'Connor and Veljko Radeka for providing a very good working environment during my visit at BNL and for many useful discussions

SPARE

SLIDES

Constant field scaling



Width of a depleted zone as a function of the bias V $x_d = \sqrt{\frac{2\varepsilon_{Si}}{qN_A}}\sqrt{\phi_{bi} + V}$

Threshold voltage of a MOS transistor $V_T = V_{FB} + \phi_0 + \frac{\sqrt{2 \cdot q \cdot \varepsilon_{Si} \cdot N_A}}{C_{ox}}\sqrt{\phi_0 + V_{SB}}$

$$L \downarrow \rightarrow x_d \downarrow \rightarrow N_A \uparrow \text{ and } V \downarrow \rightarrow V_{DD} \downarrow$$

$$N_A \uparrow \rightarrow V_T \uparrow \rightarrow t_{ox} \downarrow$$

Generalized selective scaling

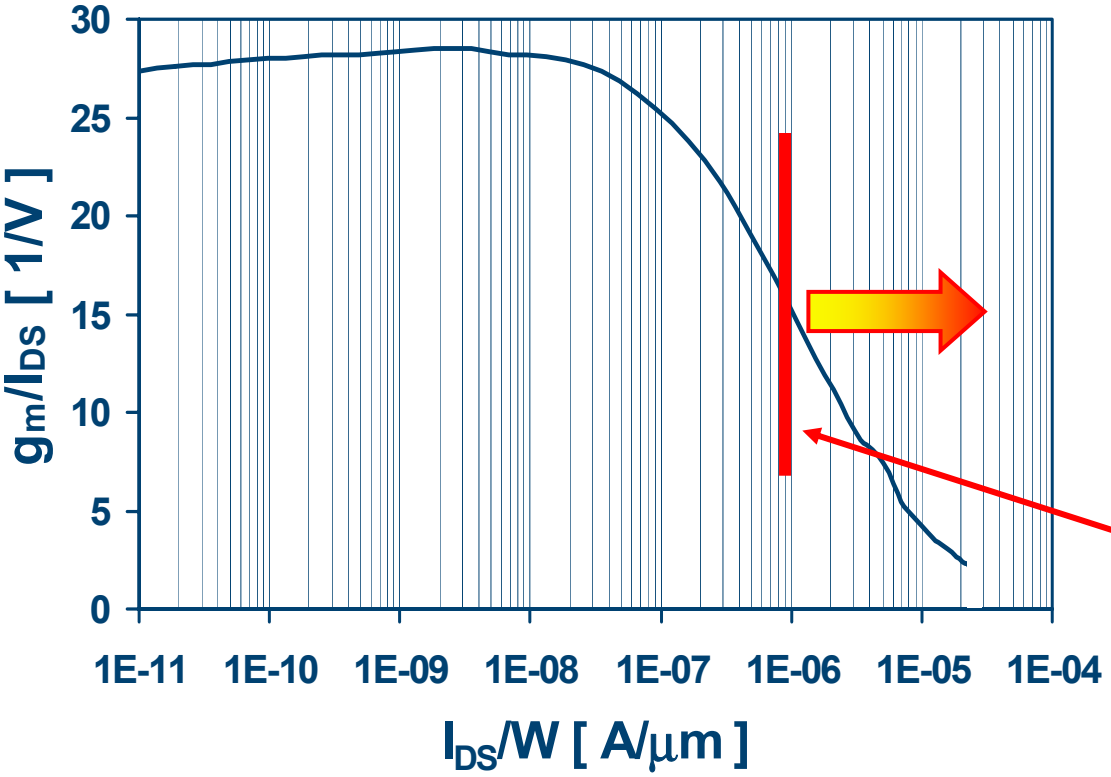
Physical parameter	Constant-Electric Field Scaling Factor	Generalized Scaling Factor	Generalized Selective Scaling Factor
Channel length, Insulator thickness	$1/\alpha$	$1/\alpha$	$1/\alpha_d$
Wiring width, channel width	$1/\alpha$	$1/\alpha$	$1/\alpha_w$
Electric field in device	1	ε	ε
Voltage	$1/\alpha$	ε/α	ε/α_d
On-current per device	$1/\alpha$	ε/α	ε/α_w
Doping	α	$\varepsilon\alpha$	$\varepsilon\alpha_d$
Area	$1/\alpha^2$	$1/\alpha^2$	$1/\alpha_w^2$
Capacitance	$1/\alpha$	$1/\alpha$	$1/\alpha_w$
Gate delay	$1/\alpha$	$1/\alpha$	$1/\alpha_d$
Power dissipation	$1/\alpha^2$	ε^2/α^2	$\varepsilon^2/\alpha_w\alpha_d$
Power density	1	ε^2	$\varepsilon^2\alpha_w/\alpha_d$

α is the dimensional scaling parameter, ε is the electric field scaling parameter, and α_D and α_W are separate dimensional scaling parameters for the selective scaling case. α_D is applied to the device vertical dimensions and gate length, while α_W applies to the device width and the wiring.

D. J. Frank et al., "Device Scaling Limits of Si MOSFETs and Their Application Dependencies", *Proc. IEEE*, vol. 89, no. 3, March 2001, pp. 259-288.

Weak inversion region width

t_{ox} scales ⟶ for the same device dimensions the boundary between weak inversion and strong inversion moves towards higher currents



$$I_{DS\_w.i.\_to\_s.i.} = 2\mu C_{ox}\frac{W}{L}n\phi_t^2$$

Scaling impact on μC_{ox}

Due to the scaling of the gate oxide thickness, the specific gate capacitance C_{ox} increases with scaling. This increases the transistor driving capability. For a given W/L ratio and a fixed bias current, the transconductance also increases with scaling.

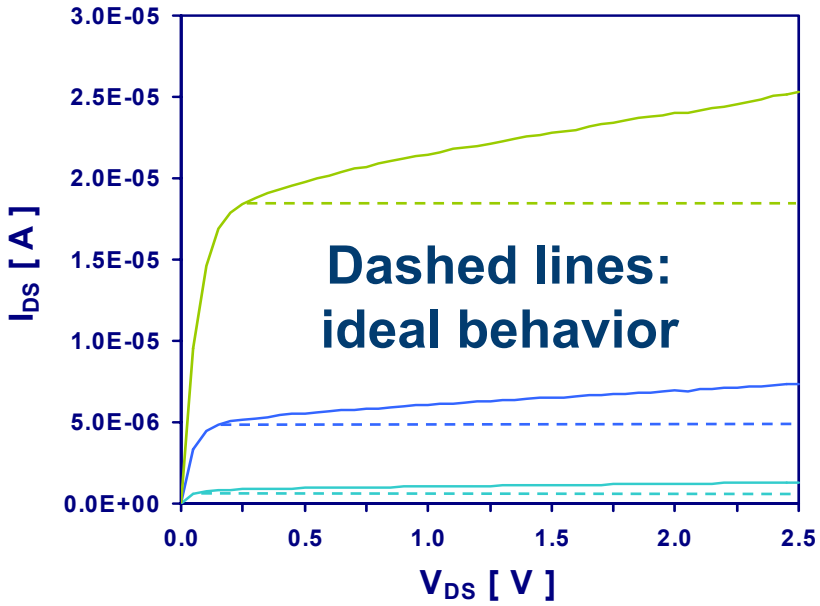
$$g_m = \sqrt{2\frac{\beta}{n} I_{DS}} = \frac{\beta}{n}(V_{GS} - V_T) \qquad \beta = \mu\, C_{ox} \frac{W}{L} \qquad C_{ox} = \frac{\varepsilon_{SiO_2}}{t_{ox}}$$

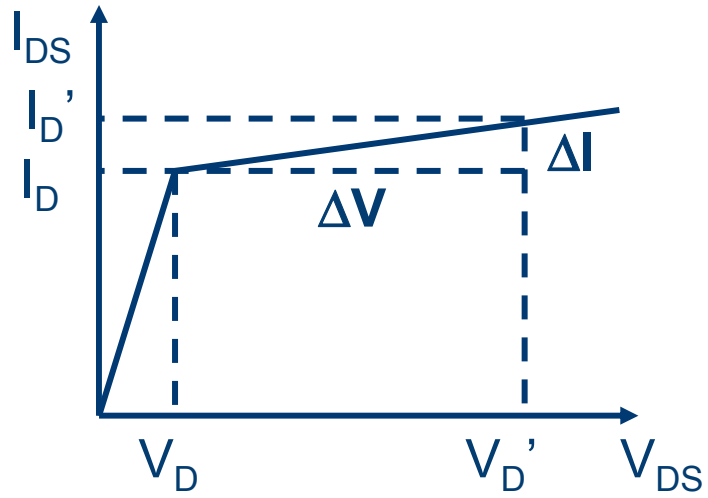
L_{min} [μm]	$t_{ox\_physical}$ [nm]	$t_{ox\_effective}$ [nm]	C_{ox} [fF/μm^2]	μC_{ox} [μA/V^2]
0.8	17	---	2.03	~ 90
0.5	10	---	3.45	~ 134
0.25	5.5	6.2	5.5	~ 250
0.18	4.1	---	---	~ 340
0.13	2.2	3.15	10.9	~ 490

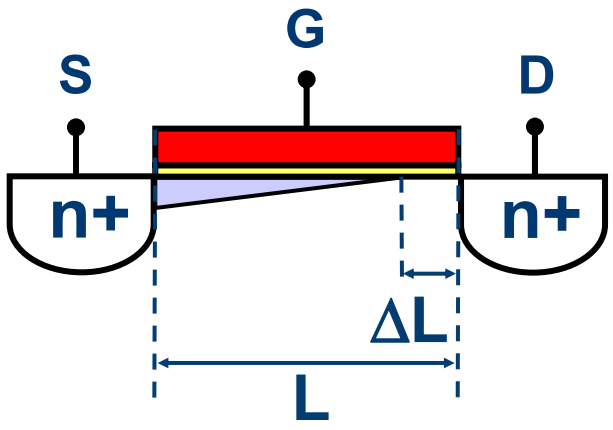
The values above are taken from measurements, design manuals or obtained from simulations. The μC_{ox} values are for NMOS transistors with low vertical field.

N. D. Arora et al., "Modeling the Polysilicon Depletion Effect and Its Impact on Submicrometer CMOS Circuit Performance", *IEEE Transactions on Electron Devices*, vol. 42, no. 5, May 1995, pp. 935-943.

Output conductance

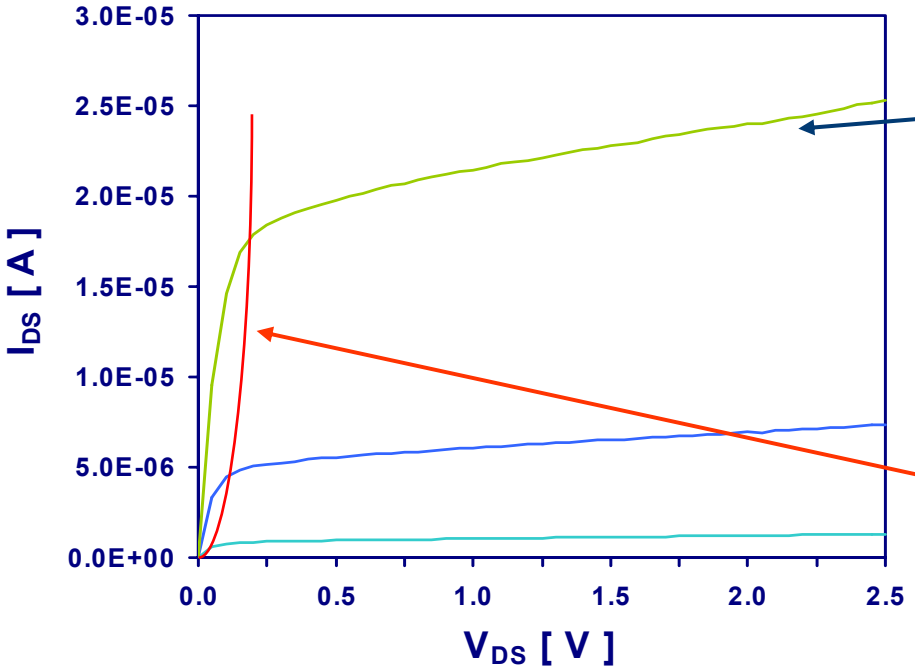






$$G_{out} = \frac{\Delta I}{\Delta V} = \frac{I_D}{\Delta V} \cdot \frac{\Delta L}{L - \Delta L}$$

Output resistance r_0



$$I_{DS} = \frac{\beta}{2n}(V_{GS} - V_T)^2(1 + \lambda V_{DS})$$

$$V_{DS\_SAT} = \frac{V_{GS} - V_T}{n}$$

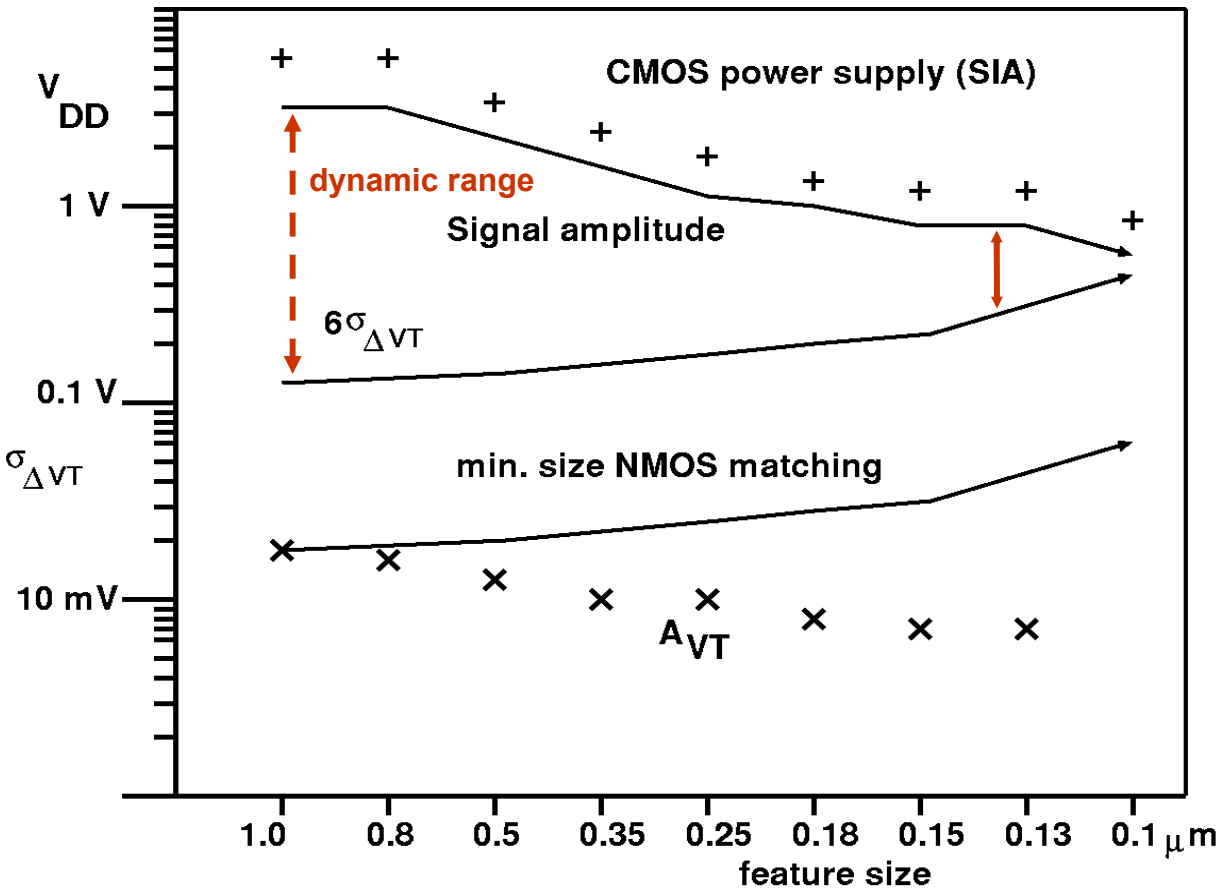
$$I_{DS\_SAT} = \frac{\beta}{2n}(V_{GS} - V_T)^2 = \frac{\beta}{2} n V_{DS\_SAT}^2$$

$$g_{out} = g_{ds} = \frac{\partial I_{DS}}{\partial V_{DS}} = \lambda \cdot I_{DS\_SAT}$$

$$r_0 = \frac{1}{g_{ds}} = \frac{1}{\lambda \cdot I_{DS\_SAT}} = \frac{V_E \cdot L}{I_{DS\_SAT}}$$

$$\lambda = \frac{1}{V_{DS} - V_{DS\_SAT}} \cdot \frac{\Delta L}{L - \Delta L} \approx \frac{1}{V_{DS} - V_{DS\_SAT}} \cdot \frac{\Delta L}{L}$$

Scaling impact on matching

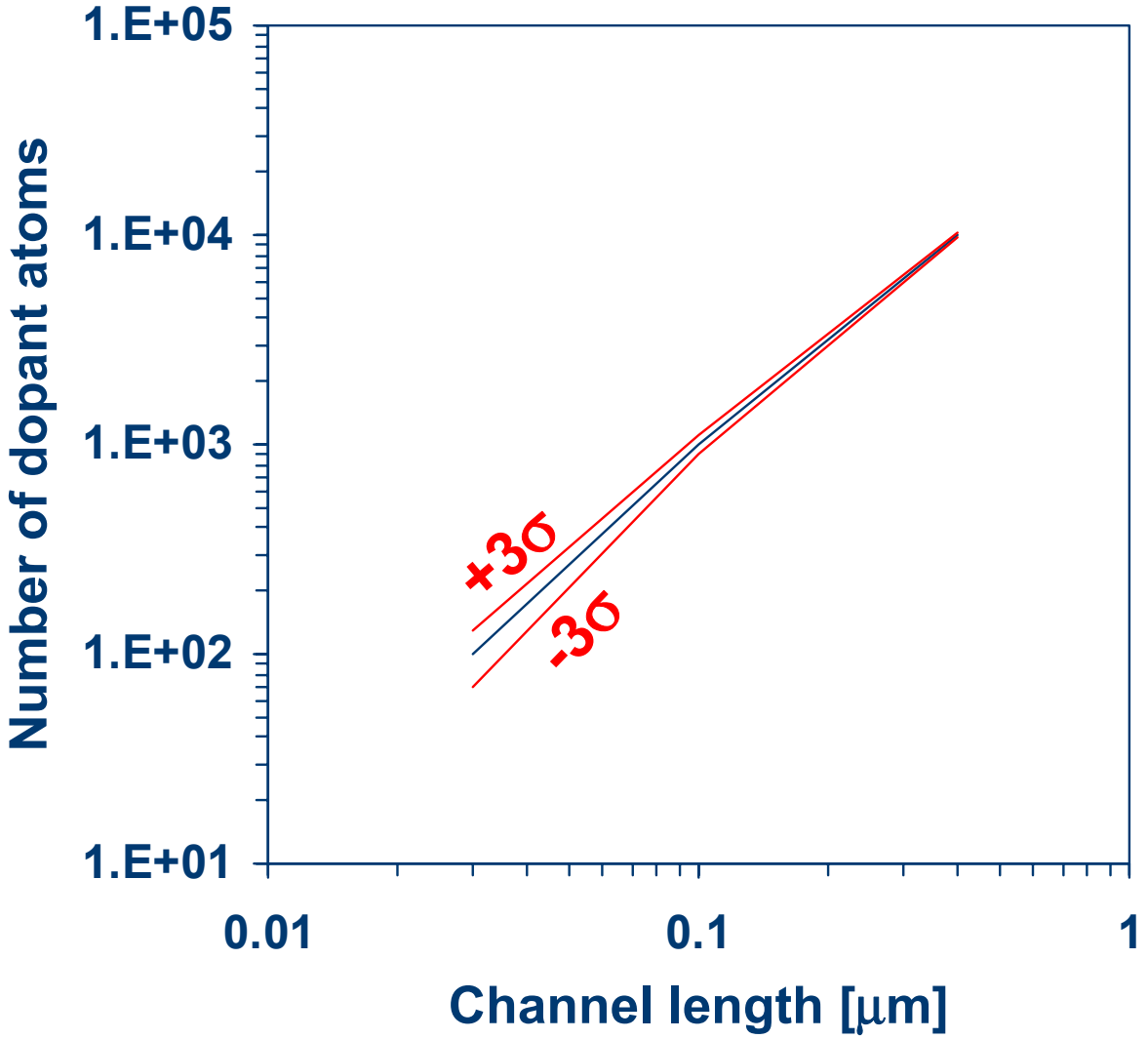


$$\sigma_{\Delta V_{th}} = \frac{A_{Vth}}{\sqrt{W\,L}}$$

Matching will have a very important impact on the performance of deep submicron CMOS circuits

M.J.M. Pelgrom et al., "Transistor matching in analog CMOS applications", *Technical Digest of the International Devices Meeting 1998*, pp. 915-918.

Scaling impact on matching (2)



The ion implantation process follows Poisson statistics. Therefore, the uncertainty in the number of dopant implanted is given by the square root of the number.

The error becomes proportionally more important for smaller devices! (=1/√N)

Scaling & dopant fluctuations

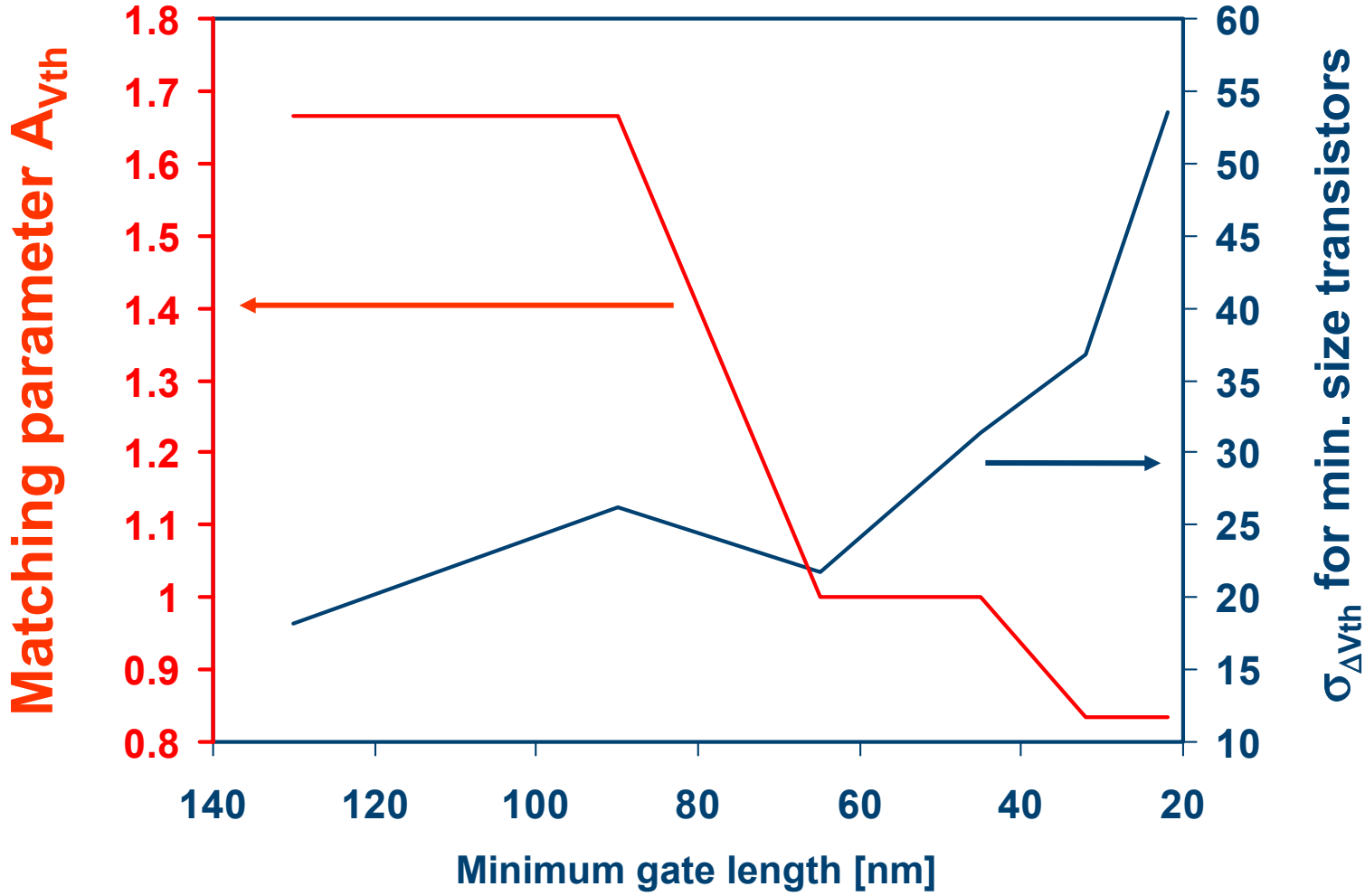
$$\sigma_{\Delta V_{th}} = C \cdot \frac{t_{ox} \cdot \sqrt[4]{N}}{\sqrt{W\,L}}$$

- For the same device dimensions, matching improves
- For minimum size devices, matching might be worse

L_{min} [μm]	t_{ox} [nm]	N_a [cm^{-3}]	A_N / t_{ox} [mV·μm / nm]	A_N [mV·μm]	$\sigma_{\Delta Vth}$ [mV]	$6 \cdot \sigma_{Vth}$ [mV]
1.2	25	$5 \cdot 10^{16}$	0.328	8.2	6.84	29
1	20	$6 \cdot 10^{16}$	0.344	6.9	6.89	29.2
0.8	15	$7.5 \cdot 10^{16}$	0.365	5.5	6.84	29
0.5	10	$1.2 \cdot 10^{17}$	0.414	4.1	8.28	35.1
0.25	5.5	$2.4 \cdot 10^{17}$	0.498	2.7	11	46.5
0.18	4	$3.3 \cdot 10^{17}$	0.542	2.2	12	51.1

P.A. Stolk et al., "Modeling Statistical Dopant Fluctuations in MOS Transistors", *IEEE Trans. Elect. Dev.*, vol. 45, no. 9, Sept. 1998 , pp. 1960-1971.

Matching data from the Roadmap



Data taken from The International Technology Roadmap for Semiconductors (2001 Edition)

Analog power consumption (2)

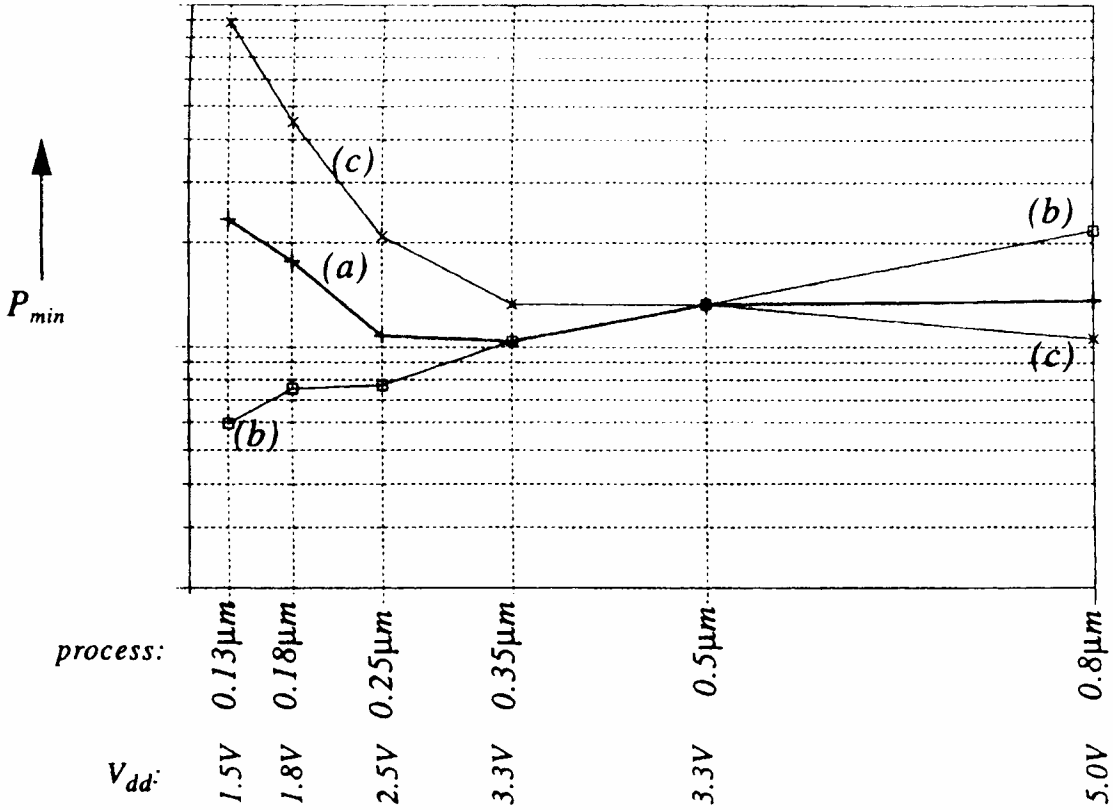


Fig. 8. Minimum power consumption for a voltage follower circuit (with constant topology, SINAD and maximum signal frequency). (a) Made in various processes, operated at their corresponding supply voltages. (b) Made in various processes, all operated at $V_{dd} = 3.3$ V. (c) All made in 0.5-μm CMOS, operated at various supply voltages.

Speed-power-accuracy trade off

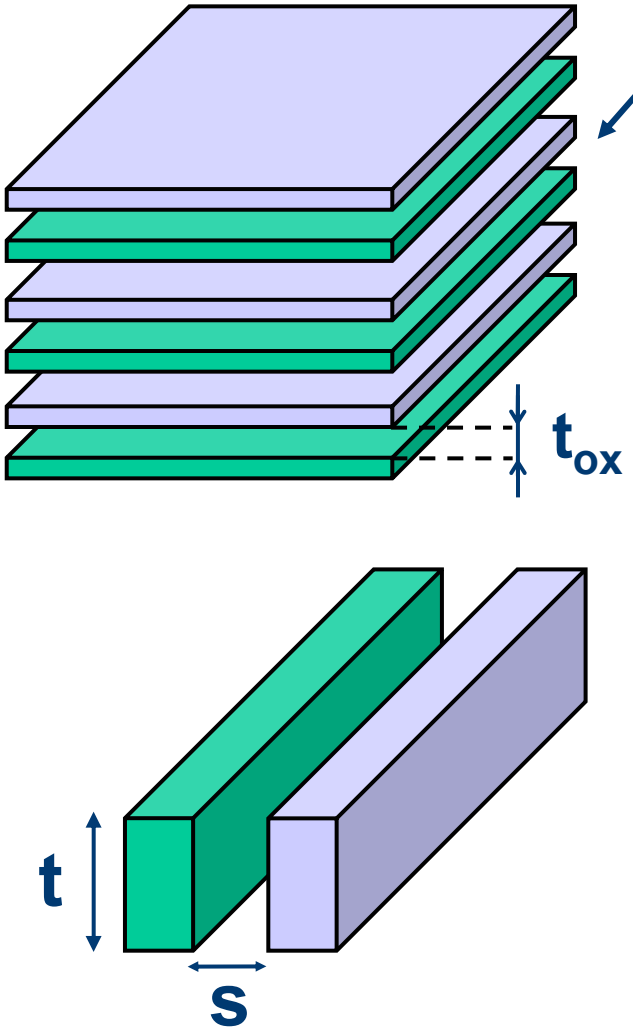
$$\text{Speed} \propto \frac{g_m}{WLC_{ox}}$$

$$\sigma_{\Delta V_{th}} = \frac{A_{V_{th}}}{\sqrt{WL}} \qquad \text{Accuracy} \propto \frac{V_{DD}}{\sigma_{\Delta V_{th}}} = \frac{V_{DD}}{A_{V_{th}}} \cdot \sqrt{WL}$$

$$\text{Power} \propto I \cdot V_{DD}$$

$$\frac{\text{Speed} \cdot \text{Accuracy}^2}{\text{Power}} \propto \left(\frac{g_m}{I}\right) \cdot \frac{V_{DD}}{C_{ox} \cdot A_{V_{th}}^2}$$

Multi-metal-layer capacitors



This solution is a possibility, but it does not exploit the fact that in deep submicron processes the highest parasitic capacitance can be obtained "horizontally" rather than vertically, i.e. $t_{ox} > s$

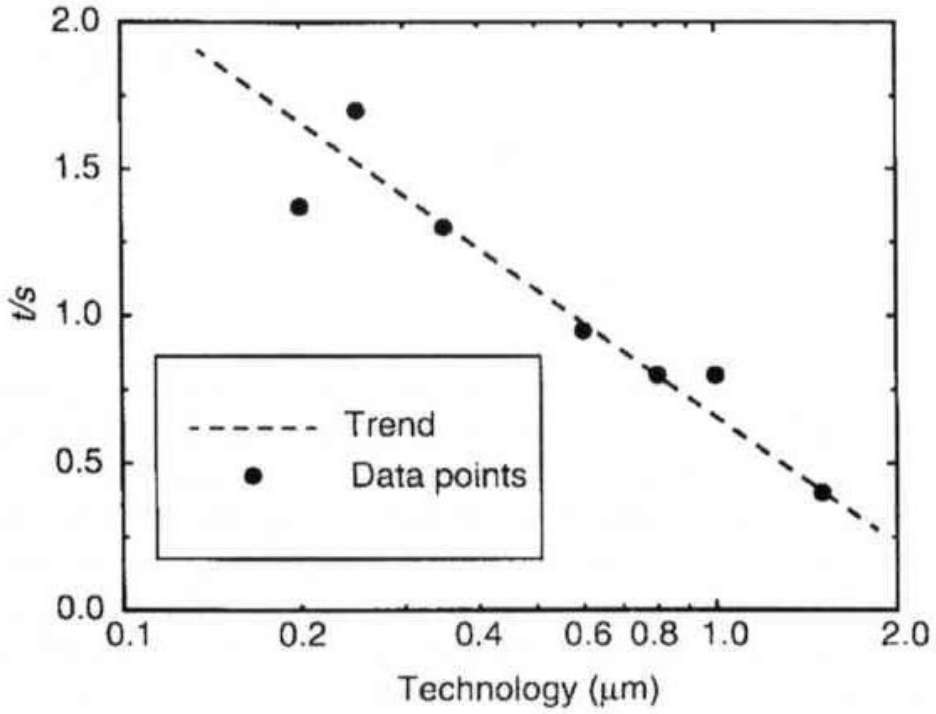
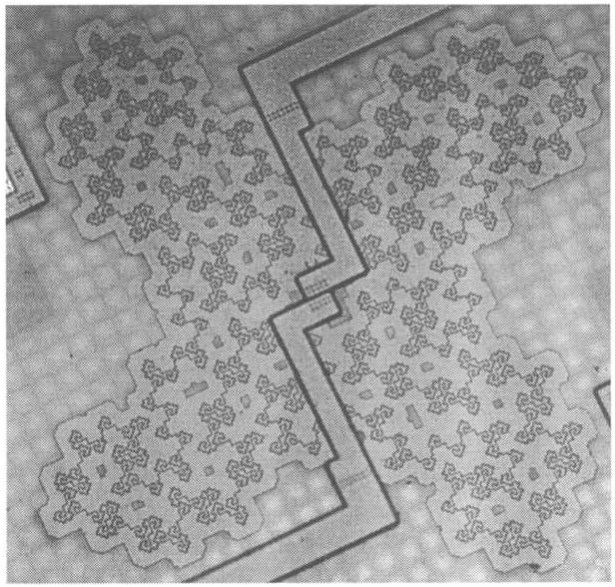
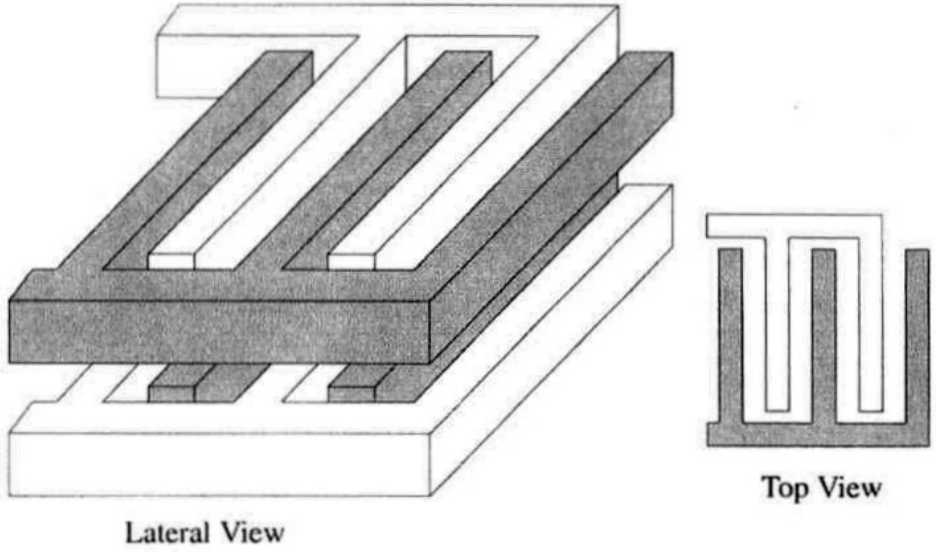


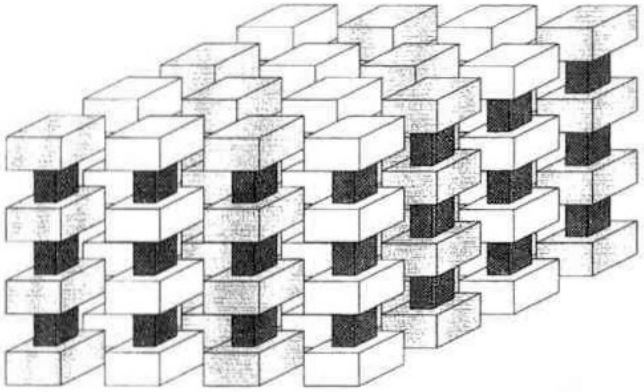
Fig. 3. Ratio of metal thickness to horizontal metal spacing versus technology (channel length).

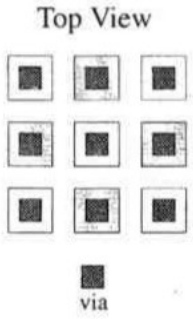
- **Hirad Samavati et al., "Fractal Capacitors", *IEEE Journal of Solid-State Circuits*, vol. 33, no. 12, December 1998, pp. 2035-2041.**

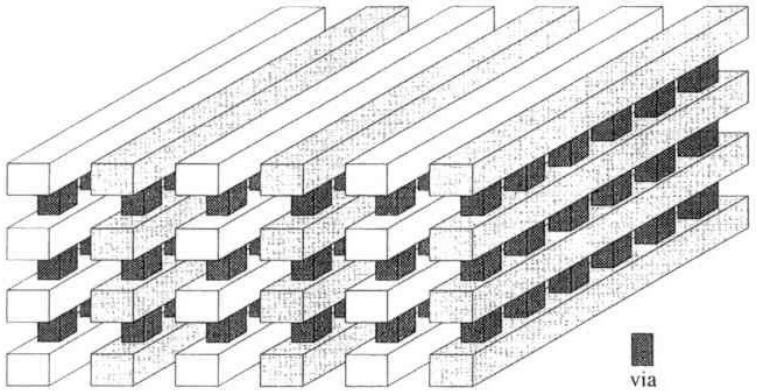
Multi-metal-layer capacitors











- **Hirad Samavati et al., "Fractal Capacitors", *IEEE Journal of Solid-State Circuits*, vol. 33, no. 12, December 1998, pp. 2035-2041.**
- **R. Aparicio and A. Hajimiri, "Capacity Limits and Matching Properties of Integrated Capacitors", *IEEE JSSC*, vol. 37, no. 3, March 2002, pp. 384-393.**