

# SEU Robustness, Total Dose Radiation Hardness and Analogue Performance of the Beetle Chip

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## *Abstract*

The Beetle is a 128 channel readout chip for silicon strip detectors in LHCb. In addition to the pipelined readout path known from the RD20 architecture which can be used either in analogue or binary mode, the Beetle features an additional prompt binary readout path, used for the LHCb pile-up veto counters and a triple-redundant layout of the control logic. It is manufactured in commercial 0.25  $\mu\text{m}$  CMOS technology using radiation hard design techniques.

In addition to a total dose irradiation with X-rays, an SEU irradiation test with 65 MeV protons was performed with Beetle1.3. The results of this test are presented together with new results from the Beetle versions 1.3, 1.4 and 1.5, which were submitted in the Beetle\_ER engineering run in May 2004.

## I. THE BEETLE CHIP ARCHITECTURE

The Beetle [1] is an analogue pipelined readout chip and implements the RD20 front-end architecture [2]. For a fast trigger decision it provides a comparator with prompt binary output signals. Using the comparator output signals instead of analogue front-end signals, the Beetle can alternatively operate in a binary pipelined mode. Figure 1 shows a schematic block diagram of the latest versions Beetle1.2 to 1.5. The chip integrates 128 channels. Each channel consists of a low-noise charge sensitive preamplifier, an active

CR-RC pulse shaper and a buffer. For capacitive loads  $\leq 50$  pF the chip achieves rise times  $\leq 25$  ns and spillover of  $\leq 30\%$  of the maximum at 25 ns after the peak, suitable for operation within the LHCb experiment. The chip provides two different readout paths. For the binary readout the front-end's output couples to a comparator which features invertable outputs to detect input signals of either polarity and individually adjustable threshold levels. Four adjacent comparator outputs are logically ORed, latched, multiplexed by 2 and routed off the chip via low voltage differential signaling (LVDS) ports at 80 MHz. The pipelined readout path can operate in either a binary mode by using the comparator outputs or an analogue mode by sampling the front-end buffer's output with the LHC bunch-crossing frequency of 40 MHz. The sampled amplitudes are stored in an analogue memory (pipeline) with a programmable latency of at maximum 160 sampling intervals. This is combined with an integrated trigger buffer of 16 stages. Upon a trigger the corresponding signals stored in the pipeline are transferred to the multiplexer via a resettable charge sensitive amplifier. The number of active output ports is configurable and allows a readout time of at minimum 900 ns per event. The output of a sense channel is subtracted from the analogue data to compensate common mode effects. On-chip digital-to-analogue converters (DACs) with a resolution of 8 bits generate the bias currents and control voltages. For test and calibration purposes, an adjustable charge injector is implemented on each channel. All bias settings and configuration parameters, e.g. trigger latency, readout mode and readout speed, can be programmed and read back via a standard I<sup>2</sup>C-interface [3]. All digital I/Os, except for

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the I<sup>2</sup>C-lines and the daisy chain ports, use LVDS signals.

The Beetle is designed in a commercial 0.25  $\mu\text{m}$  CMOS technology and has a die size of  $6.1 \times 5.4 \text{ mm}^2$ . The pitch of the analogue input pads is 40.24  $\mu\text{m}$ . If no prompt readout is required, the chips can be mounted side-by-side, since no connections to the top and bottom side of the chip are required. This allows an overall pitch of 50  $\mu\text{m}$  matching the readout pitch of typical high resolution silicon strip detectors. In case of the silicon vertex detector, the readout chip will be positioned only 5 cm from the LHC beams, which means that the Beetle has to be radiation hard. The chip is designed to withstand a total dose in excess of 10 Mrad (100 kGy) by taking the following design measures [4]: forced bias currents are used in all analogue stages instead of fixed node voltages; enclosed gate structures for NMOS transistors suppress increasing leakage currents under irradiation; a consistent use of guard rings minimises the risk of Single Event Latch-up (SEL) [5].

## II. CHIP PERFORMANCE

Most analogue measurements performed on the previous versions of the Beetle chip have been repeated with Beetle1.3. Measurements of pulse-shapes gain and noise (tab. 1) were conducted, all reproducing the results presented in [6] and [7] very well. Also a comparison of the equivalent noise charges of Beetle1.3 with the results from the Beetle\_FE 1.1 frontend-only test chip was performed. It showed an only marginal degradation of the noise performance due to the stages of the pipelined readout, corresponding to a  $50 e^-$  rise in the offset parameter.

Table 1: ENC of the Beetle1.3 chip in pipelined operation mode as a function of the  $V_{fs}$  (shaper feedback) control voltage.

$V_{fs}$	Equivalent Noise Charge
0 mV	$547.7 e^- + 52.64 e^-/\text{pF}$
100 mV	$539.1 e^- + 51.89 e^-/\text{pF}$
400 mV	$542.8 e^- + 49.38 e^-/\text{pF}$
1000 mV	$465.1 e^- + 45.22 e^-/\text{pF}$

## III. THE BEETLE\_ER ENGINEERING RUN

A Production Readiness Review (PRR) for the Beetle chip was held at Heidelberg on the 20<sup>th</sup> of April 2004. It concluded that Beetle1.3 fulfils the requirements of the VeLo<sup>1</sup> and ST<sup>2</sup> detectors, but needs an improved

<sup>1</sup>Vertex Locator

<sup>2</sup>Silicon Tracker, consisting of Trigger Tracker (TT) and Inner Tracker (IT) detectors

discriminator for the application in the VETO<sup>3</sup>. Thus it concluded to place two or three versions of the chip on the reticle for an engineering run. In case of three versions in equal quantities, a subsequent production run would result in  $\approx 12500$  chips/version, while only  $\approx 3500$  are needed to equip the experiment, leaving enough margin for production yield and spares.

Therefore it was later on decided to place equal quantities of any chip version on the reticle of the engineering run.

Although the Beetle1.3 fulfils the requirements of VeLo and ST, an attempt was made to fix the remaining minor problems along with the redesign of the comparator needed in the pile-up VETO. Those include a wrongly encoded pipeline column number parity bit in consecutive readout, some cross talk between the readout lines of the pipeline, and baseline variations between consecutive and non-consecutive event readouts. The foreseen modifications were categorized into low risk and high risk, and submitted in two different designs, in order to maximize the probability of receiving a working chip that satisfies all requirements by VETO, VeLo and ST.

### A. Beetle1.3

As a backup in case the other versions would fail to qualify in time, 2 instances of the unchanged Beetle1.3 [6] [7] were placed on the reticle.

### B. Beetle1.4

This version included all changes that were considered to be a *low risk* by the PRR. These included:

- *Improved Comparator:* The linearity of the local threshold DAC was improved by better matching the components. The crosstalk or feedback<sup>4</sup> was reduced by the removal of an analogue-powered inverter stage considered to be the culprit for this effect.
- *Pipeline Column Number Parity Bit:* This bit was swapped with another (static) signal in the readout header and is thus transmitted later. This resolves the issue that the parity of the previous data frame was transmitted.
- *Beetle ID:* A version identification was included by means of some unused bits in the *CompThreshold* register, allowing the identification of different chip versions via I<sup>2</sup>C readout.
- *Alignment Markers:* Cross markers included in two positions on the chip layout facilitate automatic bonding. These unique structures enable a

<sup>3</sup>Pile-Up Veto Counters on the opposite side of the interaction point

<sup>4</sup>depending on the chosen polarity

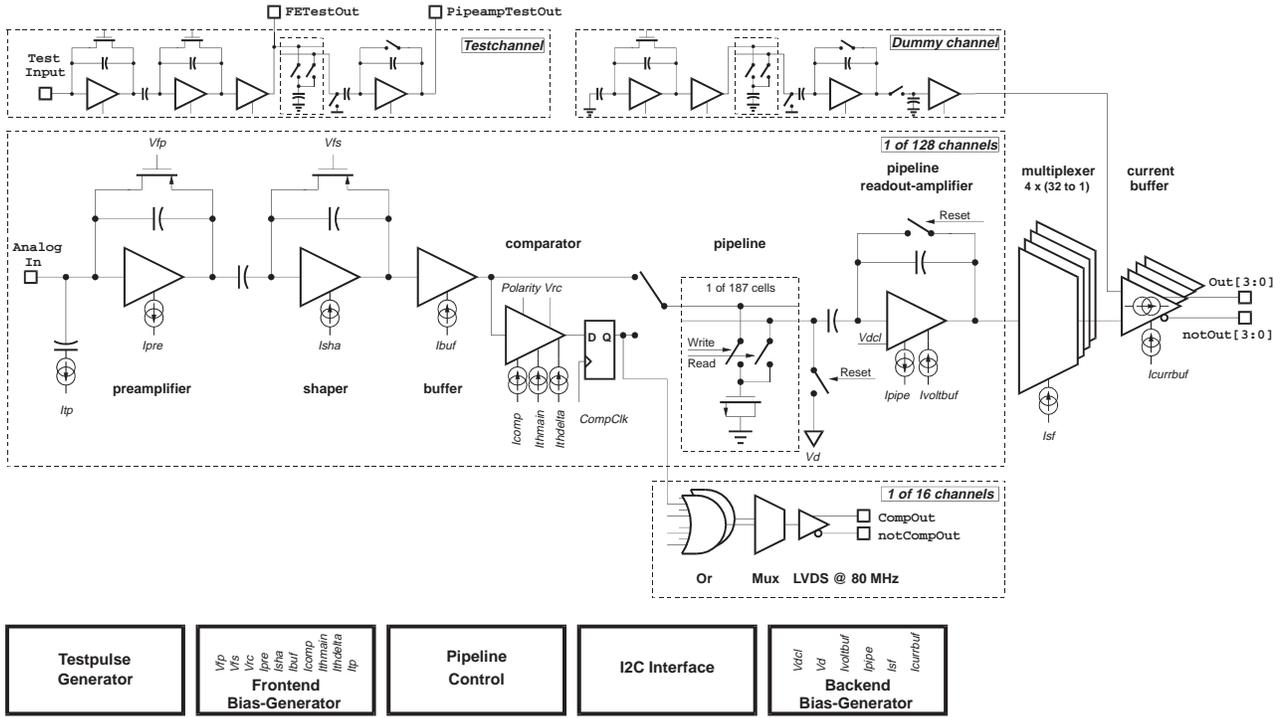


Figure 1: Block schematic of the Beetle chip.

reliable calculation of the chip's position by means of the bonding machines pattern recognition algorithm.

- *Reduced even/odd Crosstalk:* An increased spacing of the pipeline readout lines reduces the crosstalk from signals on an even channel number to the following odd one (or from an odd channel to the preceding even channel number, since capacitive coupling is symmetric) to the same value for all neighbouring channels.

The Layout of the Beetle1.4 chip is shown in fig. 2.

### C. Beetle1.5

On Beetle1.5, depicted in fig. 3, also all "high risk" changes promising an improved analogue performance were included. In addition to the changes implemented on Beetle1.4 these concern:

- *Revised Power Routing:* The power supply of some parts of the discriminator was separated from the front end. This resulted in a revised power routing of the comparator and two new power pads.
- *Pipeline Cells:* The storage capacitors of the pipeline were changed from NMOS transistors to NFET over NWELL structures. For the latter the NWELL replaces the voltage-dependent inversion channel representing one of the capacitor plates,

thus removing the voltage dependency of the capacitance and improving the chip's linearity.

- *Revised Pipeline Readout:* The Pipeline Readout Amplifier (Pipeamp) was split into 4 blocks equivalent to the multiplexer and connected with power bars to the latter (c.f. fig 3). By this the overall flatness of the readout baseline is greatly improved.

The driver tree of the pipeamp's reset signal was re-implemented, exactly equivalent to that of the multiplexers tracking signal.

Finally a misalignment of  $\approx 200$  ps between readout header and analogue data was resolved by an additional delay of some control signals.

As a result the differences between consecutive and non-consecutive readouts almost vanished.

- *Test Structure:* To monitor process parameters or radiation damage a test structure was included.
- *Improved Power Routing:* To gain full advantage from the changes in the power routing of the discriminator, pipeline readout and multiplexer, the power routing on the top and rear side of the chip was improved.
- *Different Beetle ID*

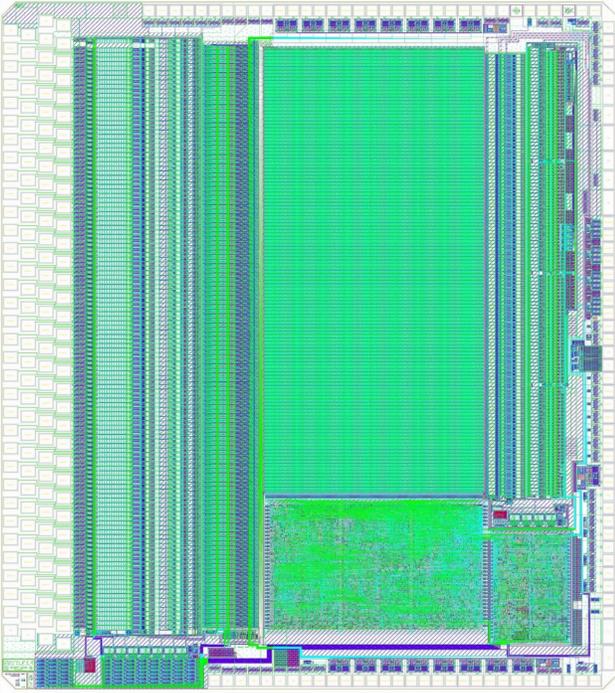


Figure 2: Layout of the Beetle1.4 chip.

#### IV. BEETLE IRRADIATION TESTS

To verify the radiation hardness of the Beetle chip and to test its SEU protection and correction mechanisms, two irradiation tests were performed.

##### A. Total Ionizing Dose Irradiation Test

A sample of 3 Beetle1.2 chips was irradiated with X-rays. Fig. 4 shows a Beetle chip in the X-ray irradiation facility at CERN. The accumulated dose achieved in the allocated time was 45 Mrad after which the chips did not show any obvious changes, neither in noise, nor in the pulse shape. A thorough investigation however revealed, that the DC-current for a 10% drop in amplitude decreased from  $\approx 210$  nA (unirradiated) to  $\approx 65$  nA (at 45Mrad), as fig. 5 shows. For 300  $\mu\text{m}$  thick silicon detectors ( $\approx 24 \times 10^3 e^-/\text{MIP}$ ), this translates to a maximum strip occupancy of  $\approx 140\%$  an unirradiated Beetle1.2 chip can read out without pile-up effects. This value drops to  $\approx 42\%$  after 45 Mrad, which is still well above the highest occupancies expected in LHCb.

##### B. SEU Test with 65MeV Protons

In February 2004 a proton irradiation of 3 Beetle1.3 chips (figs. 6 and 7) was performed with the PIF<sup>5</sup> at PSI<sup>6</sup> in Villigen (Switzerland). Two goals were pur-

<sup>5</sup>Proton Irradiation Facility

<sup>6</sup>Paul-Scherrer-Institute

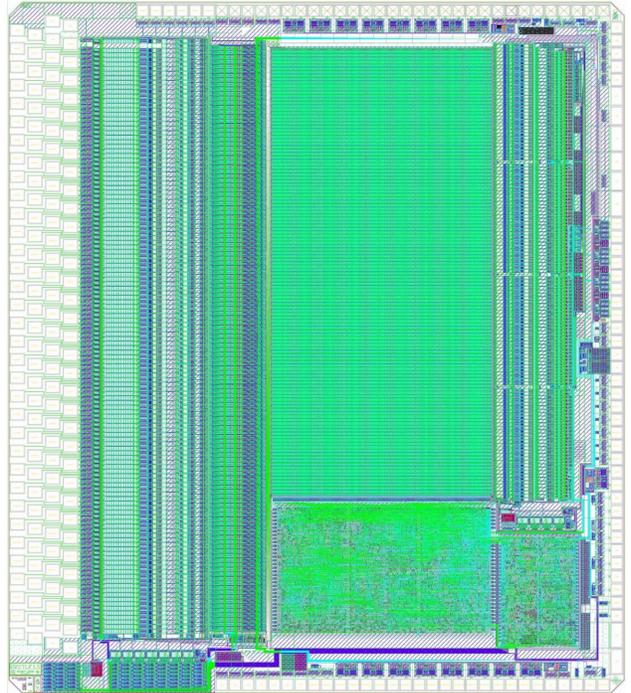


Figure 3: Layout of the Beetle1.5 chip. It can be easily distinguished from other versions by the pipeamp split into four parts.

sued with this test: A measurement of the total SEU cross section and the verification of the Beetles SEU detection and correction mechanisms.

For the latter there are 4 classes of registers on Beetle1.3 to 1.5:

- *Non-redundant registers without parity.* These are only used for the multiplexer's read bit. Since the read bit is not retrieved after leaving the last channel, an SEU can only generate a 2<sup>nd</sup> read bit, corrupting at maximum 2 data frames without any further consequences.
- *Non-redundant registers with global parity.* For area constraints, these are used in the channel-mask registers for test-pulse injection and comparator operation and for the local discriminator threshold values. Changes in the testpulse mask don't affect the chip's operation at all, while other changes only affect the discriminator operation of the chip, i.e. only in that case a reconfiguration via I<sup>2</sup>C is required. Changes in these registers are indicated in the readout data header and are also counted with the internal SEU counter.
- *Triple-redundant registers with majority voting and autocorrection.* These are used in all other static registers on the chip. The content of these registers is updated from it's majority output, if a bit flip was detected and the SEU counter is incremented.

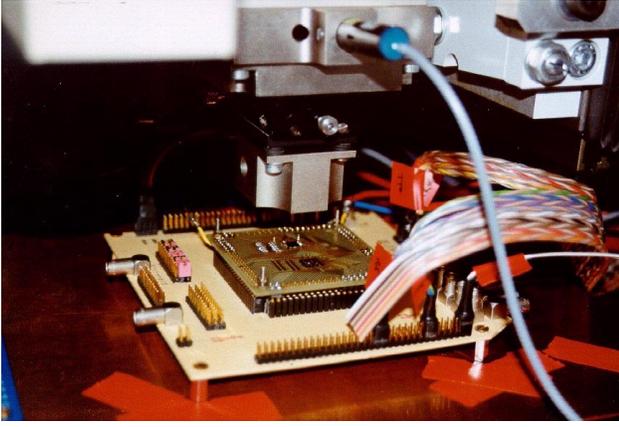


Figure 4: Beetle chip in the X-ray irradiation facility at CERN.

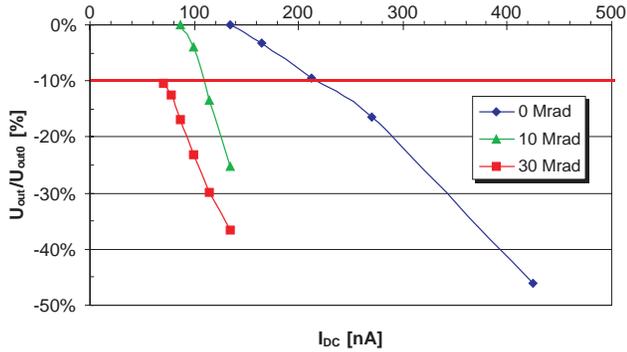


Figure 5: Relative signal amplitude as a function of the DC current into the amplifier input. For different doses in addition to the test signal, a DC current was forced into the amplifier input.

- *Triple-redundant registers with majority voting.* These are used in all state machines on the chip. Since the content of these registers is periodically updated, self-reprogramming is not required.

From this concept it is evident that all SEUs except for those in multiplexer and state machines are counted. Furthermore, uncorrected SEUs can be localised by reading back all register contents.

During a first irradiation up to 273 krad, no SEUs were encountered and in turn a second run with a flux higher by one order of magnitude was scheduled. It resulted in 4 SEUs with at least 1 SEU per chip. The results and dose profile of the two runs are given by fig. 8 and tab. 2. Strangely all 4 SEUs occurred inside a region of only 923 krad. Taking the width of this region to extract an upper limit for the SEU sensitivity, one finds

$$P = 923 \text{ krad} \cdot \frac{3 \text{ chips}}{4 \text{ SEUs}} = 692.25 \frac{\text{krad}}{\text{SEU chip}}$$

For the LHCb VeLo (1344 chips = 21 Stations á 64 Chips) and a total dose of 10 Mrad in 10 years one

calculates  $\approx 1$  SEU every 25 minutes, which does not even require a reprogramming of the chip. A similar calculation for the VETO counters (64 chips) results in  $\approx 1$  SEU in 4 days.

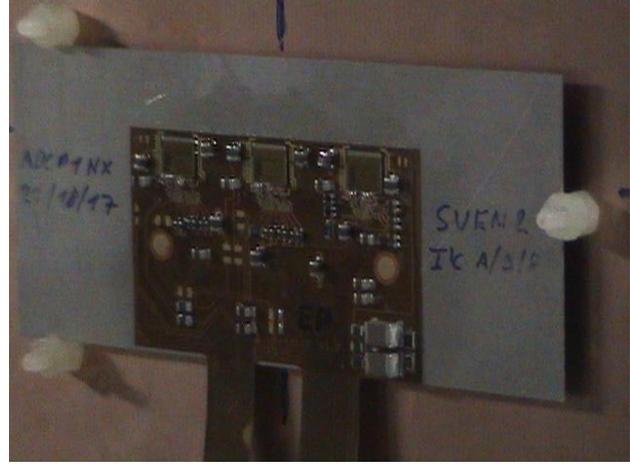


Figure 6: IT-Hybrid with 3 Beetle1.3 chips during irradiation with the PIF at PSI

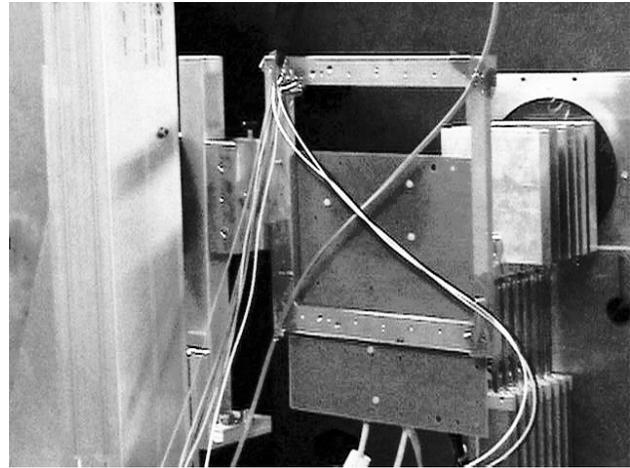


Figure 7: Proton irradiation setup at PSI. The picture is a rear view of fig. 6. The beam spot is easily visible as a discoloration around the 3 bolts holding the hybrid with the 3 Beetle chips. In the background the exit window of the proton beamline is visible.

## V. CONCLUSIONS

While Beetle1.3 already fulfills all VeLo and ST requirements, Beetle1.4 provides an improved discriminator for the VETO counters and a reduced channel crosstalk. In addition to this, Beetle1.5 fixes some minor issues, it e.g. features a flatter and more stable readout baseline.

Irradiation tests have proven, that the Beetle chip will easily stand the required total dose, while the

Table 2: Summary of the 65 MeV proton irradiation runs at PSI.

Irrad. Run	1	2
Flux	$3.13 \cdot 10^8 \text{ p s}^{-1} \text{ cm}^{-2}$	$1.56 \cdot 10^9 \text{ p s}^{-1} \text{ cm}^{-2}$
Integ. Flux	$1.95 \cdot 10^{12} \text{ p cm}^{-2}$	$5.31 \cdot 10^{13} \text{ p cm}^{-2}$
Dose	273 krad	7.66 Mrad
SEU	0	4
Analogue	unchanged	unchanged

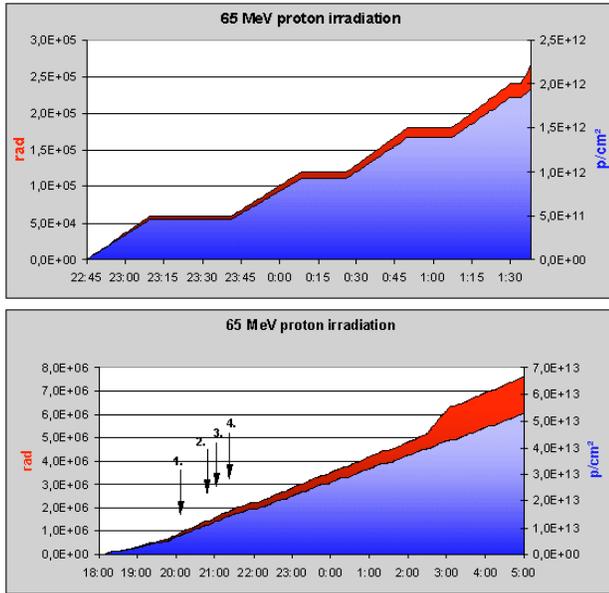


Figure 8: Integrated flux and accumulated dose on a Beetle chip as a function of time for the two 65 MeV proton irradiation runs at PSI. Top: 1<sup>st</sup> run Bottom: 2<sup>nd</sup> run.

test of its sophisticated SEU detection and correction mechanisms predict a rate of less than 1 uncorrected SEU per day.

A production run with 48 wafers is planned for the end of 2004, after the relevant Beetle versions have been qualified to the needs of the different LHCb detectors.

Currently an automated test of the chips on the wafer level is set up. It is built around a Suss PA2000 automatic probe station and sports a fast DAQ system that reads out the setup at LHCb speeds.

## V. REFERENCES

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