PACE3 : A large dynamic range analog memory ASIC assembly designed for the readout of silicon sensors in the LHC CMS Preshower.

P. Aspell [1*], D. Barney [1], W. Bialas [1, 2], J. Crooks[5], M. Dupanloup [3], A.Go [4], K. Kloukinas [1], D. Moraes [1], Q. Morrissey [5], S. Reynaud [1]

[1] CERN, 1211 Geneva 23, Switzerland

[2] AGH University of Science and Technology,
Faculty of Physics and Applied Computer Science, Krakow, Poland

[3] IPNL, 43 boulevard du 11 novembre 1918, 69622 Villeurbanne, Cedex, France

[4] NCU, Chung-Li, Taiwan

[5] Rutherford Appleton Laboratory, Didcot, OXON, UK

Abstract

This paper describes the architecture of PACE3 and the key design parameters for the large dynamic range front-end amplification and low noise analog memory.
Results from PACE3 are presented characterizing the chip's performance.

I. INTRODUCTION

The CMS silicon Preshower is a fine grain detector placed in front of the endcap ECAL. Its primary function is to detect photons with good spatial resolution in order to perform Π0 rejection.

The Preshower is designed as a 2-layer sampling calorimeter. Photons incident on lead absorbers initiate electromagnetic cascades creating showers of electrons, positrons and photons. Silicon sensors are the chosen median to detect the charged particles and measure the energy deposited by the shower.

Each silicon sensor has a total active area of 61 x 61 mm^2 and is divided into 32 strips of pitch 1.875mm with strip capacitance in the region of 50pF.

PACE3 is the front-end ASIC designed specifically for the readout of these sensors in the LHC environment. It's function is both similar to that of tracking and calorimetry electronics in that it has to detect single minimum ionising particles (MIPs) with high signal to noise ratio, for calibration purposes, and measure energy up to 400 MIPs. The dynamic range requirements on PACE3 are hence very demanding from 0.1 MIP (0.35fC) up to 400 MIPs (1400fC). A MIP signal is defined as 22000 electrons or 3.5fC of charge for 300μm of fully depleted silicon. The actual thickness of the Preshower silicon sensors is 320μm.

The upper and lower limits are dictated by two different modes of operation i.e. calibration and normal running during data taking. This has led to a two gain architectural approach in the front-end amplification. High gain (HG) for calibration purposes, offers the highest signal to noise ratio on a single MIP and low gain (LG) for normal running, offering a dynamic range up to the required 400 MIPs.

The Preshower is located in a severe radiation environment of up to 10 MRads(Si) of ionizing radiation and a fluence of $2*10^{14}$ neutrons/cm^2 over the nominal lifetime of LHC.

II. GENERAL ARCHITECTURE

The architecture of PACE3 incorporates an analog memory that stores charge signals corresponding to deposited charge on all channels during successive 25ns intervals and then selects appropriate data on reception of a first level trigger (LV1A). In order to reach the dynamic range requirements the signal levels per MIP are kept low. This means switching noise from the analog memory can become the dominant noise source if the analog memory design is not optimized. The analog memory cell in PACE3 has been extensively studied to provide an optimized design for low switching noise and high dynamic range.

Three successive analog samples are stored per LV1A and their column addresses stored in a FIFO. The analog samples are then streamed out differentially together with their associated column addresses.

The depth of the FIFO is 48 and hence data corresponding to 16 LV1A's can be simultaneously stored at any one time awaiting readout.

The analog memory itself has 32 channels, corresponding to the 32 silicon strips per sensor, with 192 columns representing 192 consecutive samples at 40MHz. This corresponds to 128 columns (required for the expected latency 3.2μs) + 48 (FIFO depth) + 16 (headroom). The internal latency is

programmable; hence if the LV1A latency is greater than 3.2μs the internal latency can be increased from 128 up to 144 clock periods using the headroom of 16. A further increase of internal latency is also possible at the expense of FIFO depth.

PACE3 is divided into two separate ASICs in order to minimise cross coupling through the substrate from the digital sampling clocks of the analog memory to the sensitive front-end . The front-end pre-amplification and shaping is contained within a chip known as Delta and the analog memory is contained within a chip called PACEAM. Both ASICs are mounted together and will be packaged together in an fpBGA for use in the experiment. Figure 1 shows the two ASICs bonded together on a test board.

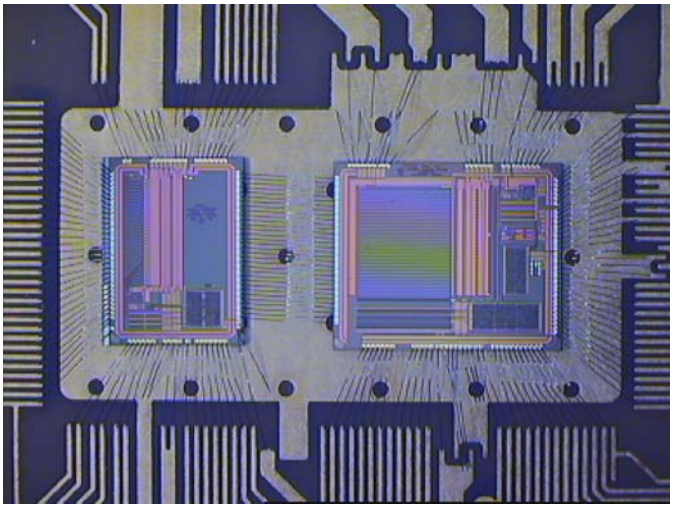

Figure 1: The two ASICs of PACE3; Delta (on the left) and PACEAM (on the right). The dimensions of the ASICs are : 3.5mm x 5mm (Delta) and 6mm x 5mm (PACEAM).

III. THE ANALOG CHANNEL

The analog channel for both Delta and PACEAM is shown in Figure 2.

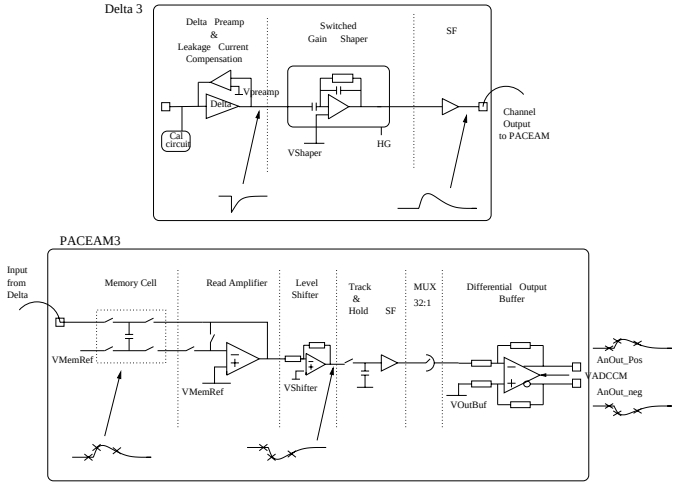

Figure 2: The analog channel within Delta and PACEAM.

The front-end chip Delta is principally an analog chip void of any sampling clock. The principle components of Delta are 32 channels of charge preamplifiers followed by a shaping stage. The Delta pre-amplifier provides a fast linear step response to collected charge over the range of 0 to 1400 fC. This charge then decays slowly over a time period of 2μs. Also associated with the pre-amplifier is a leakage current compensation circuit that allows the Delta inputs to be directly coupled to the sensor. The leakage current compensation circuit [1] deviates sensor leakage current of up to 100μA dc into itself without affecting the signal response of the circuit. The expected leakage current per strip in the Preshower is 20μA after 10 years of LHC operation.
Following the pre-amplifier is a switched gain shaper [2]. The gain is programmable via an "I^2C like" interface to one of two possible gains, LG and HG. The gain change in the shaper is obtained by switching in extra coupling capacitance to the shaper stage. At the same time the shaper transconductance is increased to obtain very similar peaking times and signal shape for the two gains.

The calculated noise for Delta is 470 e of parallel noise and a noise slope of 41e/pF as shown in Figure 3. This predicts around 2200 e noise at 50pF of sensor capacitance or a S/N ~ 10 for a signal of a single MIP.

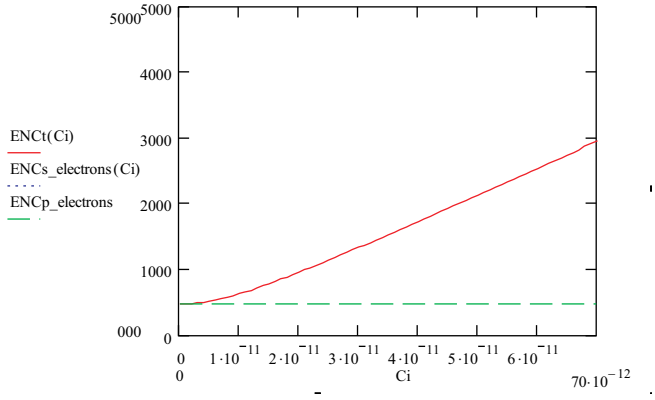

Figure 3: Calculated noise for the Delta pre-amplifier and shaper without and analog memory.

The analog channel for PACEAM is shown in the lower part of Figure 2. Bonds link the outputs of each Delta channel to the inputs of each PACEAM channel. The signal voltage from Delta is sampled onto successive analog memory capacitors each clock period.

The amplitude of the analog signal in LG is around 3mV/MIP. The noise expected due to the front-end is approximately 1/10th of this i.e. 0.3mV rms. It is clear that sampling errors or distortion due to the analog memory will therefore dominate the overall S/N ratio in LG unless great care is taken to keep these effects to an absolute minimum.. The analog memory cell itself is shown in Figure 4.

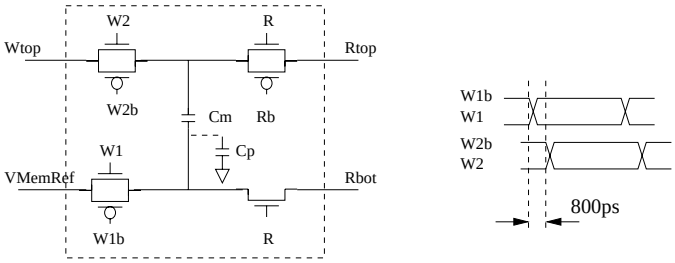

Figure 4: The analog memory cell of PACEAM.

Two effects, charge injection from the sampling switch and a low pass filter effect contribute to noise and distortion. The charge injected by a transistor switching off is dependent on the Vgs of the transistor. If the sampling switch (W2) is on the signal side of the storage capacitor (Cm) then the charge injected will be signal dependent and distortion introduced. A second sampling switch (W1) has therefore been introduced on the bottom side of the storage capacitor connected to a constant reference voltage. Turning off W1 before W2 forces a constant level of charge injection and makes it virtually independent of signal voltage. Studies showed that the level of charge injection was minimised with delay of 800ps between the turning off of W2 with respect to W1.

The low pass filter effect causes distortion by having a variable RC time constant with respect to signal voltage. It is therefore important to make the Ron of a switch as constant as possible over the signal range. This is achieved by use of both N and P MOS transistors in a switch and by optimised W/L values for both devices. The capacitor must have maximum capacitance to minimise both the voltage error due charge injection and mismatch between capacitors. It should also have a constant capacitance with respect to signal range. In the technology used a capacitor made from an NMOS structure in an NWELL maximises the capacitance per unit area. This component also exhibits a relatively flat capacitance profile (within 5%) over the signal range (0.6V to 1.8V).

IV. PACE3 MEASURED RESULTS

Measurements to qualify the circuit performance have been made using an internal programmable calibration circuit. This circuit is located in the Delta chip. The calibration circuit will also be used to cross calibrate the two gains during use in the experiment. A charge pulse may be injected to any channel via a step voltage and an injection capacitor of 1.275pF. Here 3.5fC of charge (corresponding to approximately 1 MIP) is injected per 2.75mV of voltage step. The calibration circuit is programmable through the "I^2C like" interface. Both the magnitude of the injected charge and the channel/channels to which the charge is injected can be selected. The origin of the voltage is an 8 bit DAC which must cover the full dynamic range of PACE3. It has therefore been designed with two precisions; High Precision (HP) and Low Precision (LP).

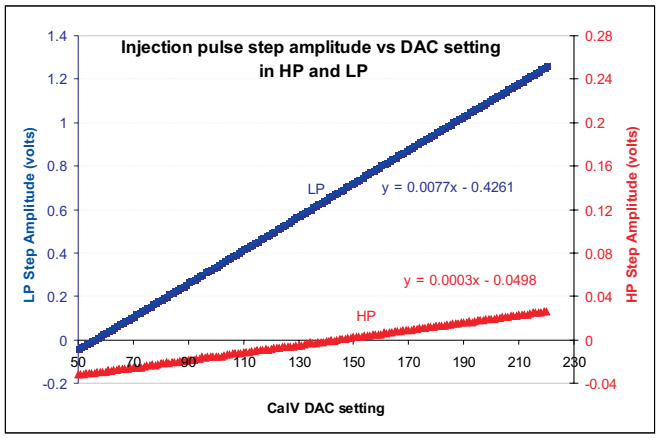

Figure 5: Measured amplitude of the internal calibration voltage step as a function of DAC setting for HP and LP.

The amplitude of the step voltage in both precisions has been measured and is shown in Figure 5. The range and precision of HP and LP is summarised in Table 1.

Table 1: Range and accuracy of the calibration circuit in both High and Low Precisions.

	Range	**mean LSB**	**σ variation from mean (LSB)**
HP	-36.6mV to 26.1mV (-13.3 MIPs to 9.5 MIPs)	0.345mV (1/8 th MIP)	2.95 μV ~ 1/900 th MIP
LP	-41.1mV to 2.12V (-14.9 MIPs to 770 MIPs)	7.68mV (2.8 MIPs)	5.81 μV ~ 1/500 th MIP

Figure 6 shows the measured signal response of Delta in HG. The peaking time is 27ns in HG and 25ns in LG. The peaking time is constant with respect to amplitude in both gains. The undershoot is 7% in both gains.

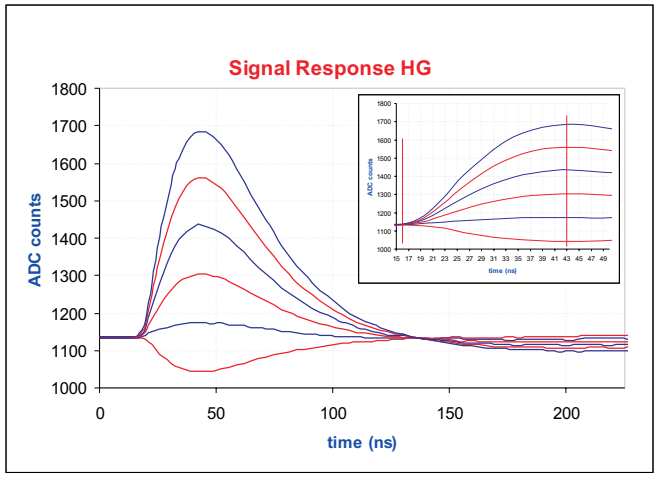

Figure 6: The signal response of Delta measured in High Gain. The inset is a zoom around the peak values to show constant peaking time.

The measured gains are 18.3mV/MIP in HG from 0 to 50 MIPs and 2.9mV/MIP in LG from 0 to 400 MIPs. The most important combinations of precision and gain are HGHP for calibration purposes and LGLP for normal running. Figures 7 and 8 show the linear region of the dynamic range for these two combinations.

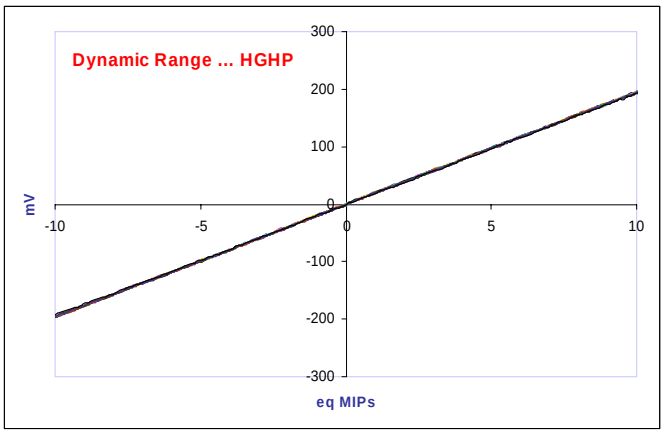

Figure 7: PACE3 dynamic range in High Gain, High Precision. All 32 channels plotted. The x-axis is the injected charge expressed as it's equivalent MIP value. The y-axis is the output voltage in mV.

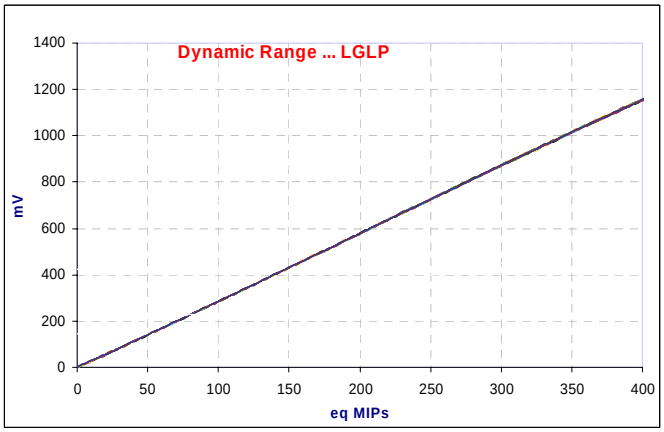

Figure 8: PACE3 dynamic range in Low Gain, Low Precision. All 32 channels plotted.

The noise has been measured across the entire analog memory. The mean noise in HG is 0.86mV rms which gives a mean S/N = 21 or the equivalent of 1047 e rms. This has been measured without a sensor connected. The distribution of noise within one channel across the 192 capacitors is shown in Figure 9.

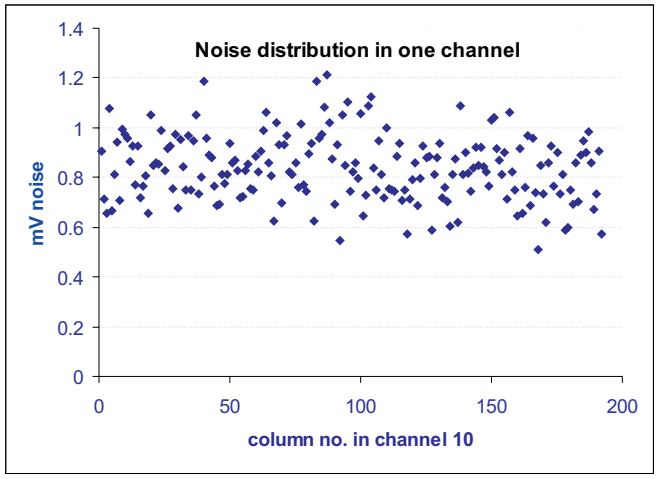

Figure 9: The noise in mV as sampled on the 192 capacitors of the analog memory in HG corresponding to a mean S/N = 21 without a sensor connected.

The pedestal variation within one channel will also contribute to noise if individual pedestal subtraction is not performed. Figure 10 shows the pedestal distribution per channel for all channels. The pedestal distribution in one channel is 0.49mV in HG and 0.365 mV in LG. The channel to channel dc offset is 3.2mV rms and is independent of gain setting.

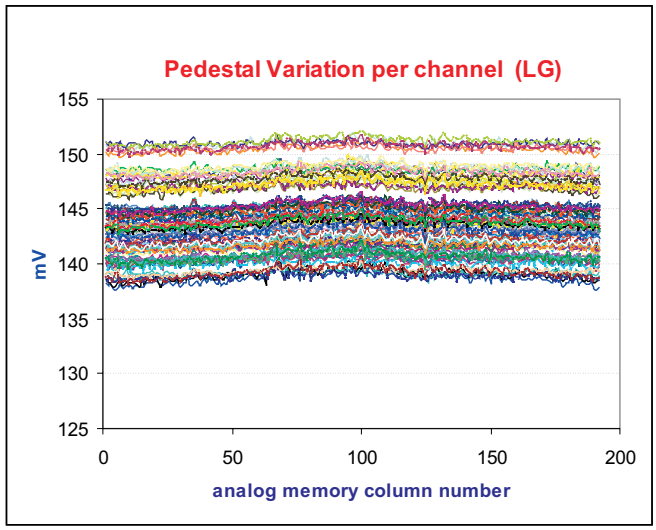

Figure 10: The pedestal variation in LG across the analog memory. Pedestals across the 192 cells for all channels are plotted.

PACE3 can be put into two modes of operation "SLEEP" and "RUN" mode. SLEEP mode powers all amplifiers down and stops the internal logic from running leaving the chip in a minimum power consuming but safe state of operation. At power-on, a power-on reset puts PACE3 directly into SLEEP mode. An "I^2C like" instruction is then used to put PACE3 in RUN mode. RUN mode powers all amplifiers to their operating levels and allows the internal logic to function as normal for data taking. The power consumption has been measured as 10mW in SLEEP mode and 650 mW in RUN mode.

V. Radiation Tolerance

The technology used for the design of PACE3 is a deep sub-micron 0.25μm CMOS technology. This technology has been extensively studied [3] for it's robustness to radiation when combined with enclosed transistor design. PACE3 has been designed to minimise the effect of radiation.

In tests, PACE3 has been exposed to Xrays with a total dose of 14 MRad(Si). Throughout and after the exposure PACE3 remained fully functional with very small degradation of the analog performance. The gain was reduced <10% and the peaking time was increased by 5% (HG) and 4% (LG). The noise and the calibration circuit performance however remained unchanged.

The logic in PACE3 has been designed to minimise a single event effect (SEE) from disturbing the operation of the chip and making the chip lose synchronisation. Critical digital circuitry is protected by triplicated logic and majority voting. It is possible within PACE3 to count the number of single event upsets (SEU) that don't cause loss of synchronisation. If a 2 out of 3 situation occurs with a triplicated logic cell indicating an upset then a counter is incremented and the result stored in a register that can be read through an "I^2C like" command.
To test for SEUs, 2 PACE3 assemblies were exposed to a 68 MeV proton beam with a fluence of $2.352*10^{13}$ p/cm^2 over 9hrs 30mins. During this exposure 2 SEUs were seen. One SEU occurred in the triplicated logic and was counted by the upset register. The second occurred in the control logic and caused loss of synchronisation.

The impact of this result on the operation of the Preshower has been estimated as now described.

The energy that is significant in inducing an SEU is E > 20MeV. The estimated neutron fluence in the Preshower for E > 20MeV in one hour of LHC ranges from $8.6x10^9$ n/cm^2 at $\eta = 2.6$ to $1x10^9$ n/cm^2 at $\eta = 1.6$. The Preshower has 4300 PACE3 modules. For the purpose of this calculation, the Preshower is artificially divided into two regions of which 1673 PACE modules lie in the inner half and 2627 lie in the outer half. For an estimation of the number of SEUs occurring within one hour of LHC it is approximated that the inner chips are exposed to the maximum fluence and the outer chips to the minimum fluence as shown in figure 11.

The result is that the probability of an SEU causing loss of synchronisation of a single chip within the whole Preshower within one hour of LHC is between 0.38 and 1.4 (90%confidence level). A loss of synchronisation requires a RySynch pulse to return the chip to normal operation. Hence a Preshower ReSynch signal should not be needed on a more regular basis than once per hour.

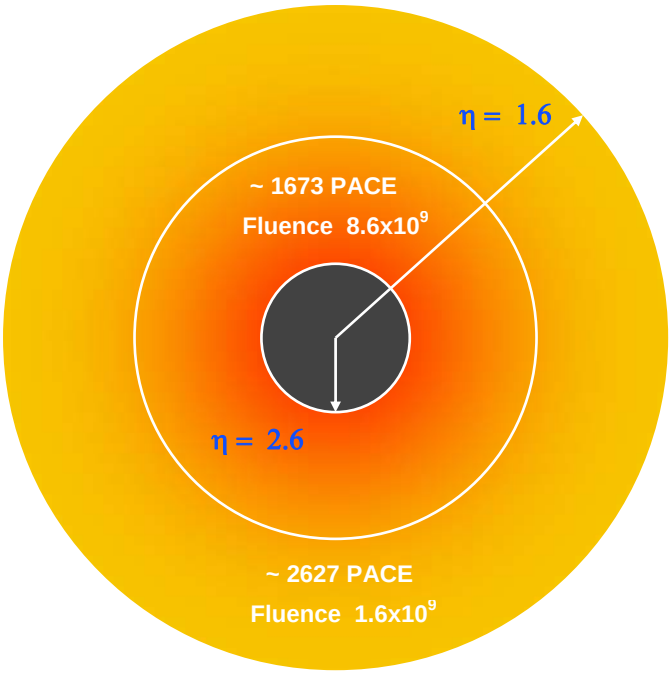

Figure 11: The number of PACE3 modules within the outer and inner ring of the Preshower and the LHC fluence (E.20MeV) as approximated at the limits of $\eta = 2.6$ and $\eta = 1.6$.

VI. Summary

A large dynamic range analog memory for the readout of silicon sensors in the LHC CMS Preshower has been designed and measured. The ASIC assembly is called PACE3 and comprises two chips DELTA3 and PACEAM3. Key features include 32 channels, large dynamic range (0.1MIP to 400 MIPs), switched gain, noise optimised for capacitive sensors, internal calibration, 192 cell deep low noise analog memory, simultaneous storage of 16 LV1As, differential multiplex analog readout, programmability through an "I^2C like" interface and radiation hard operation.

VII. References

[1] P.Aspell *Conception et mise au point de l'électronique frontale du détecteur de pied de gerbe (Preshower) de l'expérience CMS* (PhD Thesis, Université Claude Bernard - LYON - France)
[2] P.Aspell, D.Barney, P.Bloch, P.Jarron, S.Reynaud, P.Tabbers *Delta: A charge sensitive front-end amplifier with a switched gain system for low noise, large dynamic range silicon detector readout.* (Presented at the 8th Pisa Meeting on Advanced Detectors, Elba May 2000) Nuclear Instruments and Methods in Physics Research A 0 (2001) 1-7
[3] G. Anelli Conception et caractérisation de circuits intègres résistants aux radiations pour les détecteurs de particules du LHC en technologies CMOS submicroniques profonds (PhD Thesis, Insitut National Polytechnique de Grenoble - Grenoble, France