PACE3:

A large dynamic range analog memory ASIC assembly designed for the readout of silicon sensors in the LHC CMS Preshower.

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# PACE principle specifications

<table>
<thead>
<tr>
<th>Main Requirements from the CMS Preshower</th>
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<tbody>
<tr>
<td>* Sensor strip capacitance  $\sim 55pF$</td>
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<tr>
<td>* 32 channels</td>
</tr>
<tr>
<td>* DC coupled sensor to electronics (implies $&lt; 20\mu A$ leakage current per channel)</td>
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<tr>
<td>* Dynamic range  $0.1 - 400$ MIPs</td>
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<tr>
<td>* Signal to noise ratio of  10 (for calibration using single MIPs)</td>
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<tr>
<td>* Internal calibration possibility over full dynamic range</td>
</tr>
<tr>
<td>* Operate at the LHC bunch crossing frequency of 40 MHz (peaking time $\sim 25ns$)</td>
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<tr>
<td>* LV1 latency  $3.2\mu s$ programmable</td>
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<tr>
<td>* 3 samples per LV1A</td>
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<tr>
<td>* Analog memory 192 cells deep, FIFO 48 deep (16 LV1As)</td>
</tr>
<tr>
<td>* Multiplexed differential analog readout</td>
</tr>
<tr>
<td>* Programmability through I²C</td>
</tr>
<tr>
<td>* Radiation Environment:  10 Mrads(Si) of ionising radiation</td>
</tr>
<tr>
<td>2 * $10^{14}$ n cm$^{-2}$ neutron fluence</td>
</tr>
</tbody>
</table>
Assembly of two ASICs
Delta3 and PACEAM3

Technology 0.25um CMOS

Reception of ASICs
PACE3 June 03
PACE3b March 04

Designers:
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D. Moraes
M. Dupanloup
Q. Morrissey
PACE3 analog chain

**Diagram Description:**
- **Delta 3:**
  - Delta Preamp & Leakage Current Compensation
  - Shaper
  - Switched Gain
  - SF
  - Channel Output to PACEAM

- **PACEAM3:**
  - Input from Delta
  - Memory Cell
  - Read Amplifier
  - Level Shifter
  - Track & Hold
  - MUX 32:1
  - Differential Output Buffer
  - AntOut_Pos
  - ADCCM
  - AntOut_neg

**Components:**
- Delta
- Preamp
- Vshaper
- HG
- VmemRef
- Voutbuf
- Anout_neg
- Anout_pos
The Delta front-end analog channel
PACEAM analog chain

**Diagram:**
- Analog Memory
- Read Amplifier
- Inverting Level Shifter
- Track & Hold
- Analog Multiplexer
- Differential Output Amplifier

**Components:**
- Input pad
- VMemRef
- VReadRef
- VShift
- Hold
- VOutBuff
- AnOut_pos
- AnOut_neg

**Annotations:**
- Analog Memory: 32 * 196 cells
- Read Amplifier
- Inverting Level Shifter
- Track & Hold
- Analog Multiplexer
- Differential Output Amplifier

**Additional Details:**
- W1b
- W1
- W2b
- W2
- 800ps
- Wtop
- Rtop
- W2b
- W1
- Rb
- W1b
- Rb
- W2
- Cp
- Cm
- Rb
- VMemRef
- 800ps
Signal Response in HG and LG

HG
Peaking time = 27 ns
Undershoot ~ 7%

LG
Peaking time = 25 ns
Undershoot ~ 7%
PACE3 Calibration

Calibration of system with real single MIPs. Cal pulse... 1 to 50 MIPs

Overlap between the two gains to inter-calibrate.

High Precision (HP)
Range .... -31.4mV to 31.4mV, lsb = ~0.314mV
(Range .... -10 to 10 MIPs, lsb = 1/10th MIP)

Low Precision (LP)
Range .... -31.4 mV to 1.256 V, lsb = 7.8 mV
(Range .... -10 to 400 MIPs, lsb = 2.5 MIP)

Will need to measure LP and HP response periodically to calibrate the calibration circuit.

Step response from the calibration circuit

~ 400 MIPs equivalent 1.256

3.14 mV step = 1 MIP
Calibration Circuit O/P Voltage Step

Match the response of a real MIP with electronic injection pulse

0

DAC CalV input value

0

256
Internal Calibration Circuit (HP and LP)

- **VCal**: Voltage Reference
- **CalOut**: Output of Calibration Pulse
- **CalPulse**: Calibration Pulse Signal
- **CalChan<31:0>**: Calibration Channel Selection
- **Channel 30**: Connected to HP
- **Channel 31**: Connected to LP
- **1.275pF**: Capacitance
- **40pF**: Capacitance
- **20:1**: Gain Ratio
- **3.14mV = 4fC**: Calibration Voltage

The diagram illustrates the internal calibration process with connections to HP and LP channels, including voltage references and gain stages.
Calibration Circuit Response

**Injection pulse step amplitude vs DAC setting in HP and LP**

- HP: \[y = 0.0077x - 0.4261\]
- LP: \[y = 0.0003x - 0.0498\]

**CalV DAC setting**

- LP Step Amplitude (volts): -0.04 to 0.28
- HP Step Amplitude (volts): 0.04 to 0.28

**Linearity of Injection Pulse**

- HP: \[y = -2E-09x + 0.0003\]
- LP: \[y = -6E-09x + 0.0077\]

**RANGE**

<table>
<thead>
<tr>
<th>Mode</th>
<th>Range</th>
<th>Mean LSB</th>
<th>σ variation from mean (LSB)</th>
</tr>
</thead>
<tbody>
<tr>
<td>HP</td>
<td>-36.6mV to 26.1mV ( -11.6 MIPs to 8.3 MIPs)</td>
<td>0.345mV</td>
<td>2.95 µV</td>
</tr>
<tr>
<td></td>
<td></td>
<td>(~1/9th MIP)</td>
<td>(&lt; 1/1000th MIP)</td>
</tr>
<tr>
<td>LP</td>
<td>-41.1mV to 2.12V ( -13 MIPs to 675 MIPs)</td>
<td>7.68mV</td>
<td>5.81mV</td>
</tr>
<tr>
<td></td>
<td></td>
<td>(2.45 MIPs)</td>
<td>(&lt;1/500th MIP)</td>
</tr>
</tbody>
</table>

**Note:** Results measured through the DCU. 1 eq. MIPs = 4fC injected charge or 25ke
Dynamic Range **HG** in HP & LP (all 32 channels)

Gain = 20.8mV/MIP

<table>
<thead>
<tr>
<th>Range</th>
<th>Value</th>
</tr>
</thead>
<tbody>
<tr>
<td>HGHP</td>
<td>-10 to 10 MIPs</td>
</tr>
<tr>
<td>HGLP</td>
<td>0 to 50 MIPs</td>
</tr>
</tbody>
</table>
Dynamic Range **LG** in HP & LP (all 32 channels)

Gain = 3.3mV/MIP

<table>
<thead>
<tr>
<th>Range</th>
<th>-10 MIPs to 10 MIPs</th>
<th>0 to 400 MIPs</th>
</tr>
</thead>
<tbody>
<tr>
<td>LGHP</td>
<td></td>
<td></td>
</tr>
<tr>
<td>LGLP</td>
<td></td>
<td></td>
</tr>
</tbody>
</table>
Pedestal Variation (HG)

Channel to channel variation = 3.2 mV rms
Seems random from channel to channel and not affected by time slot.

Mean pedestal variation in one channel = 0.49 mV rms

Note: this chip had a gain in HG of 20.75 mV/MIP.
Pedestal Variation (LG)

Mean pedestal variation in one channel = 0.365 mV rms

Note: this chip had a gain in LG of 3.24 mV/MIP.

Channel to channel variation = 3.2 mV rms
Seems random from channel to channel and not affected by time slot.
Noise (HG)

Mean noise = 0.8622 mV rms

Note: this chip had a gain in HG of 20.75mV/MIP.

Mean Signal to ratio = 24.07 (1038e)
Calculated Noise (HG)

Calculated noise for Delta3

ENC = 470e + 41.5e/pF

Si Sensor ~ 55pF

Hence Delta3 noise predicted
~ 2400e rms or S/N = 10.4
Ionising radiation tests

Test carried out at CERN

X-rays to a total dose of ~ 14 Mrad

Preshower requirements 10 Mrad

1 PACE3 module irradiated

Pulse shape unchanged

Gain reduction < 2 %

Peaking time increase ~5% (HG), ~4% (LG)

Noise – no significant change

Calibration – no significant change

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Gain vs Dose

Peaking time vs dose
Single Event Effect Tests

Tests carried out at CRC (Louvain La Neuve)  
68 MeV proton beam

2 PACE3 modules exposed to a fluence of $2.352 \times 10^{13}$ p/cm$^2$ over 9hrs 30mins

PACE:
2 upsets seen:
1 in triplicated logic counted in upset reg.
1 in control logic causing loss of sync.
What do the SEE results mean for the Preshower?

Preshower Fluence (TDR : E > 100 KeV)
- Fluence $\eta = 2.6 > 1.8 \times 10^{14}$ n/cm²
- Fluence $\eta = 1.6 > 2 \times 10^{13}$ n/cm²

E>20 MeV important for SEE
Estimate gives factor 3 less
LHC: 7 years high lum, 100 days a year and 10 hours a day

Fluence in 1 hour of LHC (E>20MeV)
- Fluence $\eta = 2.6 > 8.6 \times 10^9$ n/cm²
- Fluence $\eta = 1.6 > 1 \times 10^9$ n/cm²

Preshower has 4300 PACE modules
~ 1673 inner ring
~ 2627 outer ring

Probability of an upset causing “loss of sync” within the Preshower in one hour of LHC is:

$\sigma_{LHC} = \frac{\text{errors}_{LHC(1hr)}}{\text{Nchips}_{LHC} \times \text{Flu}_{LHC(1hr)}}$

$\sigma_{CRC} = \frac{\text{errors}_{CRC}}{\text{Nchips}_{CRC} \times \text{Flu}_{CRC}}$

PACE Prob. (90% confidence) between 0.038 and 1.4
# Summary

A large dynamic range analog memory for the readout of silicon sensors in the LHC CMS Preshower has been designed, measured and due to go into production 1st quarter 2005.

The ASIC assembly is called “PACE3 comprising two chips; “Delta” and “PACEAM”

<table>
<thead>
<tr>
<th>Feature</th>
<th>HG</th>
<th>LG</th>
</tr>
</thead>
<tbody>
<tr>
<td>Analog memory size</td>
<td>32 channels x 192 memory cells</td>
<td></td>
</tr>
<tr>
<td>Maximum depth of stored samples</td>
<td>48 (16 LV1s with 3 samples stored per LV1)</td>
<td></td>
</tr>
<tr>
<td>Leakage current compensation for dc sensor coupling</td>
<td>&lt; 100 µA (&lt;20 µA per strip expected after 10 years LHC)</td>
<td></td>
</tr>
<tr>
<td>Two gain settings</td>
<td>HG ~ 20.8 mV / MIP</td>
<td>LG ~ 3.3 mV / MIP</td>
</tr>
<tr>
<td>Shaper peaking time</td>
<td>HG ~ 27ns</td>
<td>LG ~ 25 ns</td>
</tr>
<tr>
<td>Dynamic range</td>
<td>HG 0.1 – 50 MIPs</td>
<td>LG 1 – 400 MIPs</td>
</tr>
<tr>
<td>Analog memory pedestal variation per channel</td>
<td>HG σ = 0.49mV</td>
<td>LG σ = 0.365 mV LG.</td>
</tr>
<tr>
<td>Programmable internal calibration</td>
<td>High Precision (1/9th MIP LSB)</td>
<td>Low Precision (2.45 MIPs LSB)</td>
</tr>
<tr>
<td>Channel to channel offset</td>
<td>σ = 3.2 mV</td>
<td></td>
</tr>
<tr>
<td>Noise</td>
<td>( S/N = 24 without sensor, ~ 10 expected with sensor )</td>
<td></td>
</tr>
<tr>
<td>Operation within an ionising radiation environment</td>
<td>checked &lt; 14 MRad(Si)</td>
<td></td>
</tr>
<tr>
<td>SEE induced “loss of sync” probability in the Preshower per hour of LHC</td>
<td>0.038 to 1.4 (90% confidence level)</td>
<td></td>
</tr>
<tr>
<td>Power consumption</td>
<td>650 mW RUN MODE</td>
<td>10 mW SLEEP MODE</td>
</tr>
</tbody>
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