

The muon L0 Off Detector Electronics (ODE) for the LHCb experiment

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Abstract

The ODE board is the trigger L0 stage [1] of the muon detector trigger electronics. The board provides L0 trigger interface via 12 channels parallel optical link and DAQ interface via single optical link, using the GOL chips [2] as data serializer. A custom chip (SYNC) [3] receives and synchronizes logical channels signals [4] providing for the L0 buffers. The TTCrx chip [5] is used to receive the LHCb master clock and the control signals from TTC system. The board functionalities are controlled and monitored via an internal I²C serial bus. An ELMB board [6] provides the ECS interface. Each ODE manages 192 LVDS input channels at a constant rate of 40.08 MHz.

I. INTRODUCTION

The LHCb detector [4] will operate at the LHC collider at CERN. It is a single-arm spectrometer (Figure 1) designed to reconstruct B-decay vertex with a good resolution and to provide identification for charged particles.

A high performance trigger based on large transverse momentum particle and displaced secondary vertices will allow efficient B-meson events selection.

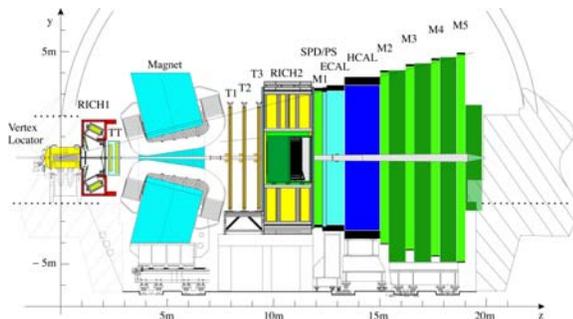


Figure 1 : The LHCb detector (top view)

The muon sub-detector must provide the trigger functionality [4][7] to detect muon tracks with large transverse momentum (flavour-tagging and B-meson decays final states).

The muon trigger architecture relays on 1248 *Trigger Sectors* (TS) built by the first stages of the electronic chain.

About 120,000 *physical channels* are firstly merged both in the chambers front-end and in the *Intermediate Board* (IB) system [8], to generate $\sim 26,000$ *logical channels*. Then in the *Off Detector Electronics* (ODE) boards the logical channels are synchronized to the bunch crossing, arranged to implement the required *trigger sectors* and, finally, sent to the L0 trigger logic through 1248 optical links at 1.6 Gbit/s.

The ODE board provides also a measure of the signal arrival time with a 1.5 ns time resolution and implements the L0-pipelines, the DAQ interface (via a 1.6 Gbit/s optical link) and the ECS interface.

To ensure the correct operation of the muon trigger the ODE-trigger optical links must have BER less than 10^{-12} .

Then the board layout must guarantee a good signal integrity minimizing the contribution of the main sources of noise (signal reflection, crosstalk and the power/ground noise). The EMC/EMI issues should be also considered as they could generate signal distortion.

Finally, as the system must operate near the detector in a hostile environment, radiation tolerant components must be used and control logic must be implemented using a triple modular redundancy technique to increase SEU immunity.

II. BOARD OVERVIEW

The board (Figure 2) receives up to 192 digital logical channels (LVDS standard) from the muon chamber front-end electronics [9] or from the IB System [8] at 40.08 MHz rate.

Incoming signals are synchronized with the master LHCb clock and sent to the L0 muon trigger system [7]. The arrival time respect to the master clock phase is measured and data are stored in the L0 pipeline waiting for L0 trigger decision.

For each valid L0 trigger (*L0_yes* signal), data are processed, formatted and sent to L1 DAQ electronics by a board controller (*L0_CONTROLLER*). The right board alignment is checked for each valid L0 trigger and error conditions are reported to the ECS via an error register.

Several test functionalities have been implemented for debug, monitor and control purposes.

The TTCrx chip receives the LHCb master clock, the L0 trigger information and the TTC system broadcast commands. A jitter filtering circuit acts on the recovered clock to match the GOL serializer jitter specification.

All chips on the board are managed via I2C interface. An ELMB board provides the control for the internal I2C bus and for the communication to the ECS via a CAN interface.

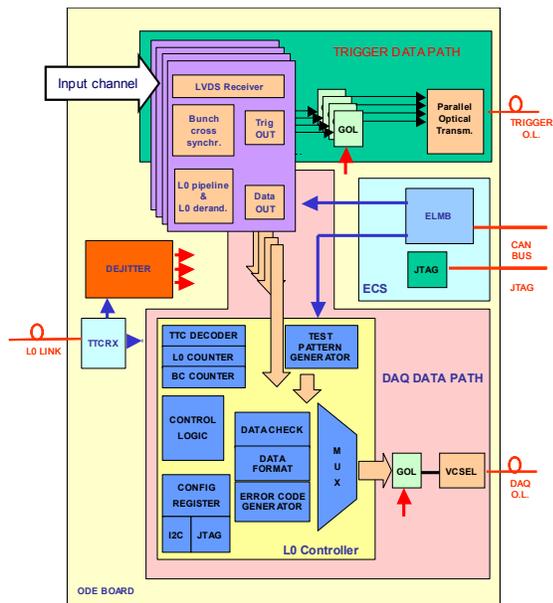


Figure 2 : ODE board block diagram

III. SYNC

Both synchronization stage and L0 pipelines are implemented in the SYNC custom chip where:

- A. input data are synchronized to the bunch crossing clock, tagged with a bunch identifier number (BX_cnt) and arranged for the trigger system on output pins;
- B. a 4-bit TDC, with a resolution of 1.5 ns, measures the arrival time of each input signal in the master clock period and data are put in L0 buffer until a L0 trigger decision occurs;
- C. for each $L0_yes$ signal, data are extracted from the L0_buffer, tagged with event identifier number (EV_cnt) and stored in the L0 de-randomizer where they can be read by the L0_CONTROLLER.

Each SYNC chip receives 8 input signals and 2, 3 or 4 chips are required to generate one *Trigger Sector* (TS) [10]. To fit all TS configurations, minimizing the number of different ODE boards, the SYNC chips are mounted on three types of Piggy Board (PB) where trigger data are merged to produce the TS. A single ODE motherboard,

with 12 PB slots, can host different types of piggy boards allowing all possible configurations.

IV. CLOCK DISTRIBUTION AND TTCRX SIGNALS

All the main sub-circuits (L0_CONTROLLER, SYNCs, GOLs) of the ODE board must work as a synchronous machine driven by the bunch-crossing clock (40.08 MHz) and fully aligned with other data of the experiment.

The board receives the master clock together with control and synchronization information, delivered by TTC system, via an optical link and the TTCrx chip.

The jitter of the clock recovered from TTCrx is higher than 240 ps (peak to peak) and exceeds the GOL chip specification (100 ps). Therefore a de-jitter circuit is mandatory to guarantee a data transmission with the required very low bit error rate (10^{-12}).

A narrow bandwidth PLL has been implemented using the QPLL chip [11]. Such circuit generates a clock signal, phase-locked to the system clock input, with a residual jitter less than 50 ps (peak to peak).

The de-jittered clock is distributed to the GOLs, to the SYNCs and to the board controller FPGA via a low jitter tree architecture. PECL circuits with about 1 ps jitter specifications are used to minimize the contribution to the overall jitter. The clock distribution scheme is shown in Figure 3.

The PLL output is split via a 1-to-10 differential clock driver (MC100LVEP111) and routed on the board. Another 1-to-5-clock driver is used to split locally the clock and to drive two GOL chips and two SYNC piggy board slots. On the piggy board, the received clock is used to drive 2 SYNC chips.

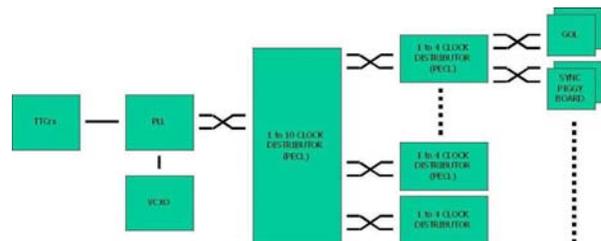


Figure 3 : block diagram of the ODE board clock distribution

The $L0_yes$ signal received by TTCrx is distributed to all the SYNC chips by the L0_CONTROLLER. This distribution scheme allows to put a veto on the $L0_yes$ or to generate a “software” $L0_valid_trigger$ via ECS.

The TTCrx broadcast commands are received and decoded by the L0_CONTROLLER too. TTC commands ($Bunch_ID_reset$, $L0_event_ID_reset$ and $L0_front-end_reset$) are delivered as synchronous signals to all other

chips on the board. They can also be generated via ECS for test purposes.

V. TRIGGER DATA FLOW

The ODE trigger interface allows a unidirectional data transfer to the muon trigger system at 40.08 MHz rate.

All input logical channels belonging to the same TS must be merged in a single data frame, tagged with the right bunch crossing identifier and sent to the muon trigger processing board every ~ 25 ns.

Each SYNC chip receives up to 8 logical channels and assigns the correct bunch identifier. Several Trigger Sector topologies are defined in different detector zones as shown in Table 1.

The number of logical channels per Trigger Sector changes is different for each detector region/station and each TS can require 2, 3 or 4 SYNC chips, with 5, 7 or 8 active channels.

Table 1 : ODE configurations versus trigger sector type

Station	Region	Logical chs per TS	SYNC per TS (PB)	PB type	Active Chs per SYNC	TS per ODE	Active ODE chs
M1	R1 R2 R3 R4	24	3	2	8	8	192
M2 or M3	R1 R2 R3 R4	28 16 28 28	4 2 4 4	1 3 1 1	7 8 7 7	6 12 6 6	168 192 168 168
M4 or M5	R1 R2 R3 R4	24 14 10 10	3 2 2 2	2 3 3 3	8 7 5 5	8 12 12 12	192 168 120 120

12 Piggy Board slots and the GOL serializers are localized on the motherboard.. Piggy Boards have different slot size and accommodate 2, 3 or 4 SYNC chips, respectively PB type 3, PB type 2 and PB type 1.

The possible ODE configurations for different detector zones are shown in Table 1. In some stations/regions only 6 or 8 of 12 possible Trigger Sectors are used and only 120 or 168 of 192 possible input signals are active but this architecture simplifies the system maintenance.

Trigger Sector data are formatted on the Piggy Board in a 32-bit data word (Table 2). The frame contains up to 28 bits of active SYNC channel hits, the two LSB of the bunch identifier and two switch bits.

The switch bits, placed in position b0 and b16, distinguish MSB from LSB part and are used for trigger data alignment. The bunch identifier bits are placed in position b1 and b17 while the others positions are for data hits.

Table 2 : Trigger Sector data word format

	b ₃₁	b ₁₇	b ₁₆		b ₁	b ₀
1 st word	14 hit data	0	1	14 hit data	0	0
2 nd word	14 hit data	0	1	14 hit data	1	0
3 rd word	14 hit data	1	1	14 hit data	0	0
4 th word	14 hit data	1	1	14 hit data	1	0

Trigger Sector data words are serialized via the GOL chips using Fast Ethernet (mode 8B/10B) and transmitted using a 12 channel parallel optical link HFBR772B (one channel per TS). Also in this case for some station/ region not all 12 links are used.

Control signals (*tx_en*, *tx_er*, *reset_b*) of each GOL are driven by a “master” SYNC on the correspondent Piggy Board.

VI. DAQ DATA FLOW

The LVDS input signals are received by SYNC where an internal 4-bit TDC, with a resolution of 1.5 ns, measures the signal arrival time within the master clock period.

TDC data and bunch counter identifier are stored in the L0 buffer. After a *L0-yes* signal, data are extracted and put in the L0 de-randomizer together with event identifier number and error flags. A simplified block diagram of SYNC is shown in Fig. 4.

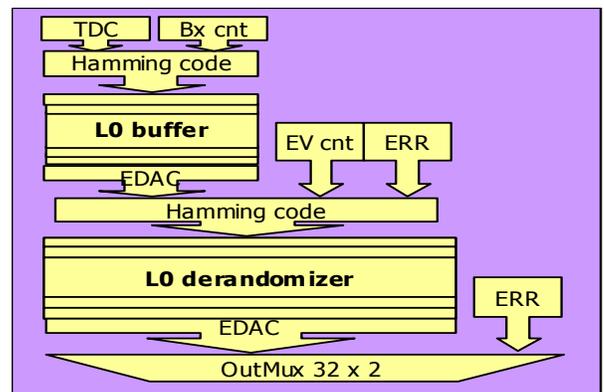


Fig 4 : Simplified SYNC block diagram

Each SYNC produces 2 words of 32 bits, one containing the TDC data (*dataword*) and the other (*infoword*) containing the *bunch_counter_identifier*, the *event_counter_identifier* and the error flags. These two words are multiplexed on a 32 bit wide output data bus. Therefore two accesses are required to fully read the complete SYNC information.

24 SYNC chips can be hosted in the ODE board and each SYNC read-access requires 25 ns. Because the readout of all SYNCs ($24 \times 25\text{ns} \times 2 = 1200 \text{ ns}$) exceeds the maximum L0 readout time (900 ns per event) a parallel readout mode has been implemented using two external

data-bus ($DATA_UP$, $DATA_DW$). Each data bus can manage up to 12 SYNCs.

The $L0_CONTROLLER$ reads, at the same time, a *dataword* from one SYNC on $DATA_UP$ ($DATA_DW$) bus and an *infoword* from another SYNC on $DATA_DW$ ($DATA_UP$) bus. The *Dataword* is used to produce the DAQ data frame while the *infoword* is used to verify board alignment and to generate a footer frame (see $L0_CONTROLLER$ section for more details).

The DAQ data frame is serialized via a GOL chip driving a VCSEL laser diode using Fast Ethernet.

VII. $L0_CONTROLLER$

The $L0_CONTROLLER$ provides data processing, DAQ interface, TTC command decoding and test functionalities. It is implemented in an anti-fuse FPGA using triple redundancy technique to increase SEU immunity.

It manages broadcast cycle from the TTCrx chip and distributes common $L0$ signals (*Bunch_counter_reset*, *Event_counter_reset*, *L0_reset*, *L0_yes*). These signals can also be vetoed or externally generated by ECS and they are distributed as synchronous signals to all other chips on the board.

$L0_CONTROLLER$ has internal 12-bits bunch counter (*BC_counter*) and 12-bits event counter (*L0_counter*). For each valid $L0$ trigger, the right alignment of all *BC_counter* (TTCrx, $L0_CONTROLLER$ and SYNC chips) and *EV_counter* ($L0_CONTROLLER$ and SYNC chips) of the board is checked. Error flags are set in an error register accessible via ECS and error words are included in the DAQ data frame.

For each $L0$ valid trigger, the $L0_CONTROLLER$ must sequentially read and process data of all SYNC de-randomizers. As the operation requires more than 25 ns, to allow consecutive $L0$ triggers an internal 16 words deep queue FIFO (*Header_FIFO*) has been implemented. A word containing *BC_counter*, *L0_counter* and one bit of TTCrx alignment check is stored in the FIFO for each *L0_yes*. *Header_FIFO* data are protected against SEU by single error correction and double error detection Hamming code.

For each word in the *Header_FIFO* a data frame (see figure 6) is produced with SYNC data. It is composed by:

- 1 header word with *BC_counter*, *EV_counter* and check bit protected with double error detection single error correction Hamming code
- 24 words with SYNC TDC data
- 5 footer words containing alignment and data check bit, geographical address board information and checksum

The frame is serialized by the GOL chip driven by $L0_CONTROLLER$ and at least one IDLE character precedes the data frame for link synchronization purpose.

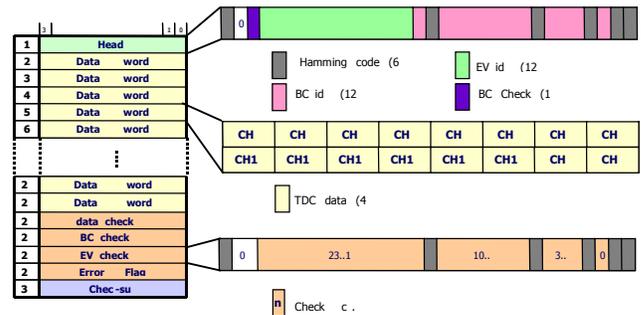


Figure 6 : DAQ data frame

Some test facilities are available for the board debug.

The main $L0$ control signals (*L0_yes*, *BC_res*, *EV_res* and *L0_res*) can be emulated via ECS.

Internal registers are used to monitor error conditions as TTCrx and GOL fault, header FIFO full and SYNC errors.

Optical link tests can be performed using pseudo-random bit generator and data frames can be stored in an internal dump FIFO accessible via ECS.

VIII. BOARD PROTOTYPES

Two prototypes of the ODE board have been developed. In the first one a custom narrow bandwidth PLL [12] has been implemented using a commercial low jitter clock generator (MAX 3670) with an external high-Q voltage-controlled crystal oscillator (VCXO). Such circuit generates a clock signal, phase-locked to the system clock input, with a residual jitter less than 40 ps, while the second prototype (Figure 7) uses the QPLL [11] chip.

As a very low BER was required for a correct trigger operation, a BER estimation has been carried out using a serial data analyzer and transmitting pseudo-random bit pattern.

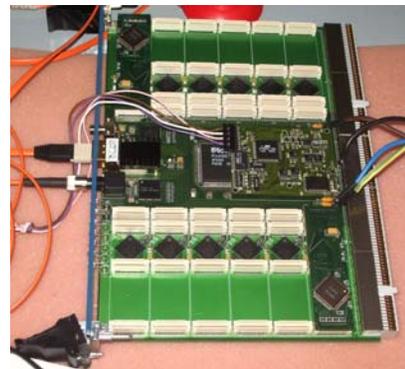


Figure 7 : ODE board prototype

Figure 8 shows the measurement for the prototype hosting the QPLL circuit. The ~ 70 ps peak to peak clock measured jitter (6 ps rms) confirms the achievement of the design goals.



Figure 8 : Jitter measurement

The eye diagram plot and the bathtub curve (Figure 9 and Figure 10) for the trigger optical link allows to infer a BER of about 10^{-16} with a 60% open eye, well below the system requirements.

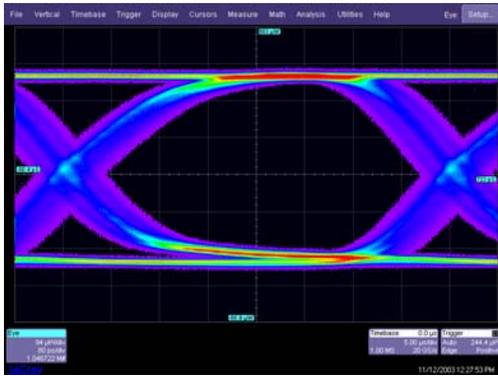


Figure 9 : Trigger link eye diagram



Figure 10 : Trigger link bathtub curve

IX. CONCLUSIONS

The architecture of the ODE board, the L0 stage of the muon front-end electronics has been presented.

The board manages up to 192 LVDS input channels and includes twelve 1.6 Gbit/s parallel optical drivers for trigger data transfer and one 1.6 Gbit/s optical driver for DAQ data transfer.

Because the BER system requirements (less than 10^{-12}) the board design was very challenging, as it requires an accurate control of timing signal jitter.

Moreover all components used should be radiation tolerant and control logic should include error detection and correction capability.

Preliminary tests carried out with a 20 GHz LeCroy serial data analyzer show the system jitter is below 7 ps rms; the measured jitter value allows inferring a BER value less than 10^{-16} .

Work is in progress to implement an effective BER measurement by comparison of the transmitted and received data.

X. REFERENCES

- [1] A. Lai et al., *Muon detector front-end architecture*, LHCb note, LHCb-2000-017
- [2] GOL reference manual – P. Moreira et al. - Version 1.4- May 2002- http://projgol.web.cern.ch/projgol/gol_manual.pdf
- [3] A. Lai et al., *The SYNC chip in the Off-Detector Electronics of the LHCb muon system*, LHCb-2001-063
- [4] LHCb Collaboration, *LHCb: Technical Proposal*, CERN LHCC-98-004
- [5] J. Christiansen et al., *TTCTx reference manual*, CERN-EP/MIC
- [6] B. Hallgren et al., *The Embedded Local Monitor Board (ELMB) in the LHC Front-end I/O Control System*, "7th Workshop on Electronics for LHC Experiments", Stockholm, Sweden
- [7] E. Aslanides et al., *A synchronous architecture for the L0 muon trigger*, LHCb note, LHCb-2001-010
- [8] A. Balla et al., *Muon Off-Detector electronics: The IB system*, LHCb 2003-023 MUON
- [9] Cadeddu S. et al., *DIALOG: a chip for the muon detector front-end and logic*, LHCb-2001-062
- [10] E. Aslanides et al., *Map of the trigger sectors for the muon detector*, LHCb-2003-161
- [11] QPLL Manual – P. Moreira. CERN – EP/MIC - 2004-01-26
- [12] E. Aslanides et al., *High speed ribbon optical link for the level 0 muon trigger*, LHCb-2003-00