The muon L0 Off Detector Electronics (ODE) for the LHCb experiment

A. Balla, M. Beretta, M. Carletti, P. Ciambrone, G. Corradi, G. Felici

INFN
Laboratori Nazionali di Frascati - Via E. Fermi 40, 00044 Frascati (Rome), Italy
giulietto.felici@lnf.infn.it

M. Gatta

INFN
Roma2 - Via della Ricerca Scientifica 1, 00133 Rome, Italy
Outline

- Apparatus main features
- The muon system detectors
- Readout system block diagram
- The muon trigger FEE requirements
- The muon off detector electronics
- ODE
  - Overview
  - Numbers
  - Trigger data path
  - Piggy Boards
  - DAQ data path
  - DAQ data frame
  - LO controller
  - ODE ECS
- Clock distribution chain
- Jitter measurements
- BER estimation
- Radiation environment
- Conclusions
Apparatus main features

- reconstruct B-decay vertex with a good resolution
- provide identification for charged particles

Muon detector
Station 1

Muon detector
Stations 2–5
**The muon system detectors**

**MWPC**

- Number of MWPC: 1368
- Readout: wires, pads, wires + pads
- Four gap chambers in Stations M2-M5. Two gap in M1 (R2-R4).
- Gas gap: 5 mm
- Wire: Gold-plated Tungsten, 30 mm dia.
- Wire spacing: 2 mm
- Wire length: 250 to 310 mm
- Gas mixture: Ar/CO2/CF4 (40:50:10)
- Gas gain: $G \approx 10^5$
- Charge/mip: $\approx 0.8 \text{ pC} @ \text{HV} \approx 2.7 \text{ kV}$
- Gap efficiency: $\geq 95\%$ in 20 ns window ($\sigma_t \approx 3.9 \text{ ns}$)
- Rate/channel: max 2 MHz in M1, < 0.6 MHz M2-M5
LHCb Muon Detector Granularity

- Number of FEE Channels: 126832
- Number of Logical Channels (FE Boards): 19584
- Number of Logical Channels (IB Boards): 8640
- Total Number of Logical Channels: 28224
- Number of Trigger Sectors: 1248
The muon trigger FEE requirements

Muon Trigger FE Main Tasks

- Provide information for the LO Muon Trigger

  - Muon tracks identification
  - \( P_\tau \) measurement

- Merging (some of) the FEE channels to generate the logical ones
- Align them in time, minimizing inefficiencies due to time misalignment
  - Bunch crossing alignment (BX identifier, 25 ns step)
  - Fine time alignment (single channel \( t_0 \), 1.5 ns step)
- Deliver the logical channels together with the BX identifier to the trigger logic

- Moreover the system must:
  - Include an interface to the DAQ
  - Include monitor and diagnostic facilities of circuitry and detector functionalities
The muon off detector electronics

Physical chs (1/2 chamber) → 48x2
FE board LVDS outputs (1/2 chamber) → 48

IB system

Logical H chs (1 TS) → 4
Logical V chs (1 TS) → 24

Trigger & DAQ

ODE system

10th Workshop on electronics for LHC and future experiments
ODE overview

- Logical channels
- Bx alignment
- LO buffer
- LO derandomizer

Send data to trigger via 12 parallel optical link @ 1.6Gbit/s

Format and send data to common L1 board via optical link @ 1.6Gbit/s

Test facilities for control and debug

Clock de-jitter and distribution

ECS interface
ODE numbers

- 192 LVDS input signals
  - 10 layers motherboard
  - 6U Compact PCI card
  - Mixed 5/3.3/2.5 V devices
- 1 TTCrx chip mounted on motherboard
- 1 de-jitter circuit
  - QPLL
- 24 SYNC chips
  - Mounted on piggy board
- 12 GOL chips for trigger
- 1 parallel optical transmitter (12 channels)
- 1 Board controller FPGA
- 1 GOL chip for DAQ
- 1 VCSEL laser
- 1 ELMB board for ECS interface
ODE trigger data path

- Unidirectional data transfer to trigger system
- Each SYNC every machine cycle (40.08 MHz)
  - Receives and synchronizes 8 input signals
  - Assign correct Bunch Crossing identifier (BX_Id)
  - 10 bit data out (8 hits + 2 LSB of BC_Id)
- 2, 3 or 4 SYNCs per trigger sector (TS)
- 1 GOL per TS
  - Transmission (tx_en, tx_er) driven by one “master” SYNC
  - Fast Ethernet mode (8B/10B)
- 12 GOLs drive a parallel optical link
  - HFBR772B - 1.6 Gbit/s x 12 link
- Test link facilities
  - Link check integrity
  - BER test

<table>
<thead>
<tr>
<th>BX_Id</th>
<th>1stword</th>
<th>2ndword</th>
<th>3rdword</th>
<th>4thword</th>
</tr>
</thead>
<tbody>
<tr>
<td></td>
<td>14 HIT DATA</td>
<td>0</td>
<td>1</td>
<td>14 HIT DATA</td>
</tr>
<tr>
<td></td>
<td>14 HIT DATA</td>
<td>0</td>
<td>1</td>
<td>14 HIT DATA</td>
</tr>
<tr>
<td></td>
<td>14 HIT DATA</td>
<td>0</td>
<td>1</td>
<td>14 HIT DATA</td>
</tr>
<tr>
<td></td>
<td>14 HIT DATA</td>
<td>0</td>
<td>1</td>
<td>14 HIT DATA</td>
</tr>
</tbody>
</table>

10th Workshop on electronics for LHC and future experiments
### ODE Piggy Boards

**Trigger sector type vs ODE configuration**

<table>
<thead>
<tr>
<th>Station</th>
<th>Region</th>
<th>Logical Channel per TS</th>
<th>SYNC per TS</th>
<th>TS per ODE (GOL)</th>
<th>Active ODE Channels</th>
</tr>
</thead>
<tbody>
<tr>
<td>M1</td>
<td>R1</td>
<td>24</td>
<td>3</td>
<td>8</td>
<td>192</td>
</tr>
<tr>
<td></td>
<td>R2</td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td></td>
<td>R3</td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td></td>
<td>R4</td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>M2 or M3</td>
<td>R1</td>
<td>28</td>
<td>4</td>
<td>6</td>
<td>168</td>
</tr>
<tr>
<td></td>
<td>R2</td>
<td>16</td>
<td>2</td>
<td>12</td>
<td>192</td>
</tr>
<tr>
<td></td>
<td>R3</td>
<td>28</td>
<td>4</td>
<td>6</td>
<td>168</td>
</tr>
<tr>
<td></td>
<td>R4</td>
<td>28</td>
<td>4</td>
<td>6</td>
<td>168</td>
</tr>
<tr>
<td>M4 or M5</td>
<td>R1</td>
<td>24</td>
<td>3</td>
<td>8</td>
<td>192</td>
</tr>
<tr>
<td></td>
<td>R2</td>
<td>14</td>
<td>2</td>
<td>12</td>
<td>168</td>
</tr>
<tr>
<td></td>
<td>R3</td>
<td>10</td>
<td>2</td>
<td>12</td>
<td>120</td>
</tr>
<tr>
<td></td>
<td>R4</td>
<td>10</td>
<td>2</td>
<td>12</td>
<td>120</td>
</tr>
</tbody>
</table>

- Minimize number of PCB layouts
- Unique motherboard for all TS
  - 12 piggy board slots
  - 6 / 8 / 12 GOL (active optical link) per ODE
- 3 different piggy boards
  - 24 SYNC per ODE (2 / 3 / 4 SYNC per piggy board)
  - 120 / 168 / 192 active input signals
ODE DAQ data path

- Unidirectional data transfer to L1 DAQ

- SYNC
  - Measure input signal phase vs LHCb clock period
  - Put data in L0 buffer (40.08 MHz)
  - Put data in L0 derandomizer after L0 trigger (1 MHz)

- SYNC data format
  - 32 bit for TDC data (data word)
  - 32 bit for BX_Id, EV_Id, data error (info word)
  - 32 bit output data bus
  - 24 SYNC X 2 access X 25 ns = 1200 ns > 900 ns

- Parallel SYNC readout mode
  - 2 x 32 bit wide buses (BUS_UP, BUS_DW)
  - 12 Sync for each bus

- LO controller
  - Read data/info words from SYNC de-randomizers
  - Create L1 DAQ data frame
  - Drive GOL (tx_en, tx_er)
    - Ethernet mode
    - VCSEL diode
- Data frame is preceded by an idle character
- Data frame is 30 words long
**LO controller**

- Receive and decode TTCrx data
- Control SYNC readout
- Format data for L1 DAQ
- Check data synchronization
- Drive GOL transmission

**Test facilities**
- Known pattern and PRBG for link integrity test
- Internal data frame dump fifo
- TTC control signal internal emulation
- Error condition monitor

**I²C interface**

**Anti-fuse technology FPGA (ACTEL AX500)**
ODE ECS

- ECS interface via ELMB card
  - CANbus interface

- ELMB internal connection
  - 2 I2C buses
    - 24 SYNC
    - 13 GOL, TTCrx, LO controller
  - 1 bus JTAG

- Initialization time

<table>
<thead>
<tr>
<th>Device</th>
<th>Byte Device</th>
<th>I2C Byte Device</th>
<th>Device ODE</th>
<th>Total Byte</th>
</tr>
</thead>
<tbody>
<tr>
<td>L0 CONTROLLER</td>
<td>3</td>
<td>9</td>
<td>1</td>
<td>9</td>
</tr>
<tr>
<td>TTCrx</td>
<td>7</td>
<td>28</td>
<td>1</td>
<td>28</td>
</tr>
<tr>
<td>GOL</td>
<td>4</td>
<td>16</td>
<td>13</td>
<td>208</td>
</tr>
<tr>
<td>SYNC</td>
<td>6</td>
<td>18</td>
<td>24</td>
<td>432</td>
</tr>
</tbody>
</table>

| Total Byte | 677         |
| Init Time  | 60 ms       |
Clock distribution

- Receive LHCb clock (40.08 MHz)
  - Completely synchronous system
- TTCrx recovered clock jitter filter
  - TTCrx jitter > 240 ps peak to peak (30 ps RMS)
  - Maximum allowed GOL jitter 100 ps peak to peak
- Narrow bandwidth PLL
  - QPLL
- Low jitter clock distribution
  - PECL standard (RMS jitter specs < 1 ps)
  - GOL, SYNC and Board Controller FPGA
Jitter measurements – eye diagram

Trigger link

0.7 UI

DAQ link

0.7 UI

QPLL clock jitter
6.02 ps rms
BER estimation

- Trigger
-16 DECADE

- DAQ
-16 DECADE

10th Workshop on electronics for LHC and future experiments
Radiation environment

- Data from LHCb electronics website (simulation safety factor of 2)

- **LO controller FPGA**
  - State machines implemented with triple modular redundancy (TMR) technique
  - Triple voted and auto-corrected registers
  - Anti-fuse technology (Actel AX500)

- **Qualified**
  - GOL (CERN)
  - TTCrx (CERN)
  - ELMB (ATLAS test)
  - QPLL (CERN)

- **Tested**
  - VCSEL Honeywell HFE439X-541 (CMS HCAL + Honeywell)
  - MC100LVEP111 (CMS)
  - Parallel Optical link HFBR772B (Marseille)

- **To be tested**
  - SYNC (Rad-Tol technology)
  - MC100EPT20, MC100EPT26, MC100LVEP1
  - Actel FPGA

**Table: Dose to L0 controller FPGA**

<table>
<thead>
<tr>
<th>Total dose (rad) (10 years)</th>
<th>1 MeV Neutron eq. (10 years)</th>
<th>Hadrons &gt; 20 MeV (10 years)</th>
</tr>
</thead>
<tbody>
<tr>
<td>$7.9 \times 10^3$</td>
<td>$9.8 \times 10^{11}$</td>
<td>$5.0 \times 10^{10}$</td>
</tr>
</tbody>
</table>

10th Workshop on electronics for LHC and future experiments
Conclusions

- The Off Detector Electronics (ODE board) of the LHCb muon system has been presented.

- The ODE board receives the logical channels and generates the Trigger Sectors
  - Three types of piggyback boards and a single ODE motherboard are used to fit every trigger sectors topologies

- The ODE board main features are:
  - 192 inputs (LVDS standard)
  - A parallel optical link with an overall bandwidth of ~ 20 Gbits/s as interface to the trigger system
  - Circuitry for L0 functionality
  - A 1.6 Gbit/s optical link as interface to L1 DAQ.

- A BER of about $10^{-16}$ can be inferred from preliminary measurements