# *Advanced PWB Substrates Enabling Technologies*

By

Tom Buck

***Dynamic Details Inc.***

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# Dynamic Details, Inc.

Enabling Technologies

## Overview

- Technology Drivers
- Advanced Materials
- Characterized FR-4
- Hybrid Constructions
- Laser Direct Imaging
- High Aspect Ratio Copper Plating
- Laser Drilling
- Planar Via Technologies

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# Advanced Printed Circuit Technologies



Chip scale packaging and ever increasing signal speeds are testing the limits of conventional PWB fabrication technologies. Bridging the gap to push forward will require an array of of enabling technologies !

- Enabling technologies for advanced PWB's
  - Advanced low loss laminate systems
    - Mixed dielectric structures
  - Laser Direct Imaging (LDI)
  - High aspect ratio Cu plating (Pulse Plating)
  - Laser drilling
    - Planar Cu filled Microvia's
    - Stacked Microvia's
  - Advanced PWB structures

Enabling Technologies

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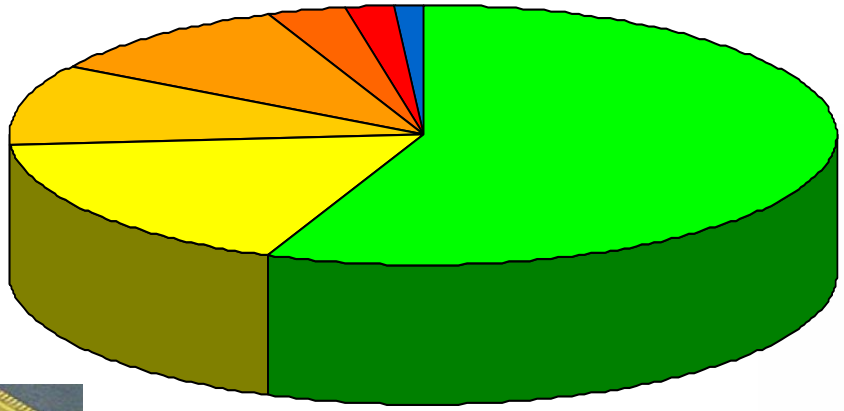
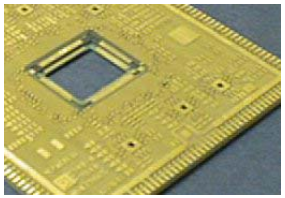
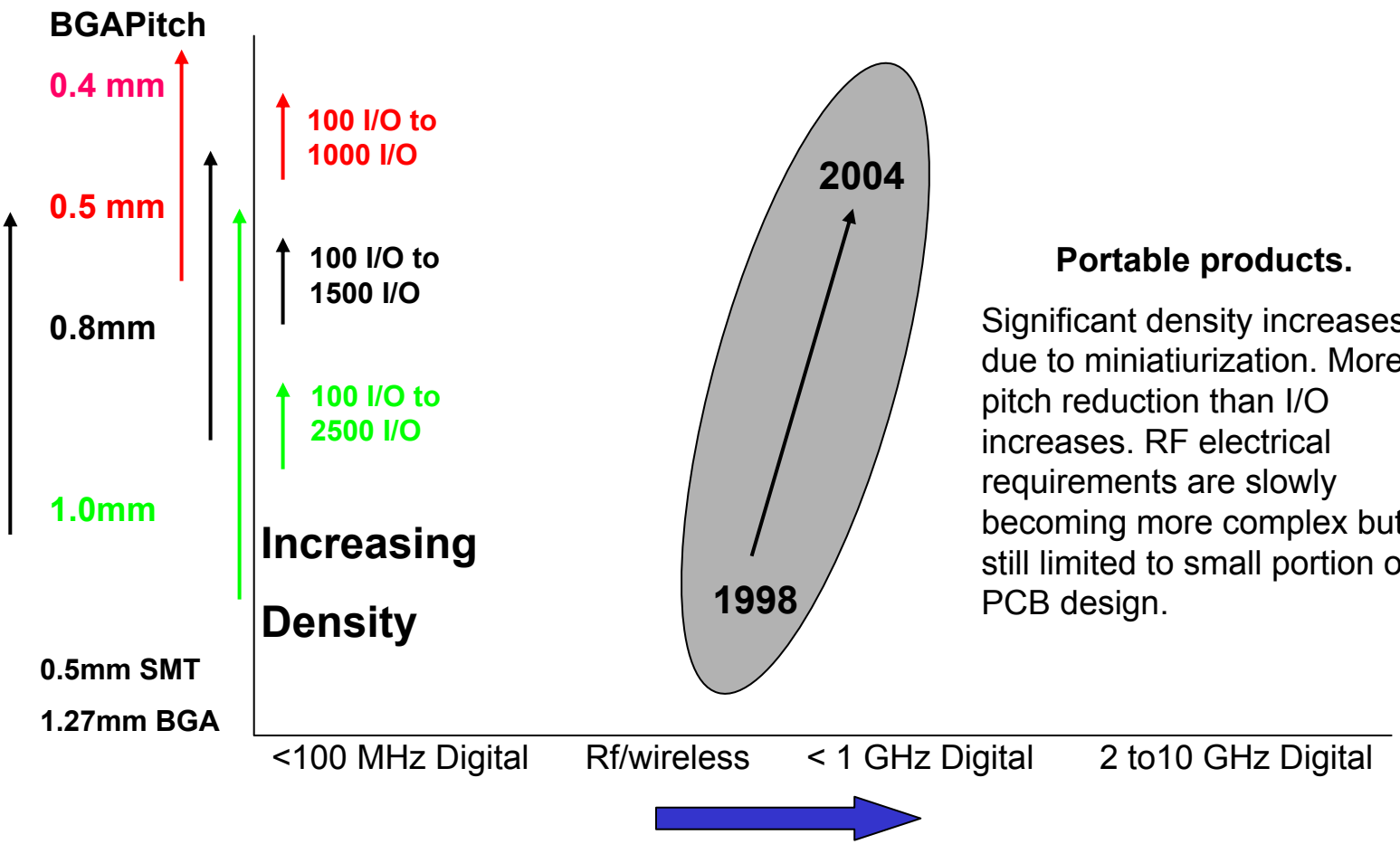
## High Density Interconnect Markets



# Trends in electrical performance and density






**Portable products.**

Significant density increases due to miniatiurization. More pitch reduction than I/O increases. RF electrical requirements are slowly becoming more complex but still limited to small portion of PCB design.

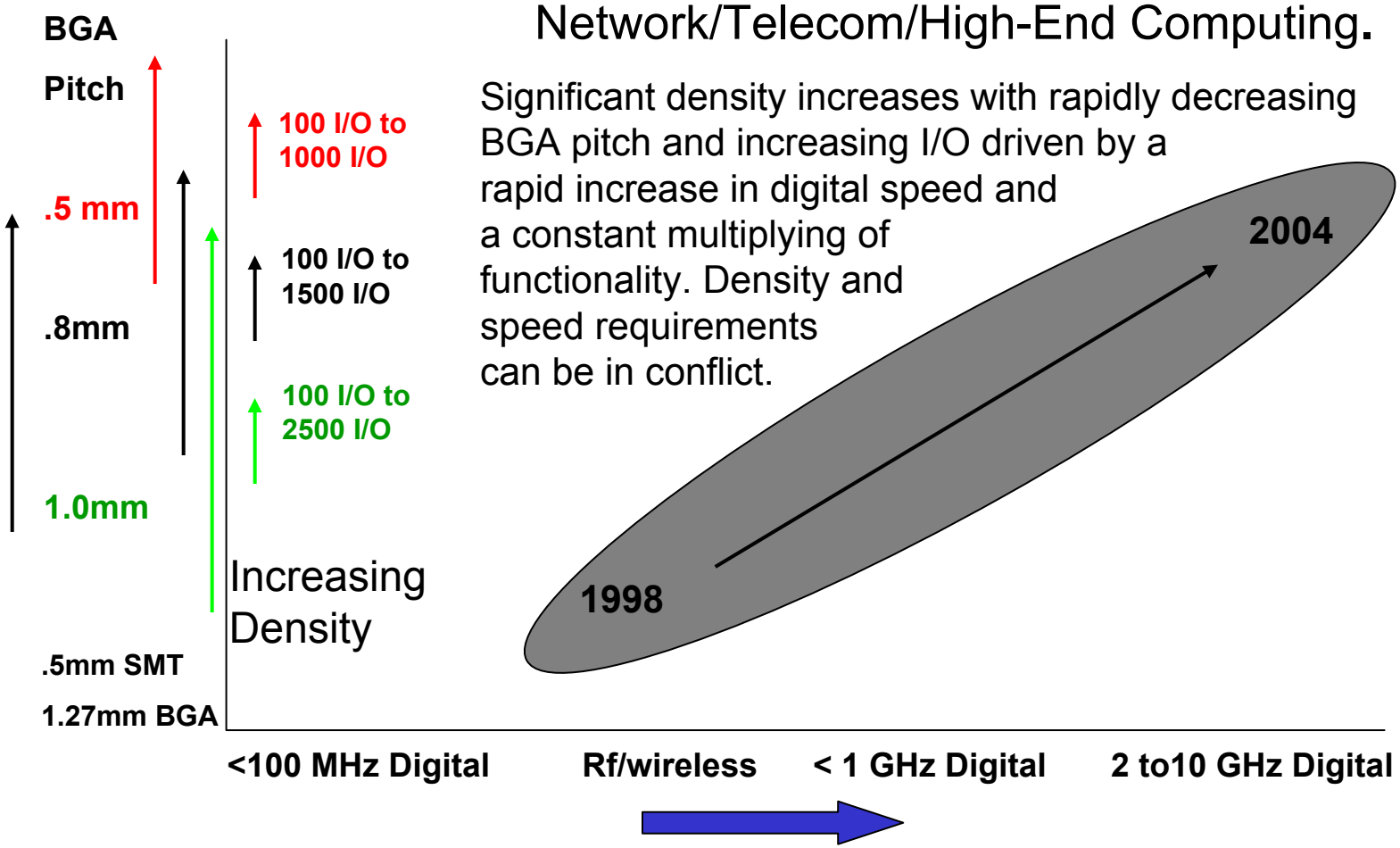
Increasing electrical performance requirements.

# Trends in electrical performance and density



## Network/Telecom/High-End Computing.

Significant density increases with rapidly decreasing BGA pitch and increasing I/O driven by a rapid increase in digital speed and a constant multiplying of functionality. Density and speed requirements can be in conflict.




Increasing electrical performance requirements.

# Electrical Considerations: High Density PWB's

Enabling Technologies.

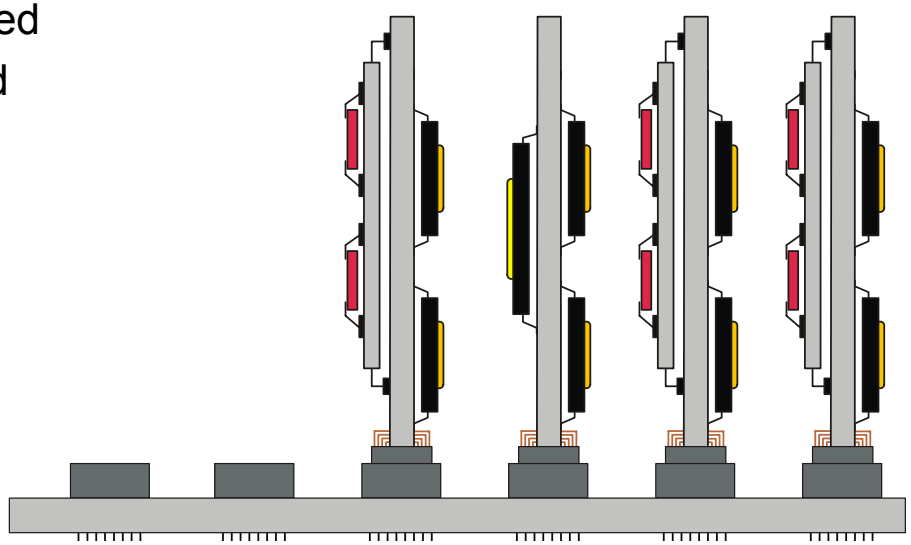
## Performance Driven Board Design

- Controlled impedance required
- Differential signaling required
  - Edge Coupled Lined
  - Broad Side Coupled
- Solid "AC Return Path"
- Low Attenuation
  - Low loss dielectric
  - Mixed dielectrics
- Higher layer counts required
  - Board thickness ?

## High Density Connectors

- Controlled Impedance
- Differential Signaling
- Minimize Crosstalk
- High Signal to Ground Ratio

## Design Challenge

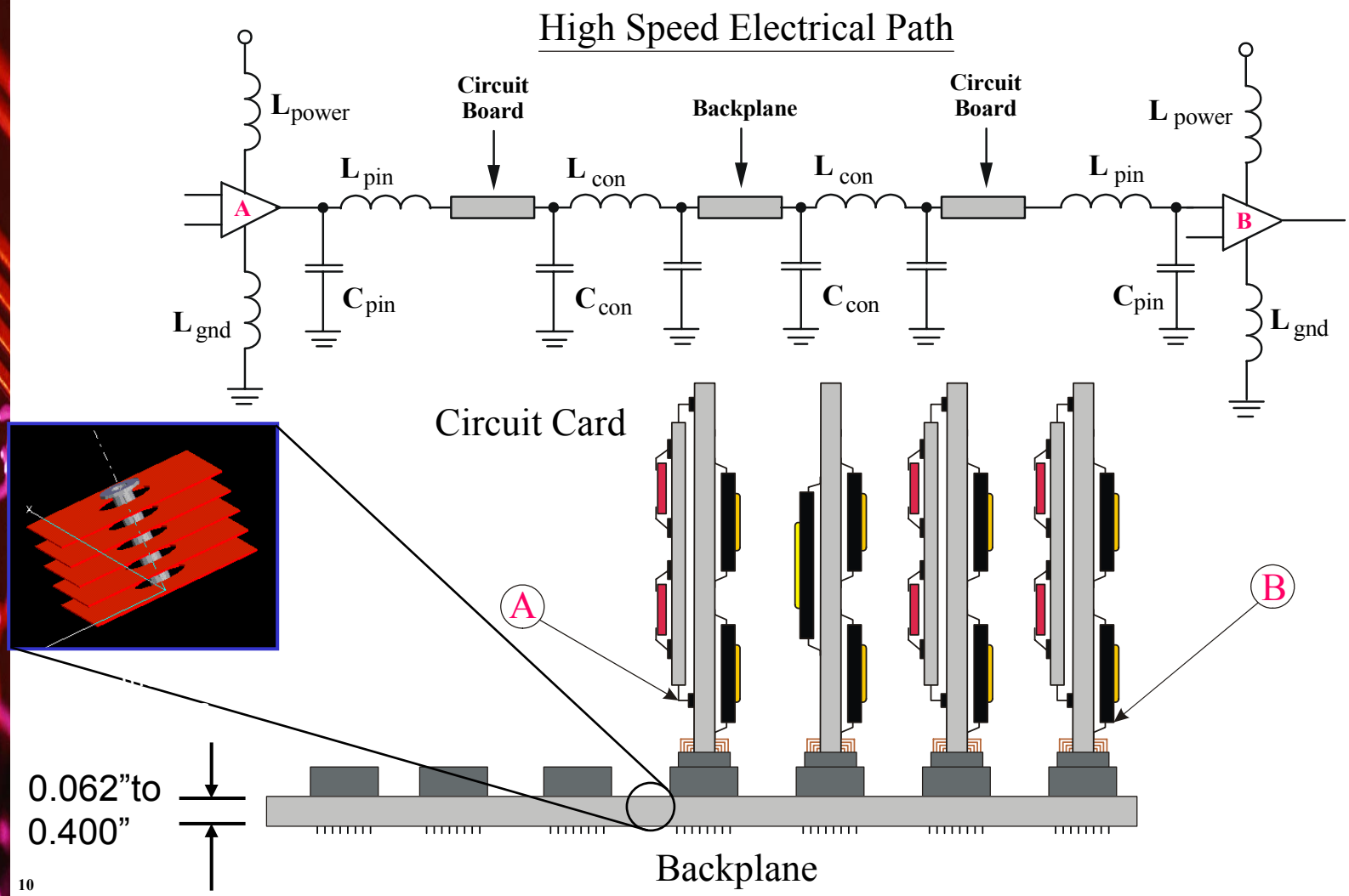


High Data Rates

0.6 Gbit/s
1.2 Gbit/s → FR-4 Epoxy Glass
2.5 Gbit/s
3.125 Gbit/s → Low Loss Epoxies
10 Gbit/s → RF Materials/Mixed

# Dynamic Details, Inc.

## The Electrical Path Is Now A 3 D Problem!



# Impact Of Current Trends On PWB Technology



**Conflicting Design Requirements**

**Increasing Signal Speeds & Frequency**

- Increased line width to reduce copper loss
- Minimum length routing
- Matched length routing
- Well characterized FR-4 and or low loss dielectrics materials
- Differential signaling between adjacent pins
- Via parameters must be characterized

**Increasing I/O Density & Reduced I/O Pitch**

- BGA escape driving up layer count
- Line widths driven down to 50 mm to 75 mm to allow escape
- Increasing layer counts driving up substrate thickness & Via length
- Smaller via diameters required for escape
- Dramatic increase in Cu plating aspect ratio
- Solder Mask registration becoming an issue with chip scale geometries

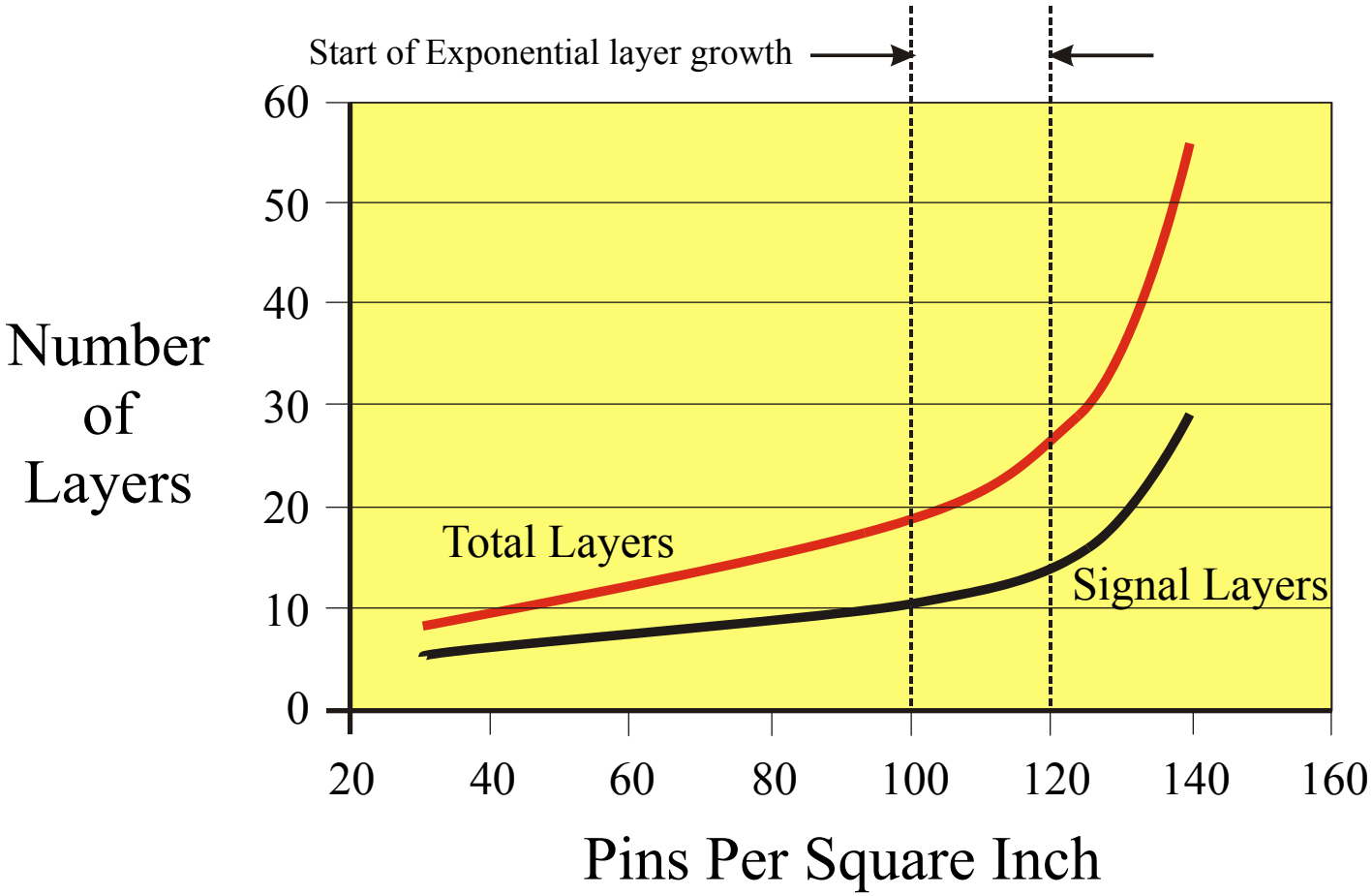
# Factors Driving Circuit Density & Cost



- Factors that will determine the break point between Conventional through hole and advanced structures:
  - Large scale use of 1.0mm BGA packages
  - Minimum component pitch (Chip scale < 0.8 mm)
  - Localized density
    - Single device with extremely high I/O (escape limited)
    - Local use of Chip Scale components
  - High density double sided designs
  - Surface Power and ground
  - Minimum drilled hole and line/space rules
  - Electrical constraints
    - Controlled length for timing
    - Line width to minimize copper loss
- The bottom line; via density is driving layer count !

# MLB Layer Count vs Component Pin Density

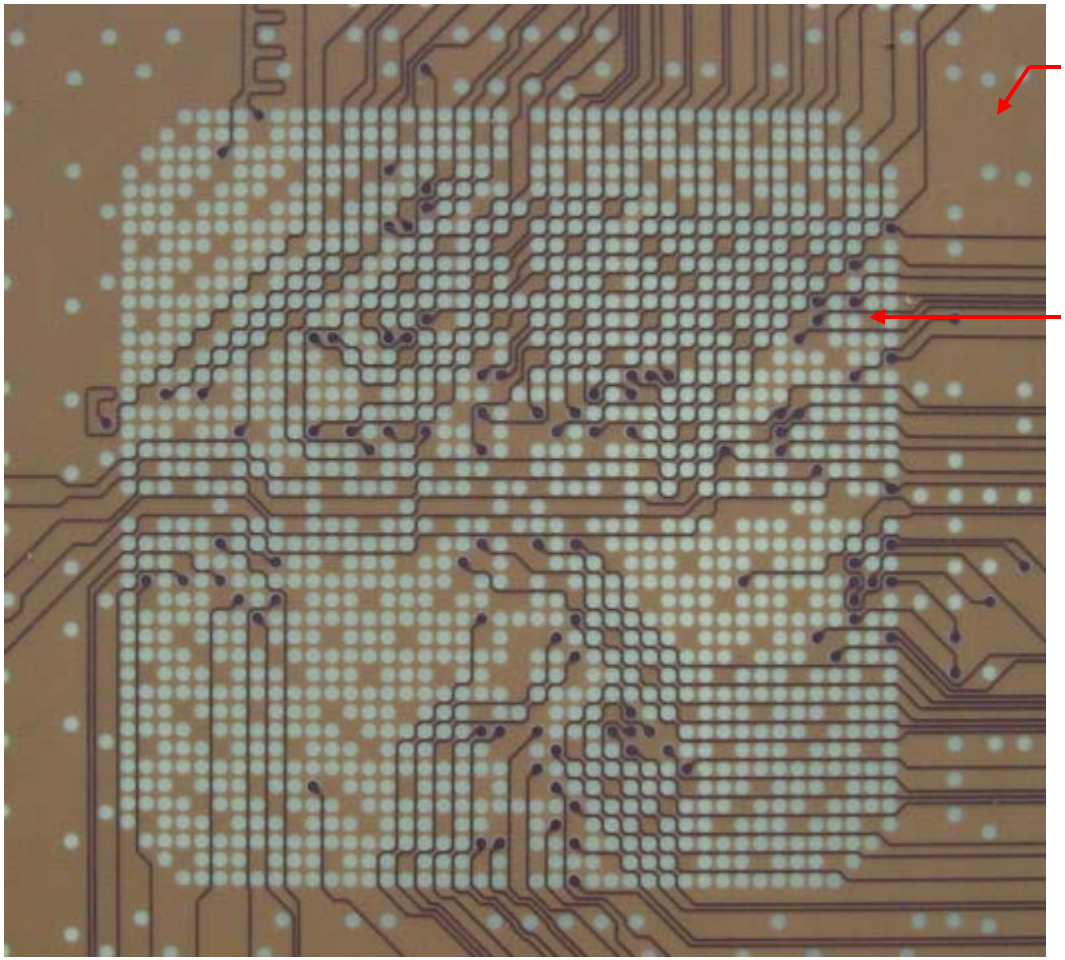




# Multilayer Signal Routing Efficiency



1.0 mm BGA Signal Layer (42 x 42 array)



5 mil line and 5 mil space yields a channel density of 100 in./in.^2 outside the array

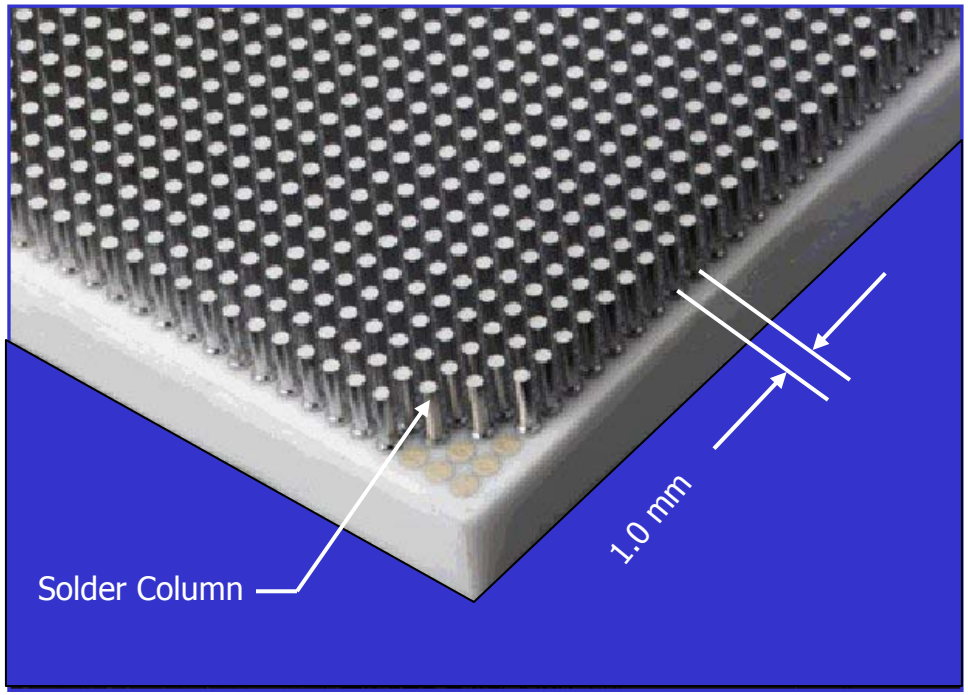
Channel density within array 25 in.in.^2

Global X,Y routing efficiency greatly reduced by large arrays

Solution:
Minimize through holes

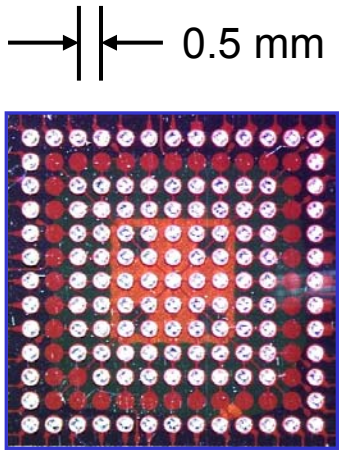
# Array Package Trends I/O's Up Pitch Down






2577 I/O 1.0 mm Ceramic Column Grid Array (CCGA) Approx. package size 52mm x 52 mm (2.04" x 2.04")

130 I/O 0.5 mm BGA Approx. package size 7.5 mm x 7.5mm (0.3" x 0.3")




Packaging Trends

# Increasing I/O Density Decreasing BGA Pitch

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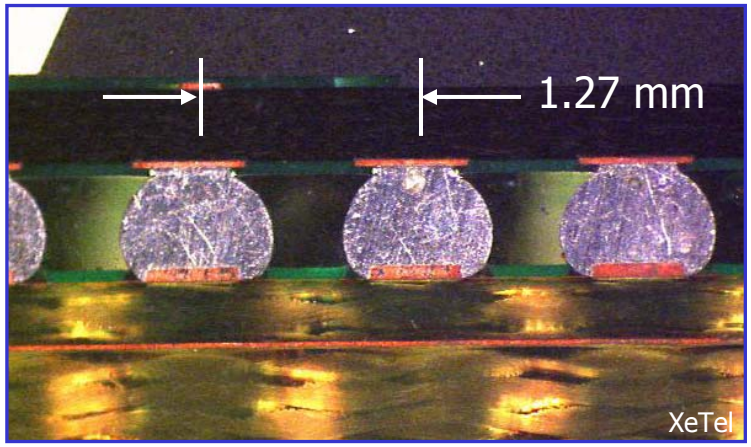
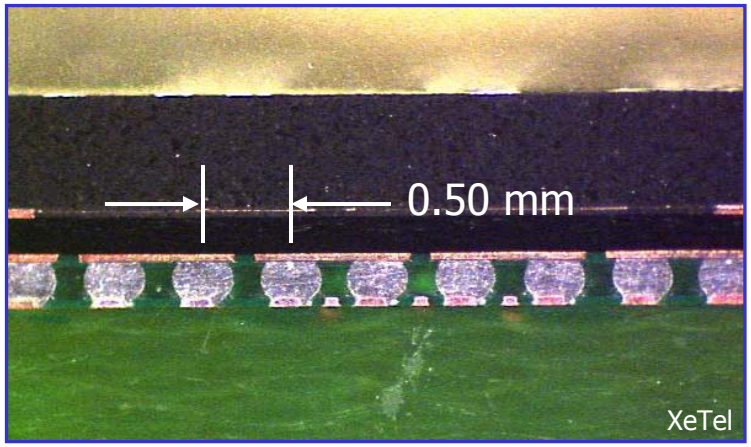



1.27 mm BGA package
Localized via density
62/cm$^2$ (400/in.$^2$)

6.45 x Increase in via density

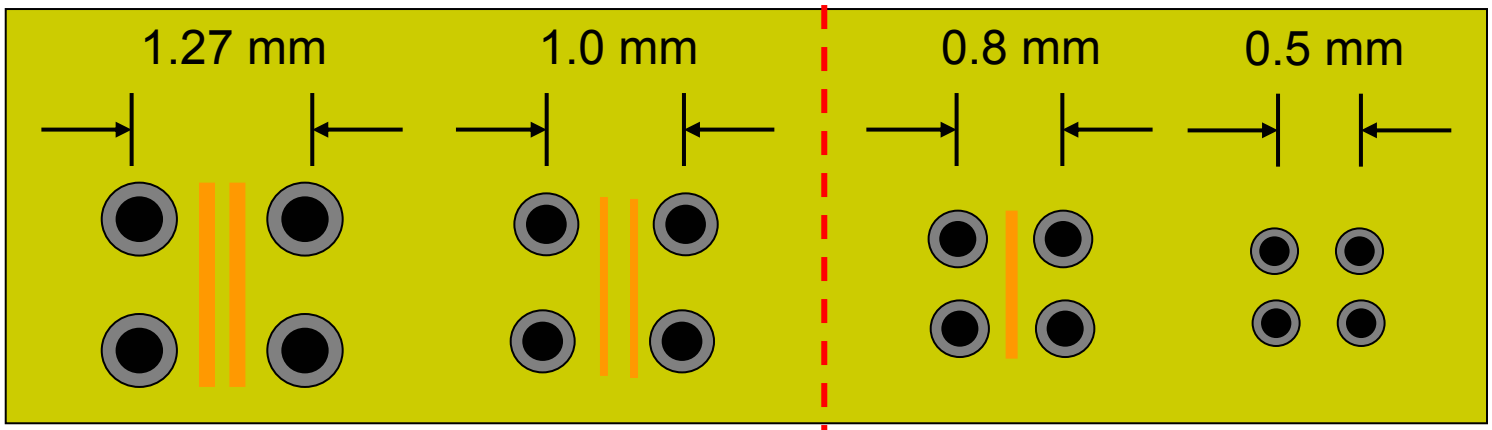



0.50 mm BGA package
Localized via density
400/cm$^2$ (2580/in.$^2$)

# Circuit Density vs BGA Pitch (Mechanical Drill)

Enabling Technologies

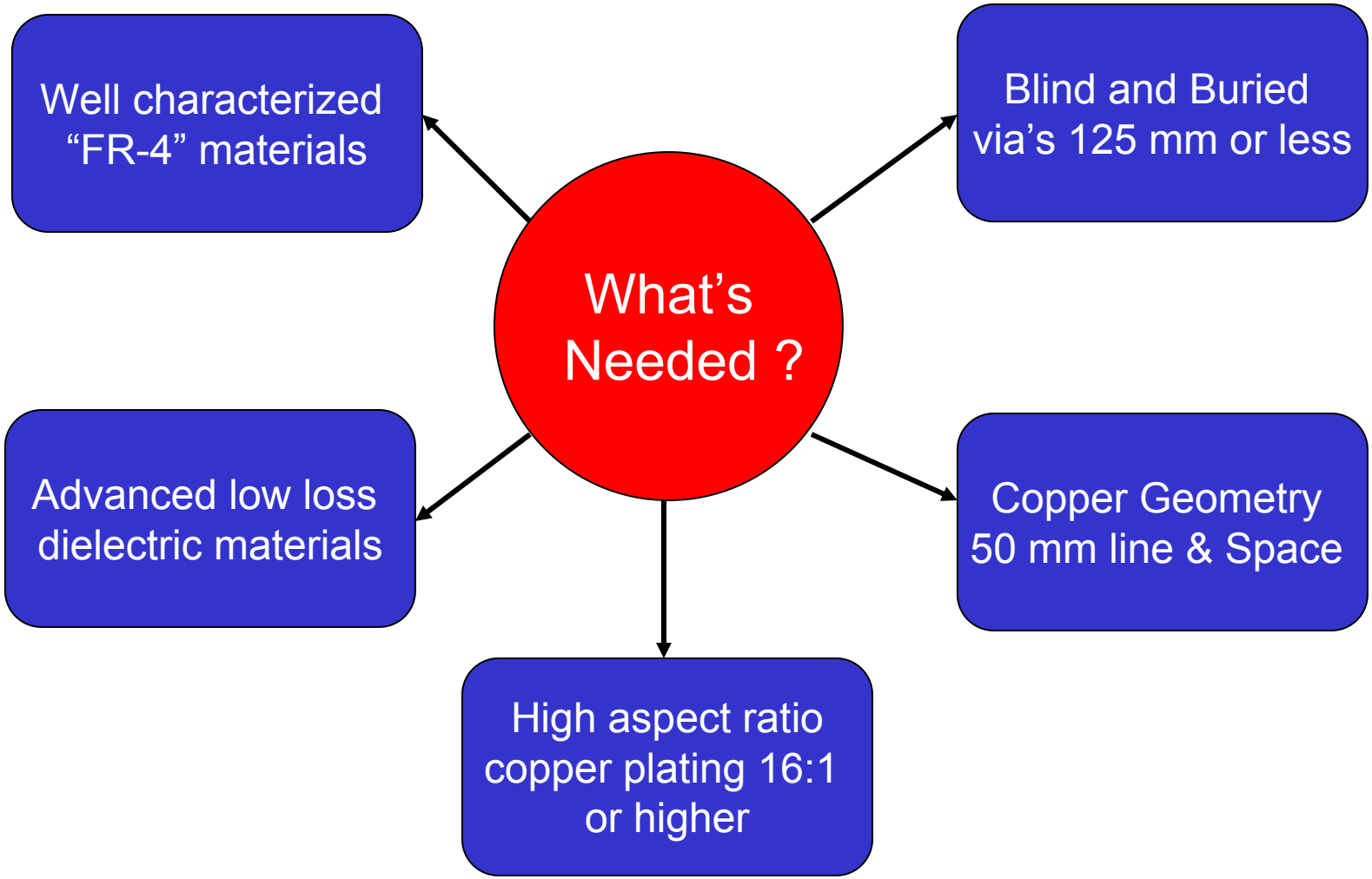
Decreasing Channel Density → Technology Shift → Increasing $




| | | | | |
|---|---|---|---|---|
| Drill dia. | 12 mils | 10 mils | 8 mils | 6 mils |
| Pad dia. | 25 mils | 20 mils | 20 mils | 16 mils |
| Line width | 5 mils | 3.5 mils | 3.5 mils | N/A |
| Space | 5 mils | | | |
| Hole density | 400/in. | 625/in. | 1008/in. | 2580/in. |
| Channel | 40 in./in.^2 | 50 in./in.^2 | 31 in./in.^2 | Escape Only ! |

# PWB Technology Requirements





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- Hybrid Constructions
- Laser Direct Imaging
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- Planar Via Technologies

Enabling Technologies

# Dynamic Details, Inc.

## Advanced Low Loss Dielectric Laminates

| Material | Composition | Tg | Dielectric Constant | | Loss Tangent | |
|---|---|---|---|---|---|---|
| **Generic FR-4 Laminates Families** | | | 1 MHz | 1 GHz | 1 MHz | 1 GHz |
| Tetafunctional (FR-4) | Epoxy/Woven:E-glass | 135 C | 4.7 | 4.25 | 0.025 | 0.016 |
| Multifunctional (FR-4) | Epoxy/Woven:E-glass | 150 C | 4.6 | 4.07 | 0.025 | 0.014 |
| High Grade Multifunctional | Epoxy/Woven:E-glass | 175 C | 4.4 | 3.9 | 0.023 | 0.012 |
| **Special Purpose FR-4 Laminates** | | | 1 MHz | 2.5 GHz | 1 MHz | 2.5 GHz |
| Low CTE FR-4 (N4000-7) | Epoxy/Woven: E-Glass | 155 C | 4.5 | 3.9 | 0.018 | 0.017 |
| | | | 1 GHz | 10 GHz | 1 GHz | 10 GHz |
| CAF Resistant FR-4 (N4000-12) (Lead Free Compatible) | Epoxy/Woven: E-Glass | 190 C | 3.7 | 3.6 | 0.010 | 0.008 |
| | | | 1 Mhz | 2 GHz | 1 Mhz | 2 GHz |
| CAF Resistant FR-4 (IS410) (Lead Free Compatible) | Epoxy/Woven: E-Glass | 190 C | 4.6 | 3.9 | 0.023 | 0.023 |

# Advanced Low Loss Dielectric Laminates

Enabling Technologies

| Material | Composition | Tg | Dielectric Constant | | Loss Tangent | |
|---|---|---|---|---|---|---|
| **High Performance Laminates** | | | 1 MHz | 1 GHz | 1 MHz | 10 GHz |
| Nelco (N7000-1) | Polyimide/Woven:E-glass | 260 C | 4.3 | 3.7 | 0.013 | 0.007 |
| Isola (P95) | Polyimide/Woven:E-glass | 260 | 4.4 | 4.2 | 0.016 | 0.014 |
| Arlon (85N) | Polyimide/Woven:E-glass | 260 | | 4.2 | | 0.012 |
| Nelco (N4500-6T) | Epoxy/NonWoven:Aramid | 180 C | 3.9 | 3.5 | 0.024 | 0.022 |
| Nelco (N8000) | Cyanate Ester/Woven:E-glass | 240 C | 3.8 | 3.5 | 0.008 | 0.006 |
| ISOLA (G200) | BT/Woven:E-glass | 185 C | 4.1 | 3.9 | 0.013 | 0.009 |
| Nelco (N5000) | BT/Woven:E-glass | 185 C | 4.1 | 3.8 | 0.013 | 0.010 |
| Nelco (N5000-32) Black | BT/Woven:E-glass | 205 C | | 4.1 | | 0.009 |
| MGC (832) Black | BT/Woven:E-glass | 205 C | | 4.1 | | 0.009 |
| Mitsui Chemical (BN300) | BT/Woven:E-glass | 300 C | | 4.0 | | 0.004 |

# Advanced Low Loss Dielectric Laminates

Enabling Technologies

| Material | Composition | Tg | Dielectric Constant | | Loss Tangent | |
|---|---|---|---|---|---|---|
| **High Performance Epoxy** | | | 1 MHz | 10 GHz | 1 MHz | 10 GHz |
| GE GETEK | Epoxy-PPO/Woven:E-glass | 180 C | 3.9 | | 0.012 | |
| Nelco N4000-13 | Epoxy/Woven:E-glass | 200 C | 3.9 | 3.8 | 0.009 | 0.010 |
| Nelco N4000-13 SI | Epoxy/Woven:Glass * | 200 C | 3.6 | 3.5 | 0.008 | 0.007 |
| Isola FR-408 | Epoxy/Woven:E-glass | 180 C | | 3.7 | | 0.010 |
| Isola IS620 | Epoxy/Woven E-Glass | 210 C | | 3.58 | | 0.0086 |
| **High Frequency Laminates** | | | 10 GHz | | 10 GHz | |
| Rogers 4003 | Hydrocarbon/Ceramic/Woven:Glass | 280 C | 3.38 | | 0.0027 | |
| Rogers 4350 | Hydrocarbon/Ceramic/Woven:Glass | 280 C | 3.48 | | 0.0040 | |
| Rogers 4403 (Prepreg) | 4000 Series Resin/1080 style Glass | 280 C | 3.2 | | 0.005 | |
| Arlon 25N) | Ceramic Filled PTFE/Woven:Glass | | 3.5 | | 0.0024 | |
| Arlon 25FR | Ceramic Filled PTFE/Woven:Glass | | 3.48 | | 0.003 | |

# Advanced Low Loss Dielectric Laminates

Enabling Technologies

| Material | Composition | Tg | Dielectric Constant | Loss Tangent |
|---|---|---|---|---|
| **High Frequency Laminates** | | | 10 GHz | 10 GHz |
| Isola GIGAVER | APPE/Woven Glass | 210 C | 3.52 | 0.0114 |
| Taconics TLE-95 | PTFE/Woven:Glass | | 2.95 | 0.0028 |
| Taconics TLX | PTFE/Woven:E-glass | | 2.50 | 0.0019 |
| Taconics HT 1.5 | Bonding Film | | 2.35 | 0.0025 |
| W.L.Gore Speed Board N | Expanded PTFE/Epoxy Resin | | 2.73 | 0.0192 |
| W.L.Gore Speed Board C | Expanded PTFE/Cyanate Ester | | 2.56 | 0.0038 |

# Advanced Low Loss Dielectric Laminates

Enabling Technologies

| Material | Composition | Dielectric Constant | Loss Tangent |
|---|---|---|---|
| **Microwave Laminates** | | 10 GHz | 10 GHz |
| Rogers RO3003 | PTFE/Ceramic | 3.00 | 0.0013 |
| Rogers RO3006 | PTFE/Ceramic | 6.15 | 0.0025 |
| Rogers RO3010 | PTFE/Ceramic | 10.2 | 00035 |
| Rogers RT/duroid 5870 | PTFE/Glass Microfiber | 2.33 | 0.0012 |
| Rogers RT/duroid 5880 | PTFE/Glass Microfiber | 2.20 | 0.0009 |
| Rogers TMM 3 | Hydrocarbon/Ceramic | 3.27 | 0.0020 |
| Rogers TMM 4 | Hydrocarbon/Ceramic | 4.50 | 0.0020 |
| Rogers TMM 6 | Hydrocarbon/Ceramic | 6.00 | 0.0023 |
| Rogers TMM 10 | Hydrocarbon/Ceramic | 9.2 | 0.0023 |
| Rogers 3001 (Bonding Film) | Thermoplastic | 2.28 | 0.003 |

# Advanced Low Loss Dielectric Laminates

Enabling Technologies

| Material | Composition | Tg | Dielectric Constant | | Loss Tangent | |
|---|---|---|---|---|---|---|
| **Special Purpose Micro-Via Dielectric Material** | | | 1 MHz | 1 GHz | 1 MHz | 10 GHz |
| Nelco 4500-6T | Epoxy/Resin Coated Foil | 180 C | 3.9 | 3.5 | 0.024 | 0.022 |
| Polyclad PCL-CF-400 | Epoxy/Resin Coated Foil | 165 C | 3.5 | 3.3 | 0.02 | 0.02 |
| Thermont | Random Aramid Fiber | 180 C | 3.9 | 3.5 | 0.024 | 0.022 |
| Nelco 1080 LD Prepreg | Uniform Weave 1080 (N4000-6 Resin) | 175 C | 4.4 | 3.9 | 0.023 | 0.012 |
| Nelco 106 LD Prepreg | Uniform Weave 106 (N4000-6 Resin) | 175 C | 4.4 | 3.9 | 0.023 | 0.012 |
| Gore Microlam® 610 | Expanded PTFE/ Resin | | 2.86 @ 2.9 GHz | | 0.016 @ 2.9 GHz | |
| Gore Microlam® 630 | Expanded PTFE/ Resin | | 2.6 @ 10 GHz | | 0.004 @ 10 GHz | |

Enabling Technologies

# UK Directive

**Definition of RoHS:** **The Restriction of Hazardous Substances in Electrical and Electronic Equipment (RoHS)**

**Who does it affect?**

- **Manufacturers, sellers, distributors and recyclers of electrical and electronic equipment containing lead, mercury, cadmium, hexavalent chromium, polybrominated biphenyls or polybrominated diphenyl ethers.**
- **From 1 July 2006 new electrical and electronic equipment will not contain lead, mercury, cadmium, hexavalent chromium, polybrominated biphenyls or polybrominated diphenyl ethers.**

# "Green" Materials



## Definition of RoHS Compliance for Materials

| Material | Allowable Amount by weight |
|---|---|
| Lead (Pb) | 0.1% by weight |
| Cadmium (cd) | <0.01% by weight |
| Mercury (Hg) | 0.1% by weight |
| Hexavalent Chromium (Hex-Cr) | <0.1% by weight |
| Polybrominated Biphenyls (PBB – fire retardant) | 0.1% by weight |
| Polybrominated Diphenyl Ethers (PBDE- fire retardant) | 0.1% by weight |

# "Green" Materials

Enabling Technologies

| Material | Resin System | (DSC) Tg | (1 GHz) εr | Loss tan |
|---|---|---|---|---|
| Nelco coming soon | Halogen-Free Epoxy | 180°C | ? | ? |
| Isola DE 156 Duraver® | Halogen-Free Epoxy | 160°C | 4.6 | .020 |
| Polyclad HF-541 | Halogen-Free Epoxy | 145°C | 4.3 | .015 |
| Polyclad HF-571 | Halogen-Free Epoxy | 165°C | 4.4 | .010 |
| Hitachi MCL-BE-67G | Halogen-Free FR4 | 200°C DMA | 4.4 | .010 |
| Matsushita R-1566 | Halogen-Free FR4 | 145°C | 4.35 | .017 |
| *MGC CCL-EL-150 | Halogen-Free FR4 | 155°C | 4.8 | .010 |
| Arlon 65GT | Epoxy/Thermount | 150 | 3.45 | .020 |
| Rogers RO4003C™ | Hydrocarbon/Ceramic | >280°C | 3.38 | .0027 |

*Mitsubishi Gas Chemical

# "Lead Free" Materials

Enabling Technologies

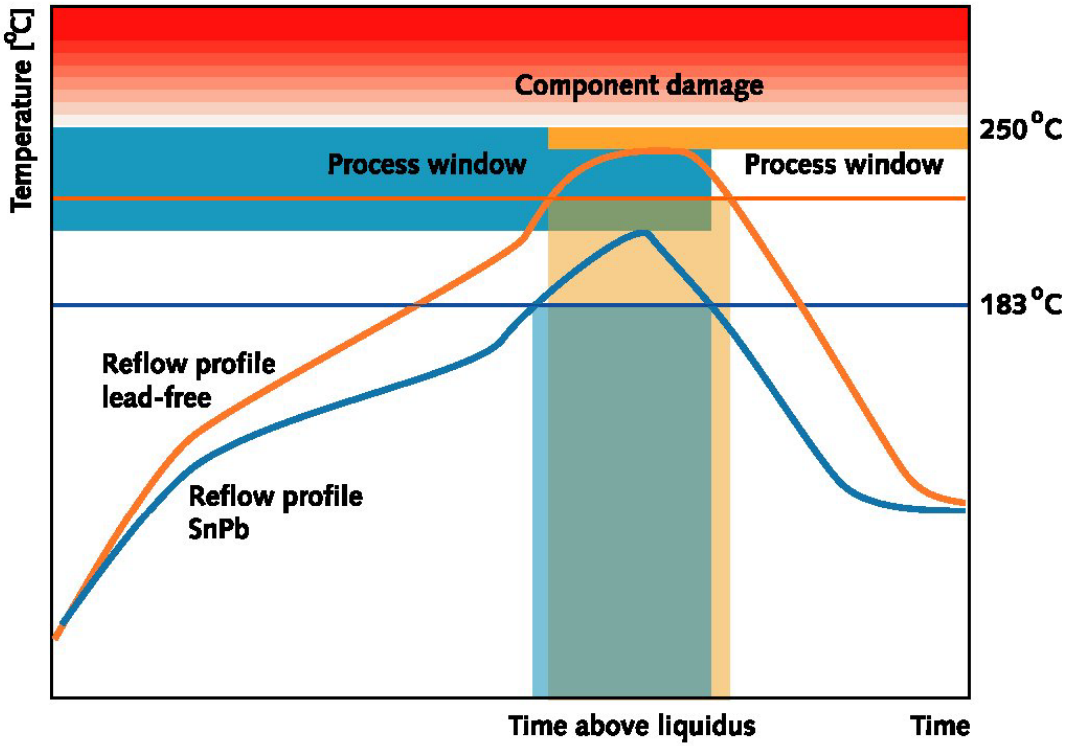
| Material | Resin System | (DSC) Tg | (1 GHz) Dk | Df |
|---|---|---|---|---|
| Isola IS 410 | High Performance Epoxy | 180°C | 4.25 | .019 |
| Nelco N4000-11 | Multifunctional | 175°C | 4.1 | .016 |
| Hitachi MCL-BE-67G | Halogen-Free FR4 | 200°C DMA | 4.4 | .010 |
| Nelco N4000-12 | Enhanced Epoxy | 190°C | 3.7 (10 GHz) | .008 |

UL V0 IPC 4101A/29

**Lead-Free Assembly Passes 6x @ 288 degrees C**
**Robust Thermal Stability**

# "Lead Free" Solder Profile






Solder Re-Flow Profile

Higher temperature & dwell time exceed current FR-4 process limits

Materials with higher Tg, Low Z axis CTE and improved T-288 resistance will be required

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## Overview

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- Laser Drilling
- Planar Via Technologies

# Dielectric Properties of "FR-4" Laminate

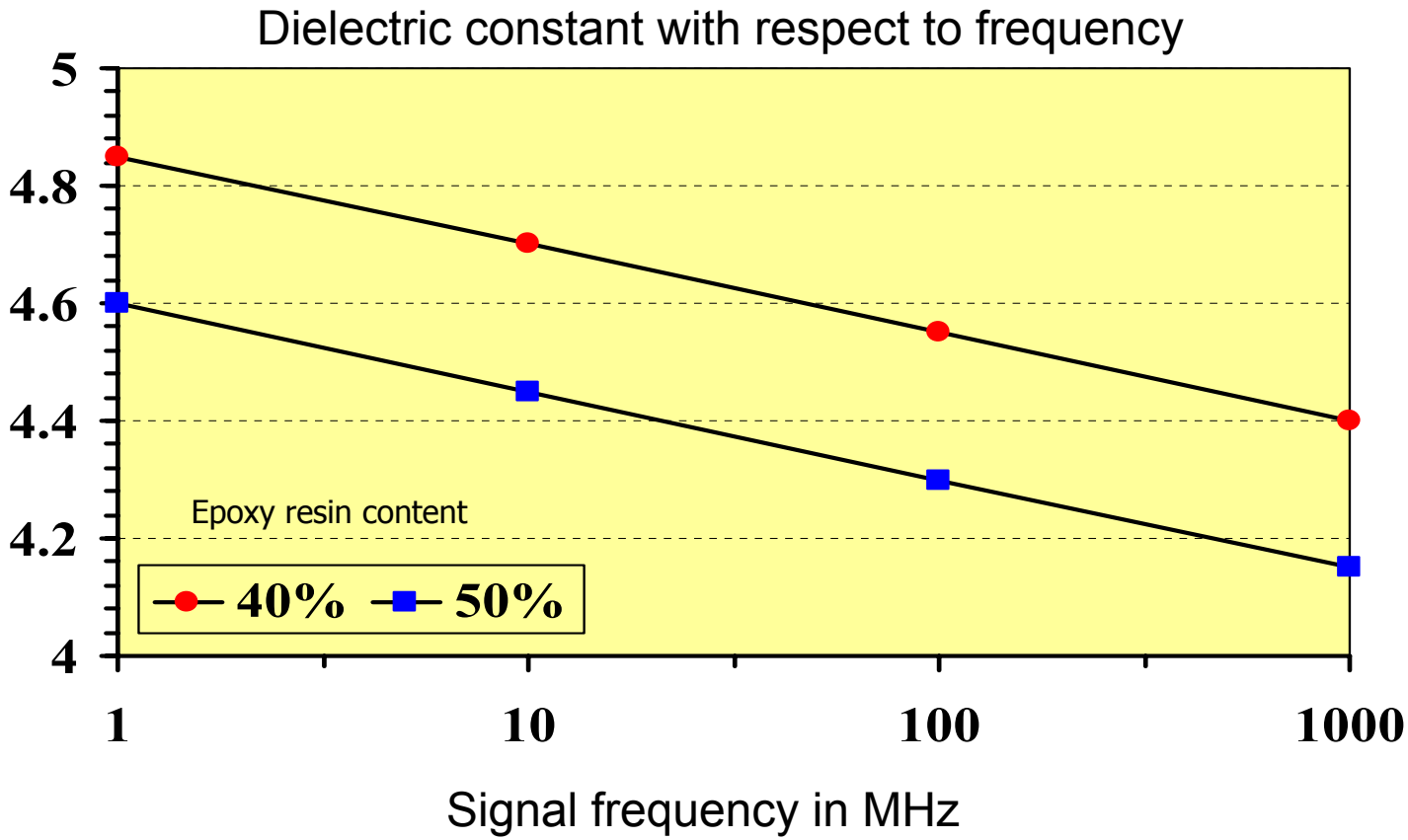


## Factors that influence dielectric constant and loss tangent:

- Signal frequency
- Temperature
- Moisture content
- Glass composition
- Ratio of epoxy resin to glass in the construction

# Dielectric Properties of “FR-4” Laminate

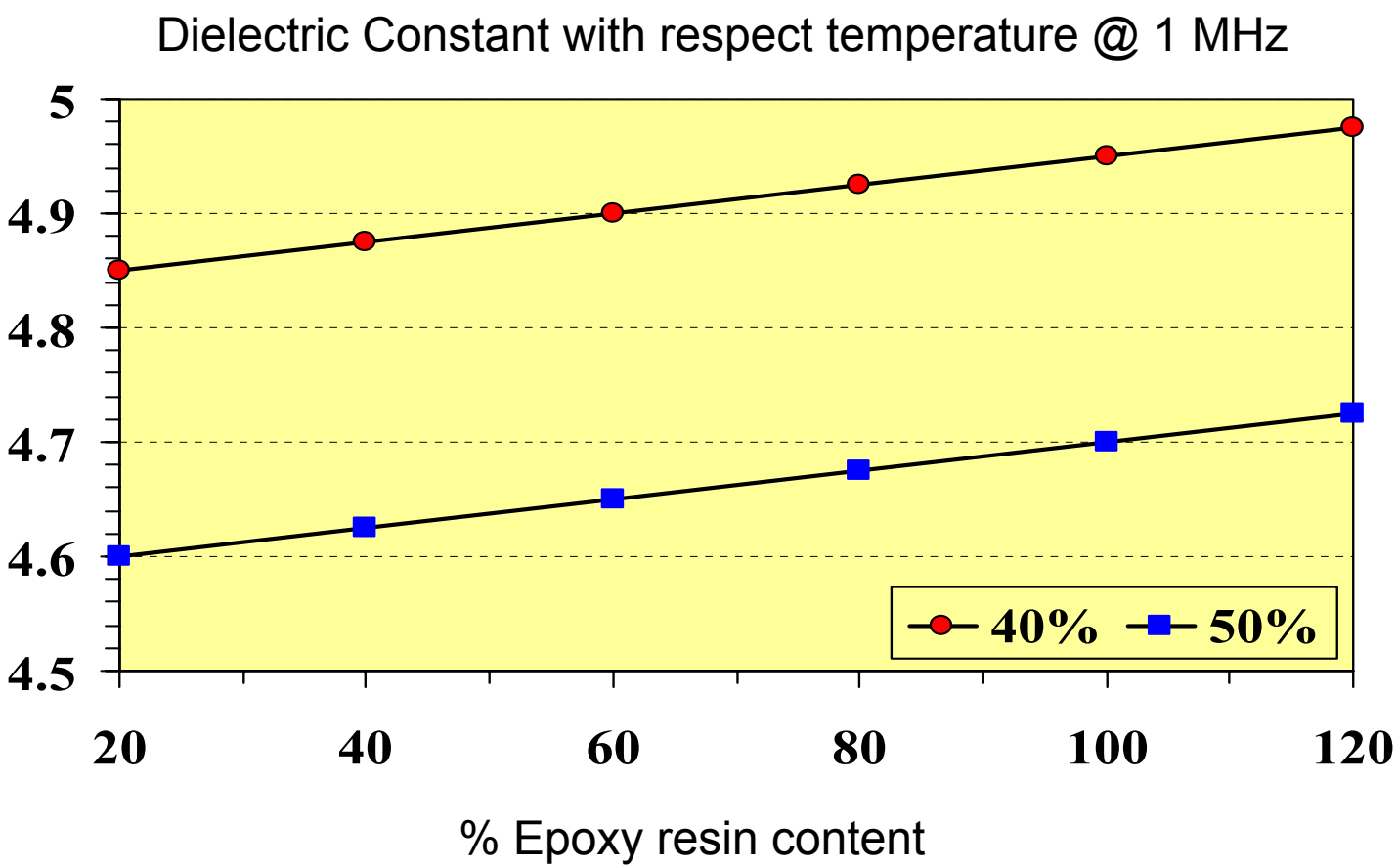





Source: D. Heywood, “Controlled Impedance PCB’s from FR4 Material”, Isola Werke UK LTD report

# Dielectric Properties of "FR-4" Laminate

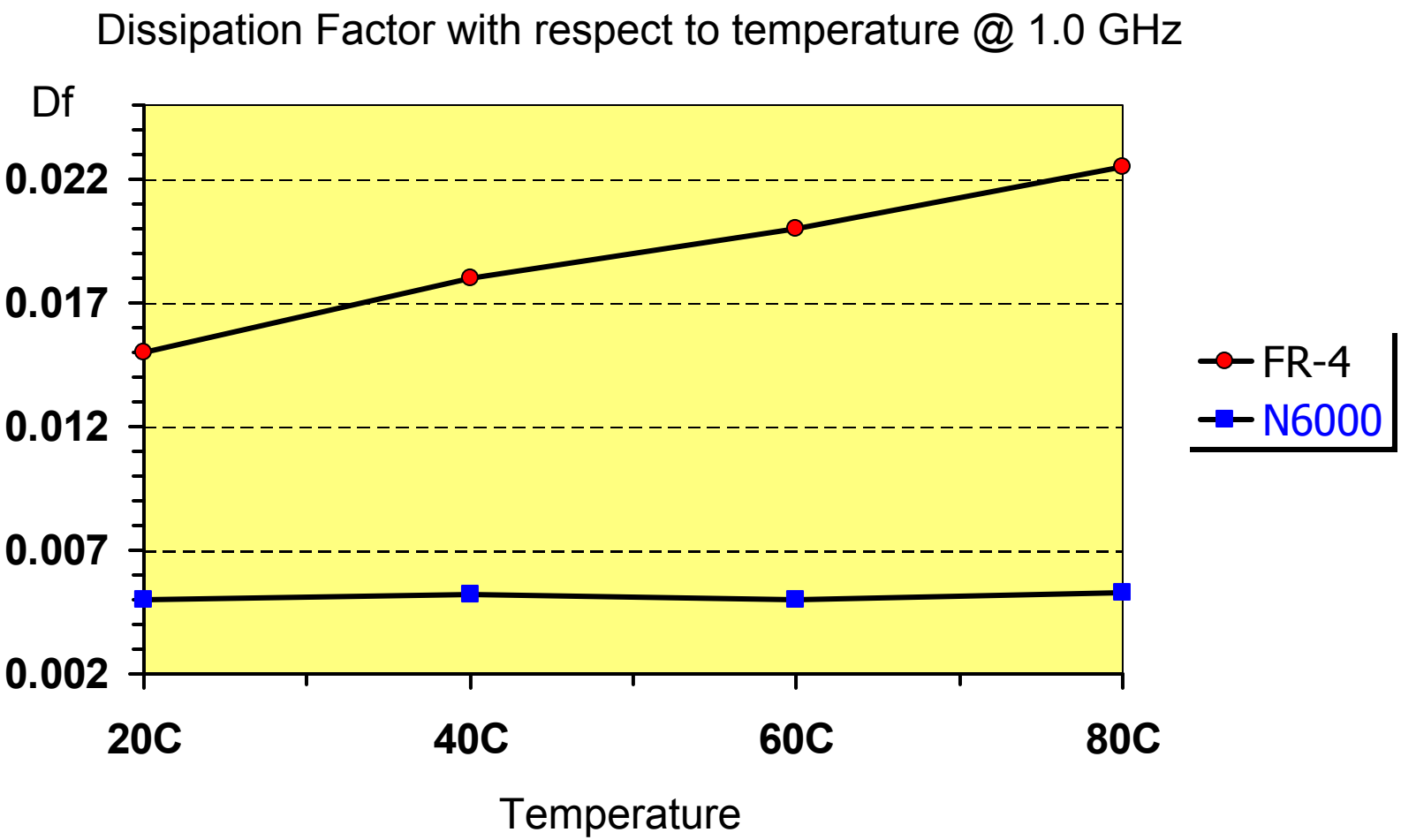
Enabling Technologies




Source: D. Heywood, "Controlled Impedance PCB's from FR4 Material", Isola Werke UK LTD report

# Dielectric Properties of "FR-4" Laminate



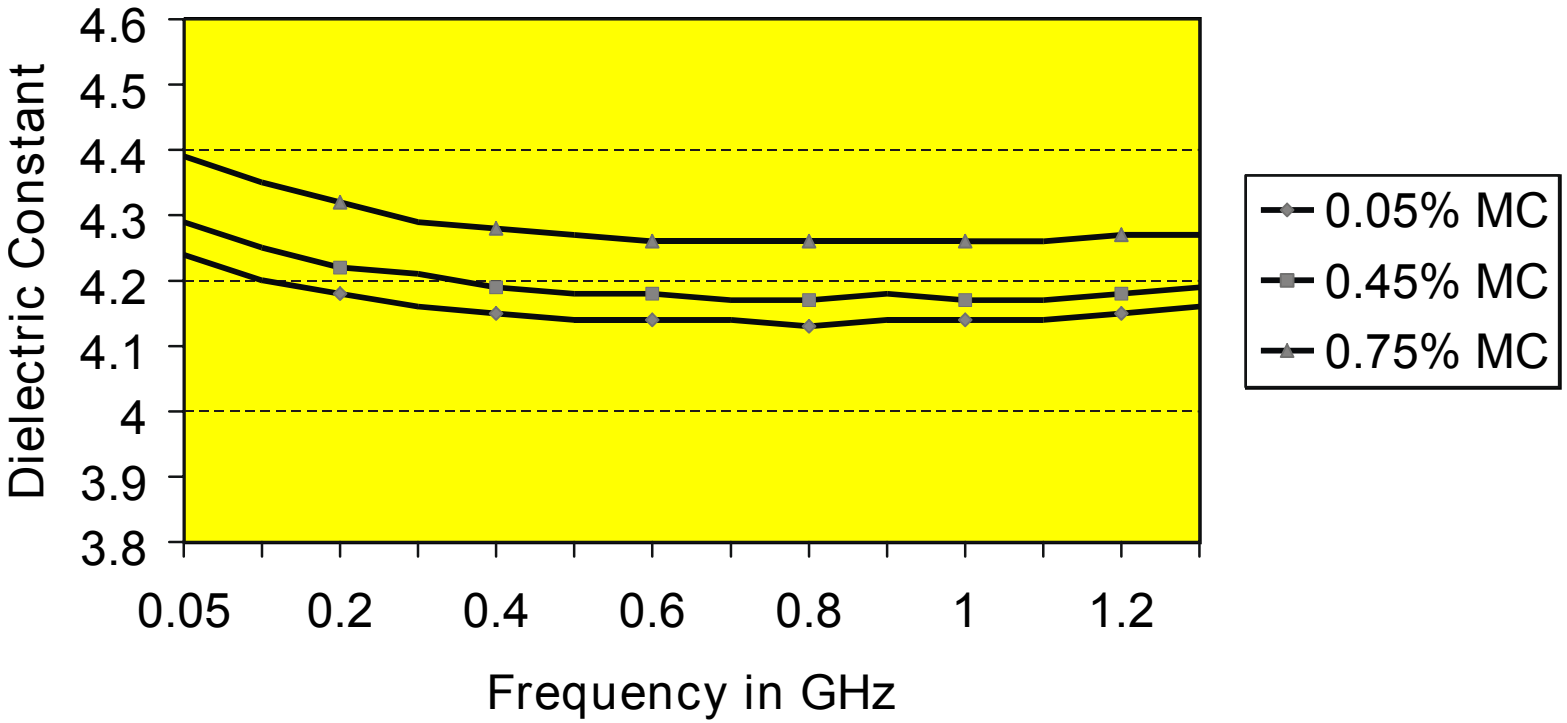



Data Source: Park-Nelco

# Dielectric Properties of "FR-4" Laminate

Enabling Technologies

Dielectric constant with respect to frequency & moisture content




FR-406
44.6 % epoxy resin

Data Source: Isola

# Dielectric Constant of “FR-4” Laminate

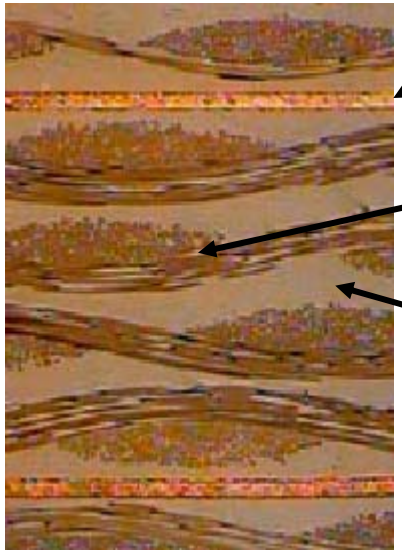


## Considerations:

- Standard “FR4” epoxy-glass laminates can maintain a dielectric constant tolerance of less than +/- 0.2 based on a specific laminate construction and resin content
- Standard tolerance on prepreg resin content is +/- 1.5% as supplied by vendors, +/- 1.0% can be attained for critical applications (special order)
- Resin content in prepreg varies for each style of prepreg
- Prepreg resin content is reduced in high pressure lamination do to flow in the melt phase

# Epoxy-Glass Laminate Construction





PWB Cross-Section

Copper Foil

Woven glass fabric
High dielectric constant ($e_r \sim 6$)

Epoxy resin
Low dielectric constant ($e_r \sim 3.5$)

- Dielectric constant of the composite laminate is a function of the resin/glass ratio
- Composite laminates can have many different resin/glass constructions

Photo Courtesy of Park Nelco

# Epoxy-Glass Laminate Construction

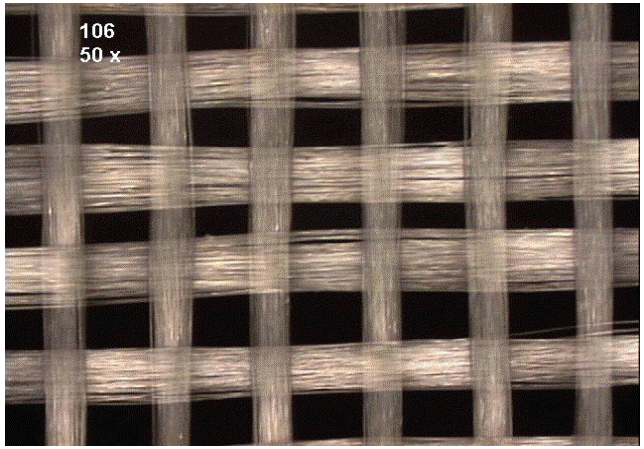


Standard glass fabrics used in the construction of Prepreg & Laminate

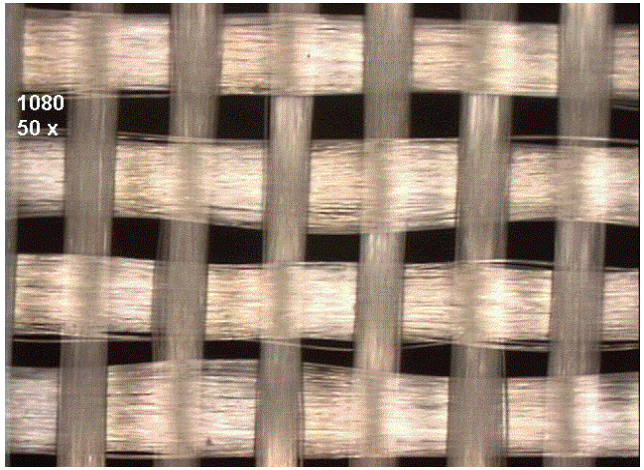
| Glass | Count Warp | Count | Warp Yarn | Yarn Fill | Glass Thickness |
|---|---|---|---|---|---|
| 106 | 56 | 56 | ECD-900 1/0 | ECD-900 1/0 | 0.0015 |
| 1080 | 60 | 47 | ECD-450 1/0 | ECD-450 1/0 | 0.0025 |
| 1280 | 60 | 60 | ECD-450 1/0 | ECD-450 1/0 | 0.0022 |
| 2113 | 60 | 56 | ECE-225 1/0 | ECD-450 1/0 | 0.0029 |
| 2116 | 60 | 58 | ECE-225 1/0 | ECE-225 1/0 | 0.0038 |
| 3070 | 70 | 70 | ECDE-300 1/0 | ECDE-300 1/0 | 0.0034 |
| 1652 | 52 | 52 | ECG-150 1/0 | ECG-150 1/0 | 0.0045 |
| 7628 | 44 | 31 | ECG-75 1/0 | ECG-75 1/0 | 0.0068 |

# Epoxy-Glass Laminate Construction






Glass Style: 106
Plain Weave
Count: 56x56 (ends/in)
Thickness: 0.0015”



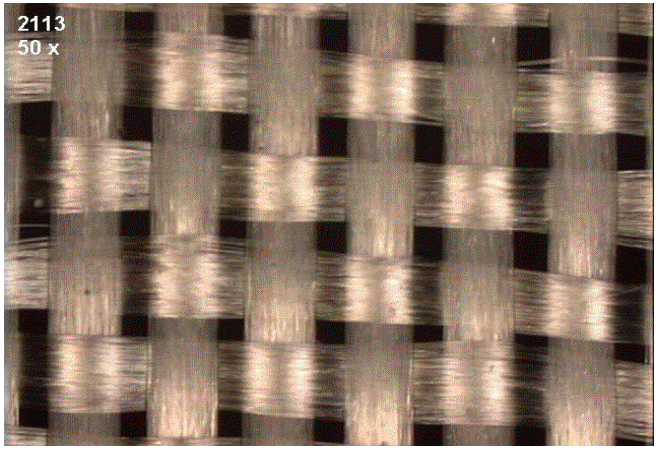

Glass Style: 1080
Plain Weave
Count: 60x47 (ends/in)
Thickness: 0.0025”

**NOTE:**
The plain weave yarn consists of yarns interlaced in an alternating fashion one over and one under every yarn.

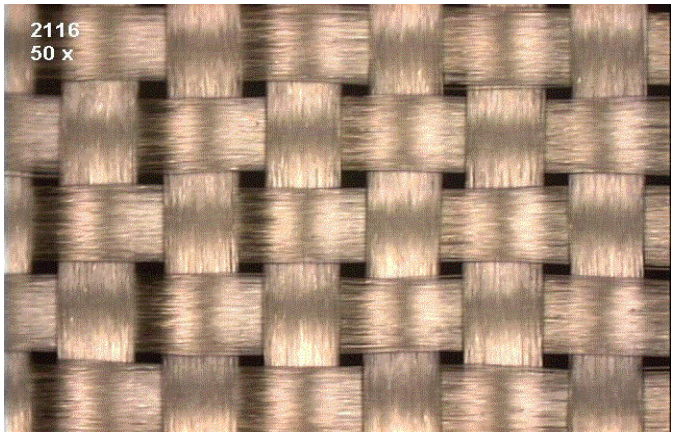
Source: Isola

# Epoxy-Glass Laminate Construction






Glass Style: 2113
Plain Weave
Count: 60x56 (ends/in)
Thickness: 0.0029”

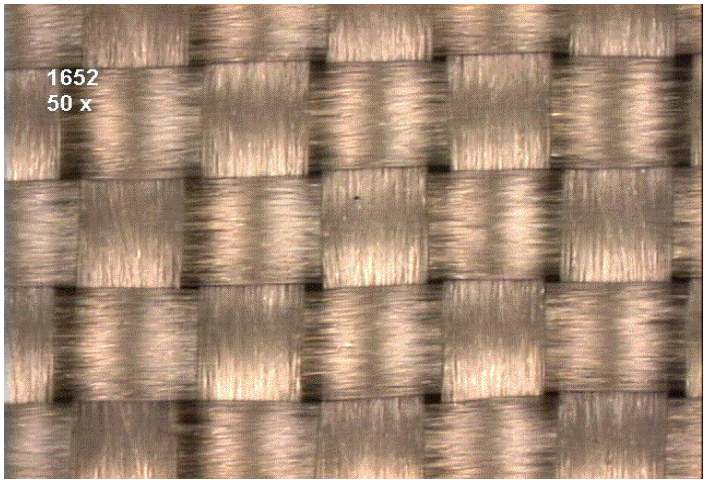



Glass Style: 2116
Plain Weave
Count: 60x58 (ends/in)
Thickness: 0.0038”

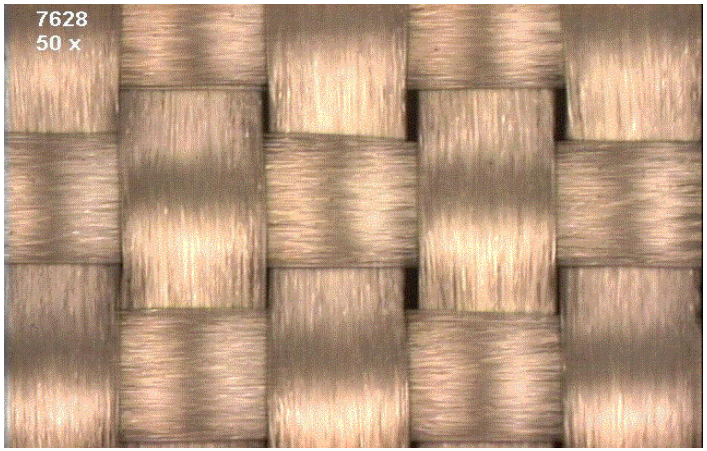
Source: Isola

# Epoxy-Glass Laminate Construction






Glass Style: 1652
Plain Weave
Count: 52x52 (ends/in)
Thickness: 0.004”




Glass Style: 7628
Plain Weave
Count: 44x32 (ends/in)
Thickness: 0.0068 (in)

Source: Isola

# Epoxy Glass Laminate Properties N4000-6

Enabling Technologies

## Dielectric properties based on construction & frequency (N4000-6)

| Thickness | Tolerance | Construction | RC% | Dielectric Constant 1MHz | Tol. | 1GHz | Tol. | 2.5 GHz | Tol. | 10 GHz | Tol. |
|---|---|---|---|---|---|---|---|---|---|---|---|
| 0.002 | 0.0005 | 1x 106 | 69.0 | 3.84 | 0.11 | 3.63 | 0.12 | 3.66 | 0.07 | 3.60 | 0.08 |
| 0.003 | 0.0005 | 1x 1080 | 62.0 | 4.00 | 0.10 | 3.80 | 0.11 | 3.76 | 0.06 | 3.72 | 0.08 |
| 0.004 | 0.0005 | 1 x 2113 | 54.5 | 4.19 | 0.11 | 4.00 | 0.11 | 3.88 | 0.07 | 3.85 | 0.80 |
| 0.004 | 0.0005 | 1x 106 1x 108 | 57.7 | 4.11 | 0.09 | 3.91 | 0.10 | 3.83 | 0.06 | 3.79 | 0.07 |
| 0.004 | 0.0005 | 1x 2116 | 43.0 | 4.54 | 0.15 | 4.37 | 0.16 | 4.09 | 0.09 | 4.11 | 0.11 |
| 0.005 | 0.00075 | 1x 106 1x 2113 | 52.8 | 4.24 | 0.13 | 4.05 | 0.14 | 3.91 | 0.08 | 3.89 | 0.10 |
| 0.005 | 0.00075 | 1x 2116 | 51.8 | 4.26 | 0.14 | 4.08 | 0.14 | 3.92 | 0.08 | 3.91 | 0.10 |
| 0.006 | 0.00075 | 1x 1080 1x 2113 | 52.2 | 4.25 | 0.11 | 4.06 | 0.12 | 3.92 | 0.07 | 3.90 | 0.08 |
| 0.006 | 0.00075 | 1x 106 1x 2116 | 50.8 | 4.29 | 0.12 | 4.11 | 0.13 | 3.94 | 0.07 | 3.93 | 0.09 |
| 0.006 | 0.00075 | 2x 2113 | 43.5 | 4.52 | 0.15 | 4.35 | 0.16 | 4.08 | 0.09 | 4.10 | 0.11 |
| 0.006 | 0.00075 | 1x 1500 | 41.7 | 4.58 | 0.16 | 4.41 | 0.17 | 4.12 | 0.10 | 4.15 | 0.12 |
| 0.007 | 0.001 | 2x 2113 | 49.6 | 4.33 | 0.14 | 4.14 | 0.15 | 3.96 | 0.09 | 3.96 | 0.10 |
| 0.008 | 0.001 | 1x 7628 | 44.4 | 4.49 | 0.15 | 4.32 | 0.16 | 4.06 | 0.09 | 4.08 | 0.11 |
| 0.008 | 0.001 | 2x 2116 | 43.0 | 4.54 | 0.15 | 4.37 | 0.16 | 4.09 | 0.09 | 4.11 | 0.11 |
| 0.008 | 0.001 | 1x 2116 1x 2113 | 48.6 | 4.36 | 0.13 | 4.18 | 0.14 | 3.98 | 0.08 | 3.98 | 0.09 |
| 0.008 | 0.001 | 1x 7629 | 42.6 | 4.55 | 0.16 | 4.38 | 0.17 | 4.10 | 0.10 | 4.12 | 0.12 |
| 0.009 | 0.001 | 2x 2116 | 47.8 | 4.38 | 0.12 | 4.20 | 0.13 | 4.00 | 0.07 | 4.00 | 0.09 |
| 0.010 | 0.001 | 2x 2116 | 51.8 | 4.26 | 0.09 | 4.08 | 0.10 | 3.92 | 0.06 | 3.91 | 0.07 |
| 0.010 | 0.001 | 1x 7628 1x 1080 | 45.0 | 4.47 | 0.12 | 4.29 | 0.13 | 4.05 | 0.07 | 4.06 | 0.09 |
| 0.010 | 0.001 | 1x 7635 | 47.5 | 4.39 | 0.11 | 4.21 | 0.12 | 4.00 | 0.07 | 4.01 | 0.08 |
| 0.012 | 0.001 | 2x 1080 1x7628 | 45.5 | 4.46 | 0.10 | 4.28 | 0.11 | 4.04 | 0.06 | 4.05 | 0.07 |
| 0.014 | 0.0015 | 2x 7628 | 38.8 | 4.69 | 0.16 | 4.53 | 0.16 | 4.19 | 0.10 | 4.23 | 0.11 |
| 0.015 | 0.0015 | 2x 7628 | 41.7 | 4.58 | 0.13 | 4.41 | 0.14 | 4.12 | 0.08 | 4.15 | 0.10 |
| 0.018 | 0.0015 | 2x 7628 1x 2113 | 42.0 | 4.57 | 0.11 | 4.40 | 0.12 | 4.11 | 0.07 | 4.14 | 0.08 |
| 0.021 | 0.002 | 2x 7628 1x 7628 | 38.8 | 4.69 | 0.14 | 4.53 | 0.15 | 4.19 | 0.09 | 4.23 | 0.10 |

Data Source: Park Nelco

# Dynamic Details, Inc.

## Epoxy Glass Laminate Properties N4000-13

Enabling Technologies

Dielectric properties based on construction & frequency (N4000-13)

| | | | | Dielectric Constant | | | | | | | |
|---|---|---|---|---|---|---|---|---|---|---|---|
| Thickness | Tolerance | Construction | RC% | 1MHz | Tol. | 1GHz | Tol. | 2.5 GHz | Tol. | 10 GHz | Tol. |
| 0.0020 | 0.0005 | 1x 106 | 68.3 | 3.43 | 0.14 | 3.33 | 0.14 | 3.24 | 0.14 | 3.21 | 0.14 |
| 0.0025 | 0.0005 | 1x 108 | 55.2 | 3.77 | 0.16 | 3.67 | 0.16 | 3.57 | 0.15 | 3.54 | 0.15 |
| 0.0030 | 0.0005 | 1x 2113 | 42.7 | 4.09 | 0.16 | 3.99 | 0.16 | 3.88 | 0.15 | 3.84 | 0.15 |
| 0.0030 | 0.0005 | 1x 1080 | 61.2 | 3.61 | 0.12 | 3.51 | 0.12 | 3.42 | 0.12 | 3.39 | 0.11 |
| 0.0035 | 0.0005 | 2x 106 | 64.6 | 3.52 | 0.10 | 3.42 | 0.10 | 3.33 | 0.09 | 3.30 | 0.09 |
| 0.0035 | 0.0005 | 1x 2113 | 48.8 | 3.93 | 0.13 | 3.83 | 0.13 | 3.73 | 0.12 | 3.69 | 0.12 |
| 0.0040 | 0.0005 | 1x 1080 1x 106 | 56.9 | 3.72 | 0.10 | 3.62 | 0.10 | 3.53 | 0.10 | 3.49 | 0.09 |
| 0.0040 | 0.0005 | 1x 2113 | 53.8 | 3.80 | 0.10 | 3.70 | 0.10 | 3.61 | 0.10 | 3.57 | 0.10 |
| 0.0042 | 0.0005 | 1x 1080 1x 106 | 58.6 | 3.68 | 0.09 | 3.58 | 0.09 | 3.49 | 0.09 | 3.45 | 0.09 |
| 0.0045 | 0.0005 | 2x 1080 | 51.4 | 3.86 | 0.10 | 3.76 | 0.10 | 3.66 | 0.09 | 3.63 | 0.09 |
| 0.0045 | 0.0005 | 1x 1080 1x 106 | 60.8 | 3.62 | 0.08 | 3.52 | 0.08 | 3.43 | 0.08 | 3.40 | 0.08 |
| 0.0047 | 0.0005 | 1x 1080 1x 1080 | 53.0 | 3.82 | 0.09 | 3.72 | 0.09 | 3.62 | 0.09 | 3.59 | 0.09 |
| 0.0050 | 0.00075 | 1x 1080 1x 1080 | 55.2 | 3.77 | 0.12 | 3.67 | 0.12 | 3.57 | 0.12 | 3.54 | 0.12 |
| 0.0050 | 0.00075 | 1x 2116 | 51.0 | 3.87 | 0.13 | 3.77 | 0.13 | 3.67 | 0.13 | 3.64 | 0.12 |
| 0.0050 | 0.00075 | 1x 2113 1x 106 | 52.0 | 3.85 | 0.13 | 3.75 | 0.13 | 3.65 | 0.12 | 3.62 | 0.12 |
| 0.0051 | 0.00075 | 1x 1080 1x 1080 | 55.9 | 3.75 | 0.12 | 3.65 | 0.12 | 3.55 | 0.11 | 3.52 | 0.11 |
| 0.0053 | 0.00075 | 2x 1080 | 57.2 | 3.72 | 0.11 | 3.61 | 0.11 | 3.52 | 0.11 | 3.49 | 0.11 |
| 0.0055 | 0.00075 | 2x 1080 | 58.4 | 3.68 | 0.10 | 3.58 | 0.10 | 3.49 | 0.10 | 3.46 | 0.10 |
| 0.0060 | 0.00075 | 2x 2113 | 42.7 | 4.09 | 0.12 | 3.99 | 0.12 | 3.88 | 0.12 | 3.84 | 0.12 |
| 0.0060 | 0.00075 | 1x 1652 | 47.5 | 3.96 | 0.11 | 3.86 | 0.11 | 3.76 | 0.11 | 3.72 | 0.11 |
| 0.0060 | 0.00075 | 1x 2116 1x 106 | 50.0 | 3.90 | 0.11 | 3.80 | 0.11 | 3.70 | 0.11 | 3.66 | 0.11 |
| 0.0060 | 0.00075 | 1x 1080 1x 2113 | 51.4 | 3.86 | 0.11 | 3.76 | 0.11 | 3.66 | 0.11 | 3.63 | 0.10 |
| 0.0060 | 0.00075 | 1x 106 1x 2116 | 50.0 | 3.90 | 0.11 | 3.80 | 0.11 | 3.70 | 0.11 | 3.66 | 0.11 |
| 0.0070 | 0.001 | 2x 2113 | 48.8 | 3.93 | 0.13 | 3.83 | 0.13 | 3.73 | 0.12 | 3.69 | 0.12 |
| 0.0075 | 0.001 | 1x 7628 | 41.0 | 4.13 | 0.13 | 4.03 | 0.13 | 3.93 | 0.13 | 3.89 | 0.13 |
| 0.0080 | 0.001 | 2x 2116 | 42.3 | 4.10 | 0.12 | 4.00 | 0.12 | 3.89 | 0.12 | 3.85 | 0.12 |
| 0.0080 | 0.001 | 1x 2116 1x 2113 | 47.8 | 3.96 | 0.11 | 3.86 | 0.11 | 3.75 | 0.11 | 3.72 | 0.11 |
| 0.0090 | 0.001 | 1x 2116 1x 2116 | 47.0 | 3.98 | 0.10 | 3.88 | 0.10 | 3.77 | 0.10 | 3.74 | 0.10 |
| 0.0095 | 0.001 | 1x 2116 1x 2116 | 49.1 | 3.92 | 0.10 | 3.82 | 0.10 | 3.72 | 0.09 | 3.69 | 0.09 |
| 0.0100 | 0.001 | 2x 2116 | 51.0 | 3.87 | 0.09 | 3.77 | 0.09 | 3.67 | 0.09 | 3.64 | 0.08 |
| 0.0100 | 0.001 | 1x 7628 1x 1080 | 44.3 | 4.05 | 0.10 | 3.95 | 0.10 | 3.84 | 0.09 | 3.80 | 0.09 |

Data Source:
Park Nelco

# Epoxy Glass Laminate Properties N4000-13 SI

Enabling Technologies

Low loss epoxy resin system & low loss/dielectric constant SI glass

| Thickness | Tolerance | Construction | RC% | Dielectric Constant 1MHz | Tol. | 1GHz | Tol. | 2.5 GHz | Tol. | 10 GHz | Tol. |
|---|---|---|---|---|---|---|---|---|---|---|---|
| 0.0020 | 0.0005 | 1x 106 | 67.8 | 3.39 | 0.05 | 3.19 | 0.08 | 3.15 | 0.02 | 3.14 | 0.02 |
| 0.0025 | 0.0005 | 1x 1080 | 54.1 | 3.51 | 0.06 | 3.41 | 0.10 | 3.21 | 0.03 | 3.19 | 0.02 |
| 0.0027 | 0.0005 | 1x 1080 | 56.9 | 3.49 | 0.05 | 3.36 | 0.09 | 3.20 | 0.02 | 3.18 | 0.02 |
| 0.0030 | 0.0005 | 1x 1080 | 64.4 | 3.45 | 0.04 | 3.30 | 0.07 | 3.18 | 0.02 | 3.17 | 0.02 |
| 0.0040 | 0.0005 | 2x 106 | 67.8 | 3.39 | 0.03 | 3.19 | 0.04 | 3.15 | 0.01 | 3.14 | 0.01 |
| 0.0040 | 0.0005 | 1x 2116 | 40.5 | 3.68 | 0.07 | 3.68 | 0.11 | 3.26 | 0.02 | 3.25 | 0.02 |
| 0.0050 | 0.00075 | 2x 1080 | 54.1 | 3.51 | 0.05 | 3.41 | 0.08 | 3.21 | 0.02 | 3.19 | 0.02 |
| 0.0050 | 0.00075 | 1x 2116 | 49.7 | 3.56 | 0.06 | 3.49 | 0.09 | 3.22 | 0.02 | 3.21 | 0.02 |
| 0.0060 | 0.00075 | 2x 1080 | 60.4 | 3.45 | 0.03 | 3.30 | 0.06 | 3.18 | 0.01 | 3.17 | 0.01 |
| 0.0070 | 0.0015 | 2x 1080 1x 106 | 57.8 | 3.48 | 0.06 | 3.34 | 0.10 | 3.19 | 0.03 | 3.18 | 0.02 |
| 0.0080 | 0.001 | 2x 2116 | 40.5 | 3.68 | 0.07 | 3.68 | 0.11 | 3.26 | 0.02 | 3.25 | 0.02 |
| 0.0090 | 0.001 | 1x 2116 1x 2116 | 45.5 | 3.61 | 0.05 | 3.57 | 0.08 | 3.24 | 0.02 | 3.23 | 0.02 |
| 0.0090 | 0.001 | 2x 1080 1x 1080 | 60.4 | 3.45 | 0.03 | 3.30 | 0.05 | 3.18 | 0.01 | 3.17 | 0.01 |
| 0.0100 | 0.001 | 2x 2116 | 49.7 | 3.56 | 0.04 | 3.49 | 0.07 | 3.22 | 0.01 | 3.21 | 0.01 |
| 0.0100 | 0.001 | 2x 2116 1x 106 | 45.3 | 3.61 | 0.05 | 3.57 | 0.08 | 3.24 | 0.02 | 3.23 | 0.01 |
| 0.0120 | 0.001 | 2x 2116 1x 2116 | 40.5 | 3.68 | 0.05 | 3.68 | 0.08 | 3.26 | 0.01 | 3.25 | 0.01 |
| 0.0140 | 0.0015 | 2x 2116 1x 2116 | 47.0 | 3.59 | 0.05 | 3.54 | 0.08 | 3.24 | 0.02 | 3.22 | 0.01 |
| 0.0150 | 0.0015 | 2x 2116 1x 2116 | 49.7 | 3.56 | 0.04 | 3.49 | 0.07 | 3.22 | 0.01 | 3.21 | 0.01 |
| 0.0160 | 0.0015 | 2x 2116 2x 2116 | 40.5 | 3.68 | 0.05 | 3.68 | 0.09 | 3.26 | 0.02 | 3.25 | 0.01 |
| 0.0180 | 0.0015 | 2x 2116 2x 2116 | 45.5 | 3.61 | 0.04 | 3.57 | 0.07 | 3.24 | 0.01 | 3.23 | 0.01 |
| 0.0200 | 0.002 | 2x 2116 2x 2116 | 49.7 | 3.56 | 0.04 | 3.49 | 0.07 | 3.22 | 0.01 | 3.21 | 0.01 |
| 0.0210 | 0.002 | 2x 2116 2x 2116 1x | 49.4 | 3.56 | 0.04 | 3.49 | 0.06 | 3.23 | 0.01 | 3.21 | 0.01 |
| 0.0240 | 0.002 | 2x 2116 4x 2116 | 40.5 | 3.68 | 0.05 | 3.68 | 0.08 | 3.26 | 0.01 | 3.25 | 0.01 |
| 0.0280 | 0.002 | 4x 2116 2x 2116 | 47.0 | 3.59 | 0.03 | 3.54 | 0.05 | 3.24 | 0.01 | 3.22 | 0.01 |
| 0.0310 | 0.002 | 2x 2116 4x 2116 | 51.0 | 3.55 | 0.04 | 3.46 | 0.06 | 3.22 | 0.01 | 3.21 | 0.01 |

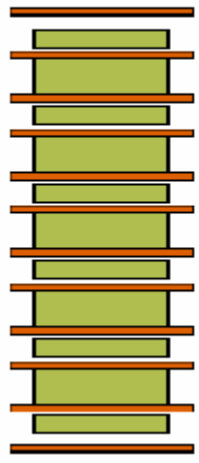
Data Source: Park Nelco

# Dynamic Details, Inc.

## Controlled Material Stack-up

Enabling Technologies

| Impedance Requirements: L# | Impedance Type | Orig Line | Fin. Line | Ref Pln | 2nd Ref Pln | Z ohms +/- | Diff Line Centers | Coplanar Spacing |
|---|---|---|---|---|---|---|---|---|
| 1 | SE-Coated Microstrip | .00475 | .00475 | 2 | | 50.0 +/- 10% | | |
| 4 | DIF-Dual Stripline Edg Cpld | .00400 | .00325 | 3 | 6 | 100.0 +/- 10% | .00800 | |
| 4 | SE-Dual Stripline | .00400 | .00450 | 3 | 6 | 50.0 +/- 10% | | |
| 5 | DIF-Dual Stripline Edg Cpld | .00400 | .00325 | 3 | 6 | 100.0 +/- 10% | .00800 | |
| 5 | SE-Dual Stripline | .00400 | .00450 | 3 | 6 | 50.0 +/- 10% | | |
| 8 | DIF-Dual Stripline Edg Cpld | .00400 | .00325 | 7 | 10 | 100.0 +/- 10% | .00800 | |
| 8 | SE-Dual Stripline | .00400 | .00450 | 7 | 10 | 50.0 +/- 10% | | |
| 9 | DIF-Dual Stripline Edg Cpld | .00400 | .00325 | 7 | 10 | 100.0 +/- 10% | .00800 | |
| 9 | SE-Dual Stripline | .00400 | .00450 | 7 | 10 | 50.0 +/- 10% | | |
| 12 | SE-Coated Microstrip | .00500 | .00475 | 11 | | 50.0 +/- 10% | | |



| Lamination Stackup: L#/Type | Description: | Thickness and Tolerances: Cu: | Laminate/PrePreg: | Base Material Rqmts: Type: | Description: | Dk | Scaling X | Y | Type/L# |
|---|---|---|---|---|---|---|---|---|---|
| 1 Sig | Foil ( H oz ) | .00060 | | | | | .00 | .00 | Sig 1 |
| | Pre-Preg ( 1 x 1080 ) | | .0030 +/- 0.0003 | Standard | FR4 Hi-Temp | 3.81 | | | |
| 2 Pln | Core 0.0020 1/1 | .00120 | .0020 | Matsu ZBC | ZBC | | .42 | .34 | Pln 2 |
| 3 Pln | | .00120 | | | | 3.8 | .42 | .34 | Pln 3 |
| | Pre-Preg ( 1 x 2113 ) | | .0030 +/- 0.0003 | Standard | FR4 Hi-Temp | 4.35 | | | |
| 4 Mix | Core 0.0280 H/H | .00060 | .0280 | Standard | FR4 Hi-Temp | | .00 | .00 | Mix 4 |
| 5 Mix | | .00060 | | | | 4.4 | .00 | .00 | Mix 5 |
| | Pre-Preg ( 1 x 2113 ) | | .0030 +/- 0.0003 | Standard | FR4 Hi-Temp | 4.35 | | | |
| 6 Pln | Core 0.0020 1/1 | .00120 | .0020 | Matsu ZBC | ZBC | | .42 | .34 | Pln 6 |
| 7 Pln | | .00120 | | | | 3.8 | .42 | .34 | Pln 7 |
| | Pre-Preg ( 1 x 2113 ) | | .0030 +/- 0.0003 | Standard | FR4 Hi-Temp | 4.35 | | | |
| 8 Mix | Core 0.0280 H/H | .00060 | .0280 | Standard | FR4 Hi-Temp | | .00 | .00 | Mix 8 |
| 9 Mix | | .00060 | | | | 4.4 | .00 | .00 | Mix 9 |
| | Pre-Preg ( 1 x 2113 ) | | .0030 +/- 0.0003 | Standard | FR4 Hi-Temp | 4.35 | | | |
| 10 Pln | Core 0.0020 1/1 | .00120 | .0020 | Matsu ZBC | ZBC | | .42 | .34 | Pln 10 |
| 11 Pln | | .00120 | | | | 3.8 | .42 | .34 | Pln 11 |
| | Pre-Preg ( 1 x 1080 ) | | .0030 +/- 0.0003 | Standard | FR4 Hi-Temp | 3.81 | | | |
| 12 Sig | Foil ( H oz ) | .00060 | | | | | .00 | .00 | Sig 12 |

# Dynamic Details, Inc.

Enabling Technologies

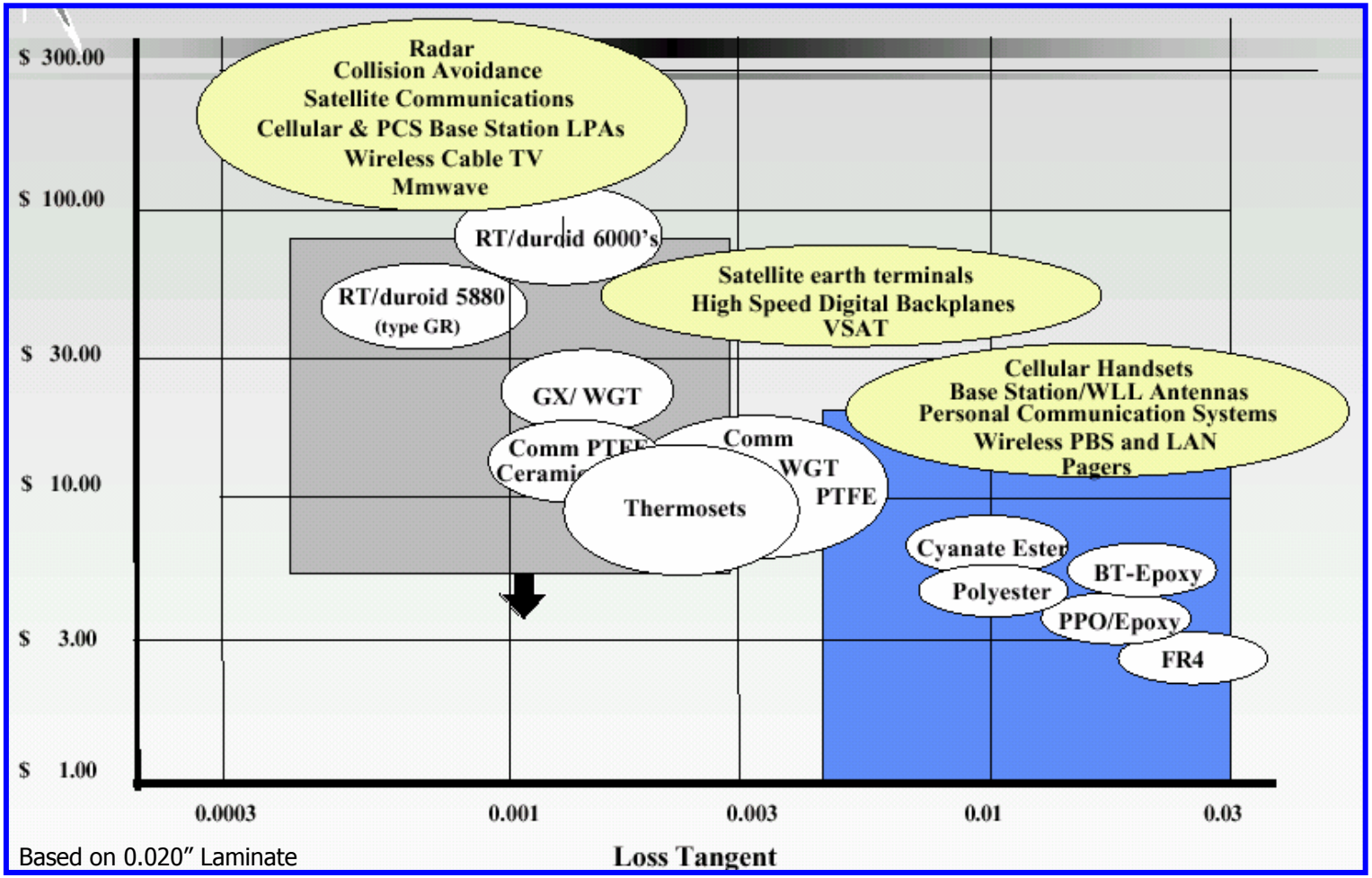
## Overview

- Technology Drivers
- Advanced Materials
- Characterized FR-4
- Hybrid Constructions
- Laser Direct Imaging
- High Aspect Ratio Copper Plating
- Laser Drilling
- Planar Via Technologies

# Dynamic Details, Inc.

## Advanced Low Loss Dielectric Laminates

### Relative Laminate Cost Per Square Foot vs Loss Tangent



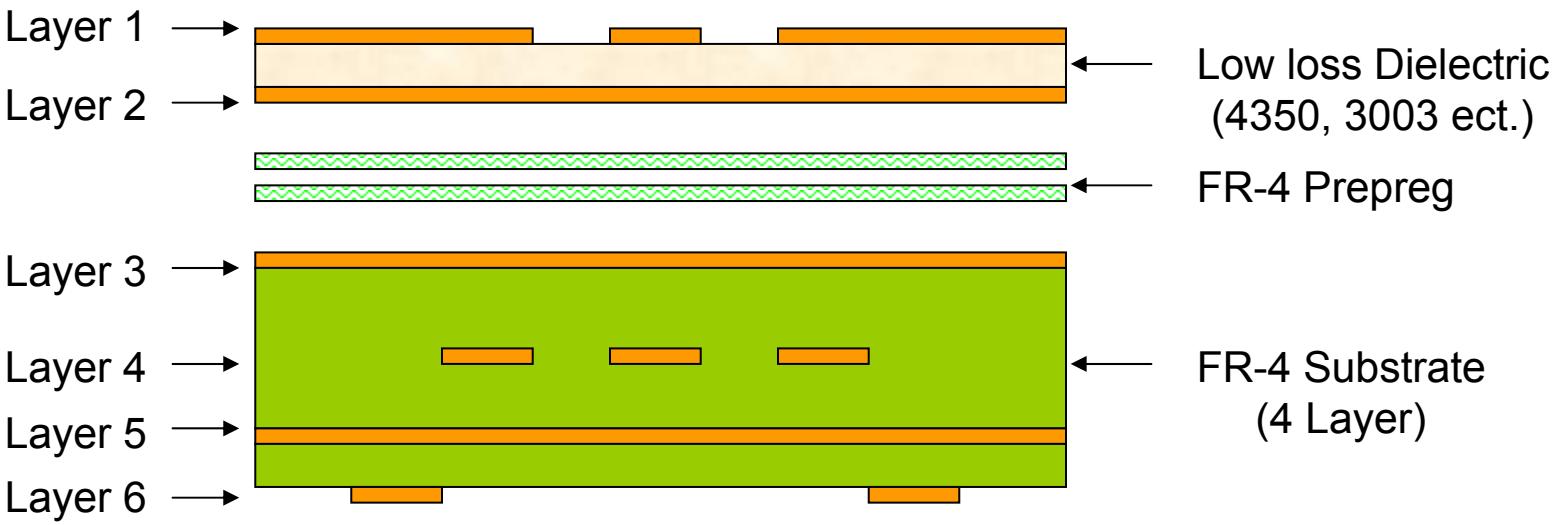

Based on 0.020" Laminate

Source: Rogers

# Mixed Dielectric Substrates



- Mixed dielectric constructions reduce cost by only using more expensive low loss materials where needed
- FR-4 Epoxy-Glass Sub-Cores provide structural support when using PTFE based laminates

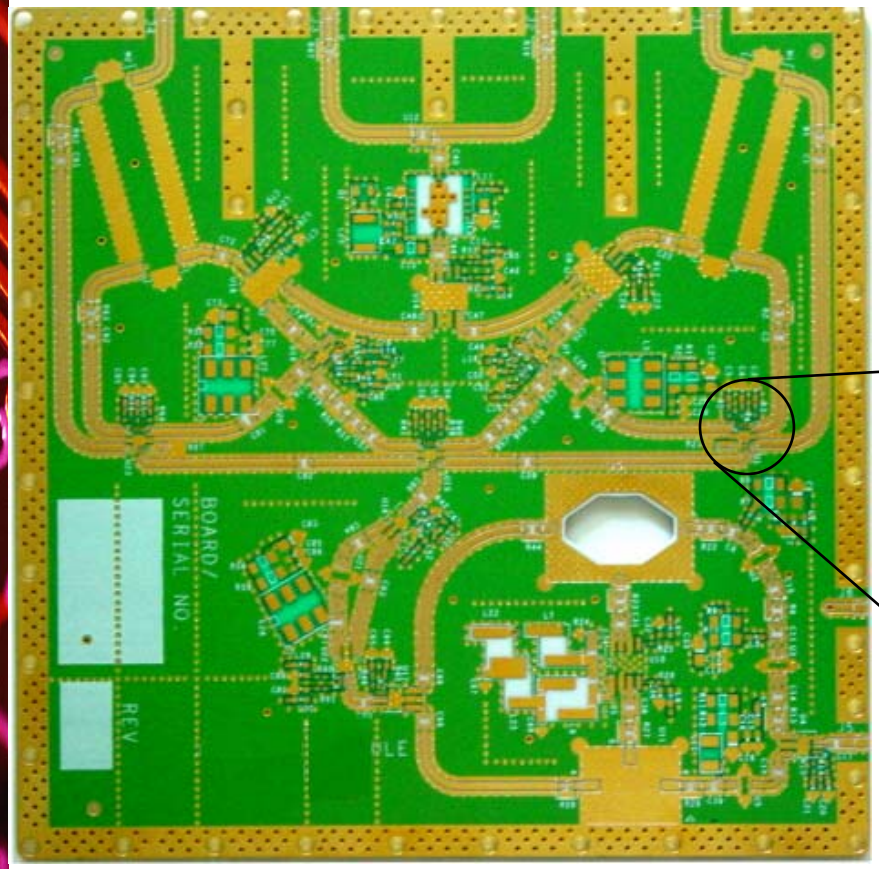



Typical mixed dielectric construction with low loss cap layer

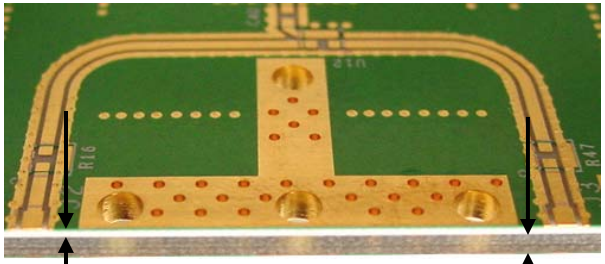
# Dynamic Details, Inc.

## Mixed Dielectric Circuit Constructions

Mixed Dielectric: Rogers 4350/FR-4

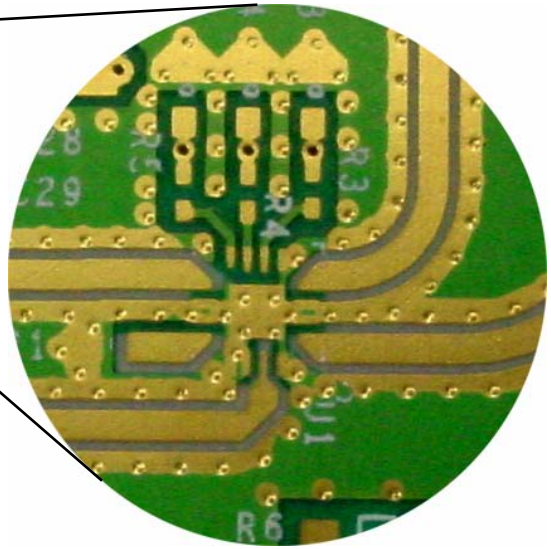



Cross-Section



Roger 4350

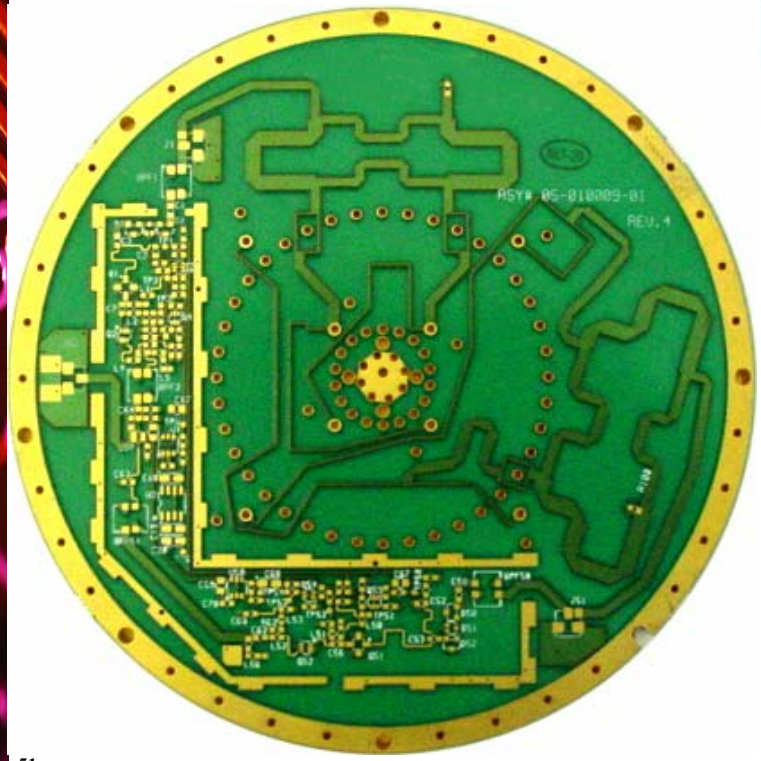
FR-4



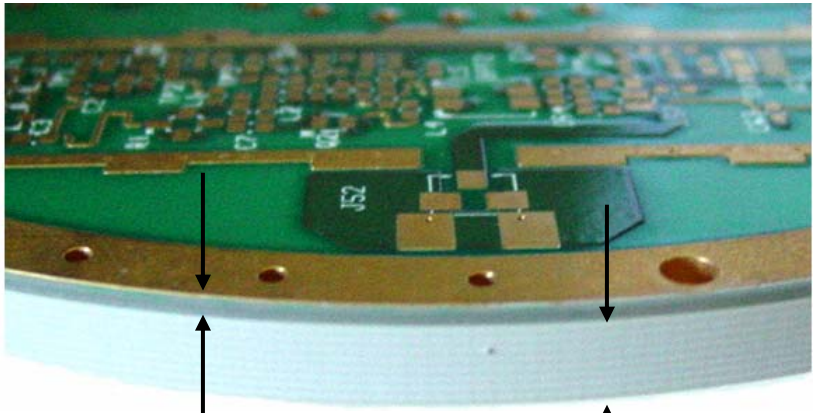
# Dynamic Details, Inc.

## Mixed Dielectric Circuit Constructions

Mixed Dielectric:
Rogers 4350/Rogers TMM 6



Cross-Section



Roger 4350
0.040” Thick

Rogers TMM 6
0.200” Thick

# Conduction Cooled Circuit Constructions



## PWB Thermal Path Considerations:

- Conduction cooling allows heat to be removed through the PWB

- Conduction cooling with integral core constructions provide thermal paths in one or more of the following ways:

  - Provide heat spreading through the core using the PWB as a radiating surface

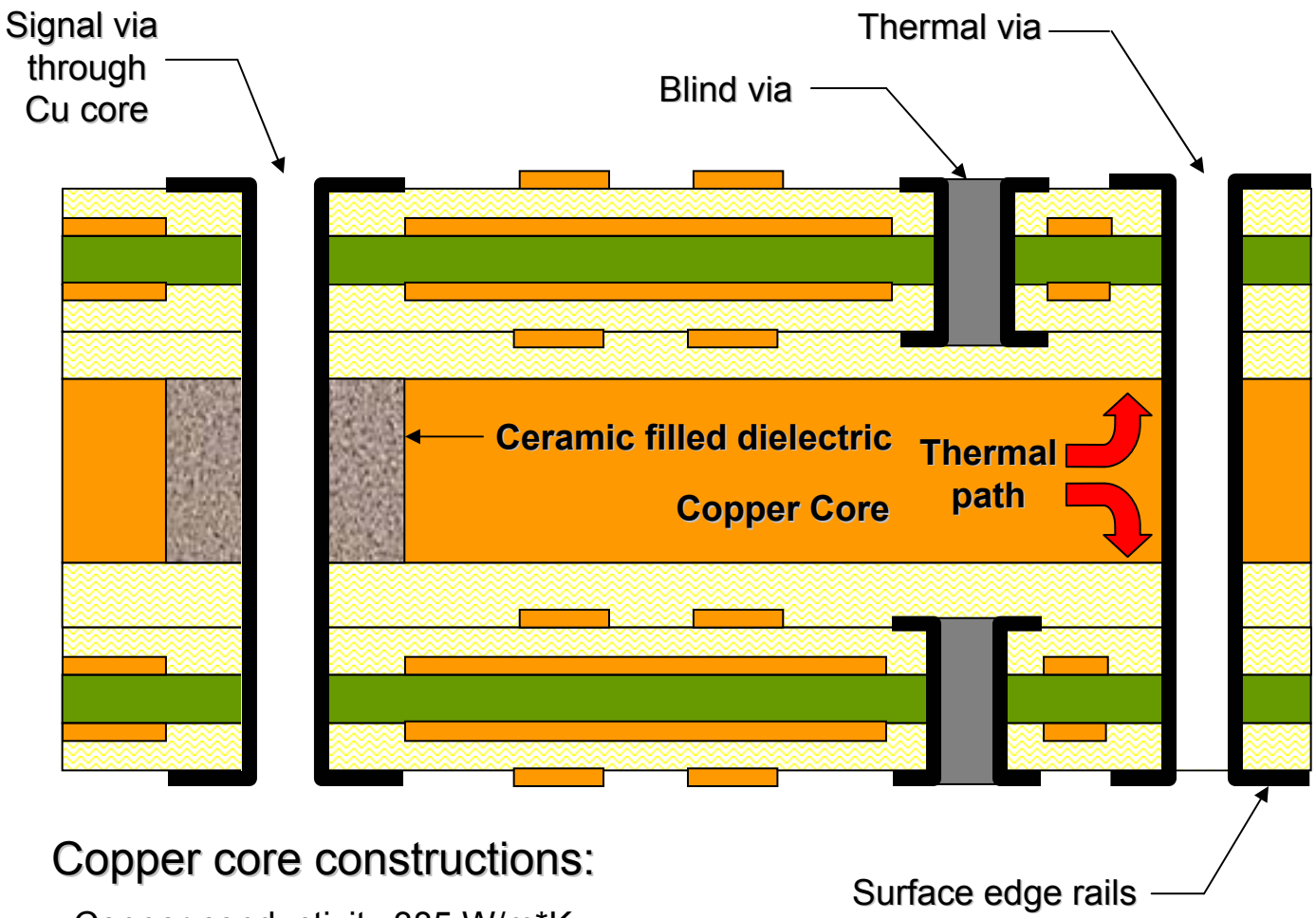
  - Using thermal via's a conducting path can be established from components to the core

  - Heat can be conducted to the edge of the card and be removed by exposing the core and connecting to an external heat sink

  - Thermal vias can be used to establish a thermal connection from the core to surface edge rails and connect to an external heat sink

# Conduction Cooled Circuit Constructions



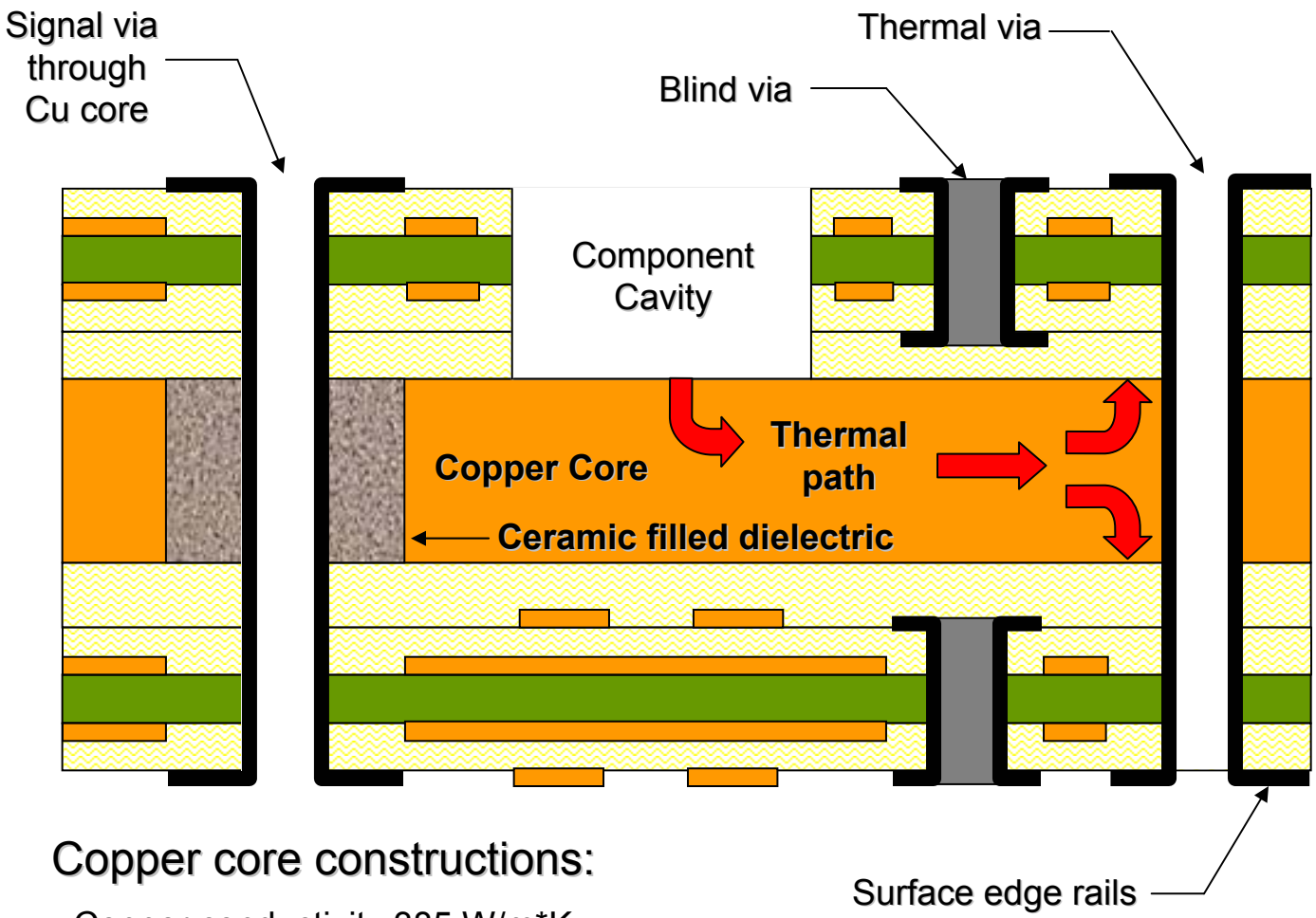



## Copper core constructions:

- Copper conductivity 385 W/m*K
- Copper core CTE 17 ppm/C
- Epoxy laminate conductivity 0.3 W/m*K

# Conduction Cooled Circuit Constructions



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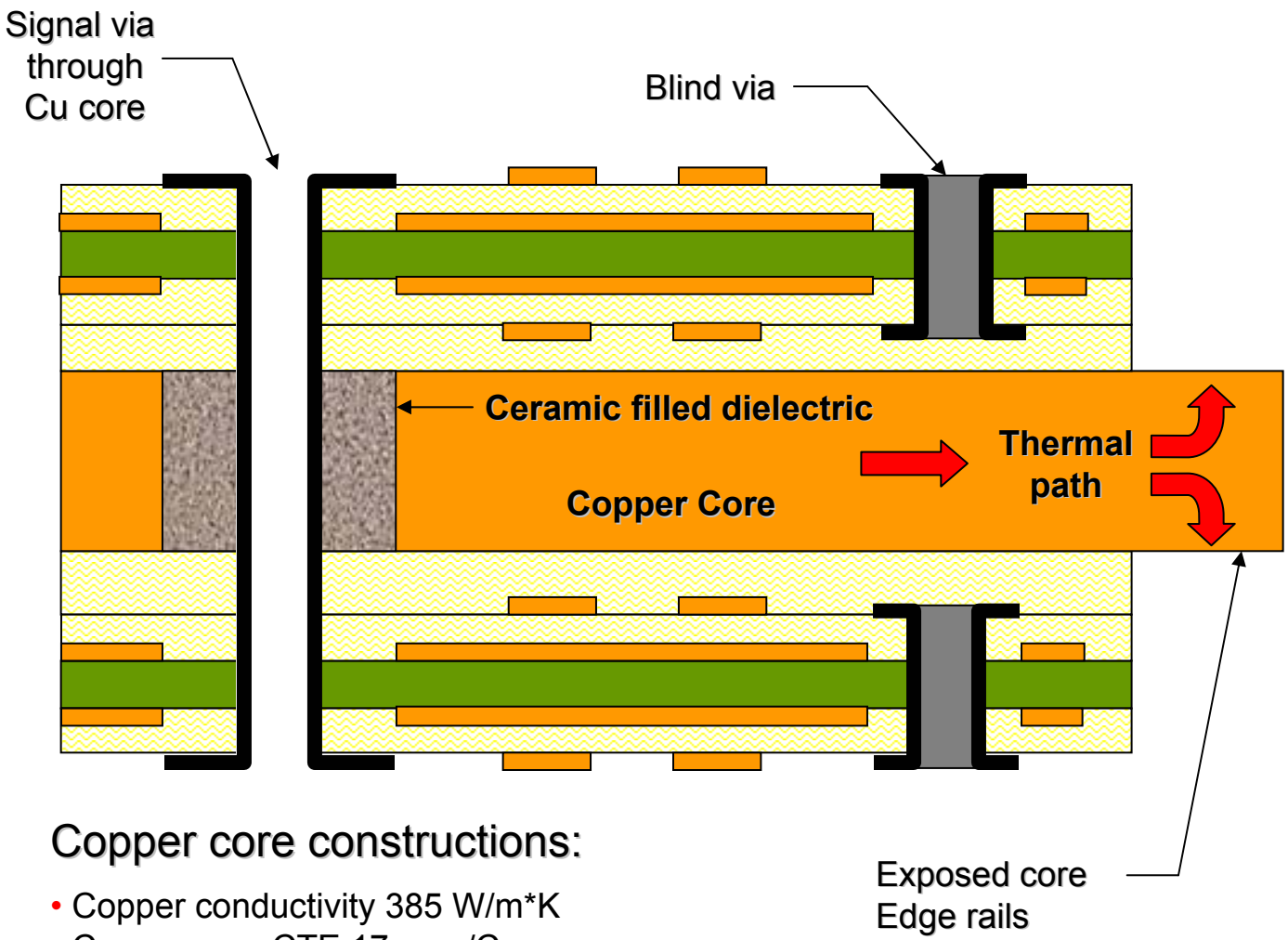


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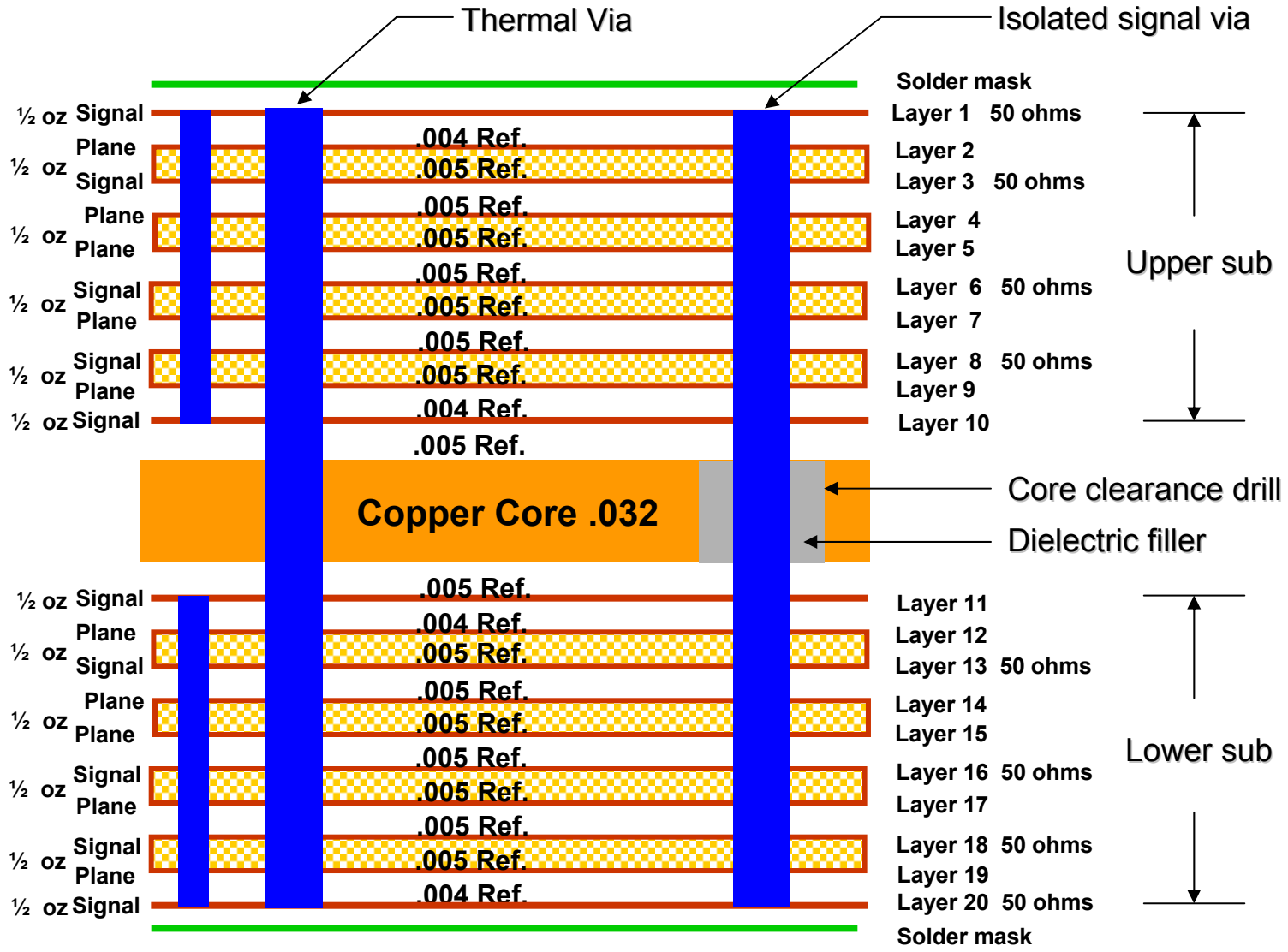
# Conduction Cooled Circuit Constructions

Enabling Technologies



# Conduction Cooled Circuit Constructions



## Thermal Mechanical Properties of Core Materials

| Raw Material | Thermal Conductivity (W/m*K) | CTE (ppm/C) | Density (g/cm3) | Tensile Modulus (msi) | Dielectric Constant (er) |
|---|---|---|---|---|---|
| ST 1000 | 1000.0 | -1.15 | 2.20 | 135.0 | 13.36 |
| ST 600 | 620.0 | -1.15 | 2.20 | 130.0 | 13.36 |
| ST 325 | 325.0 | -1.15 | 2.20 | 114.0 | 13.36 |
| ST 100 | 100.0 | -1.10 | 2.20 | 62.0 | 13.36 |
| ST 10 | 10.0 | -0.60 | 1.76 | 33.5 | In Development |
| FR4 | 0.3 | 17.00 | 1.20 | 0.3 | 4.50 |
| Polyimide | 0.7 | 14.00 | 1.42 | 0.3 | 4.00 |
| Copper | 385.0 | 17.00 | 8.92 | 17.0 | N/A |
| Aluminum | 280.0 | 24.00 | 2.70 | 4.7 | N/A |
| CIC | 108.0 | 4.00 | 9.90 | 19.0 | N/A |

Stabl ox val ues represents data of raw fibers

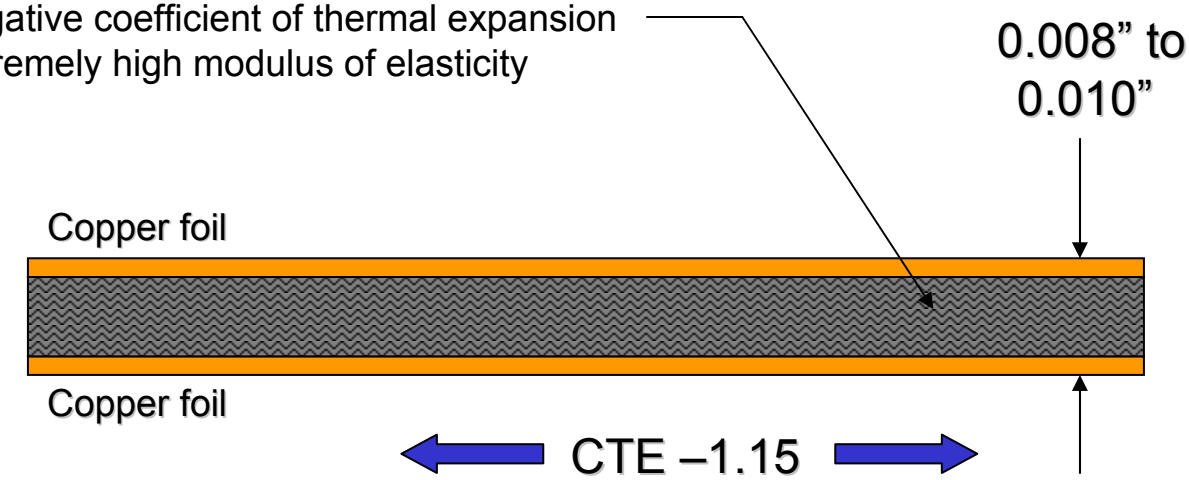
Data Source: Thermal Works

# Low CTE High Conductivity StablCor™ Laminate



## Standard weave pitch based carbon fiber fabric

- High thermal conductivity
- Negative coefficient of thermal expansion
- Extremely high modulus of elasticity

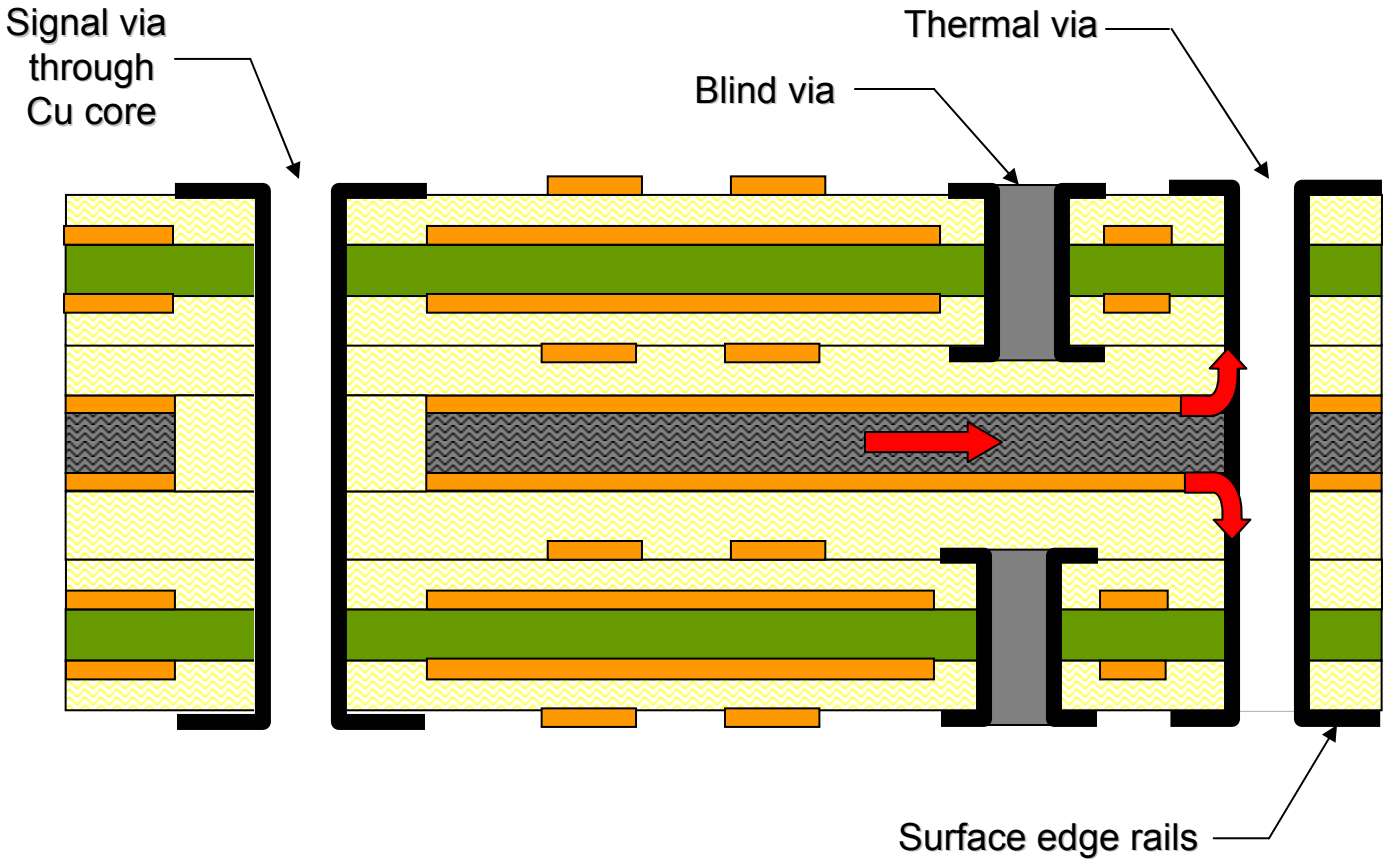



## Design Considerations:

- Carbon fiber fabric is electrically conductive
- Both copper planes must be treated as the same potential
- Split planes are made by mechanically routing resulting in loss of thermal path
- Laminate must be pre-drilled to provide electrical clearance
- Optimum designs, dielectric thickness should not exceed 0.015" from the top of core
- CTE will be based on volume metric ratio of StableCor and Copper/Dielectric materials

# Low CTE Conduction Cooled Circuit Constructions





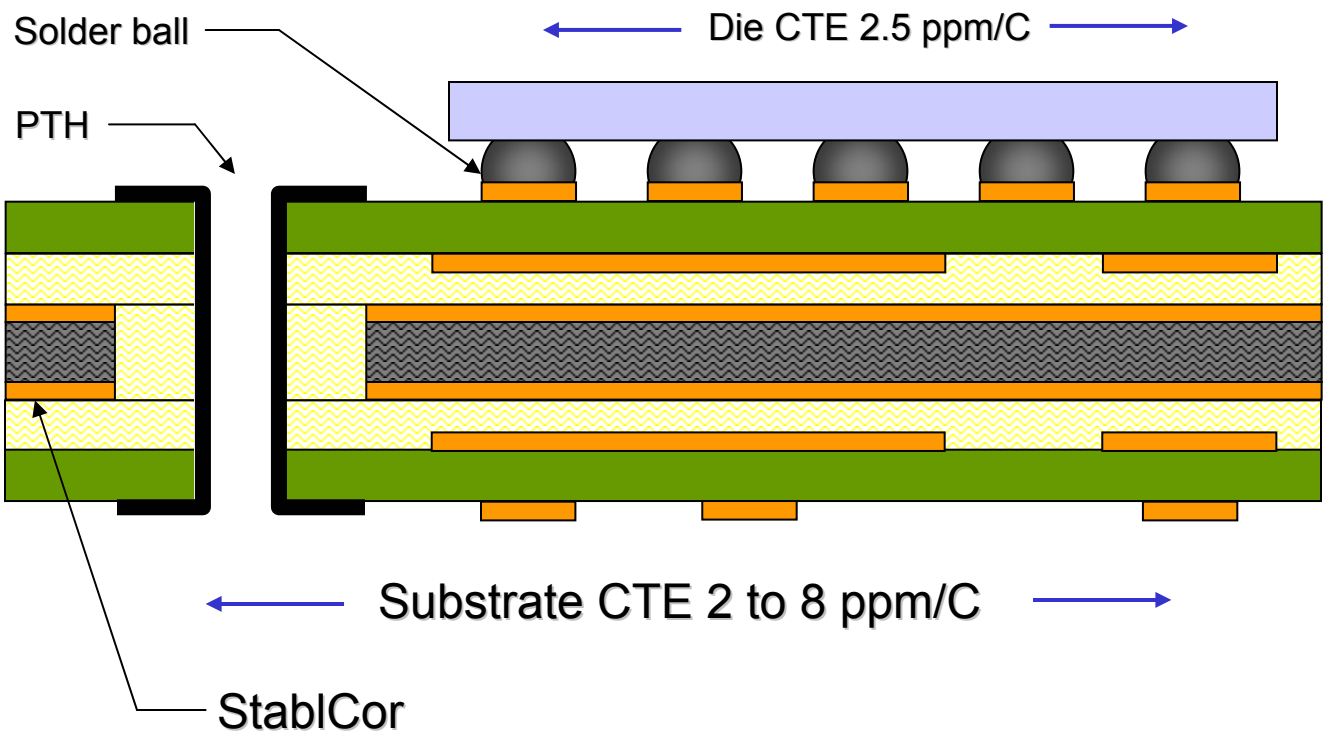

## StablCor Constructions:

- StablCor conductivity 10-1000 W/m*K
- StablCor CTE –1.15 ppm/C
- Epoxy laminate conductivity 0.3 W/m*K

# Low CTE Conduction Cooled Circuit Constructions



## Flip Chip applications

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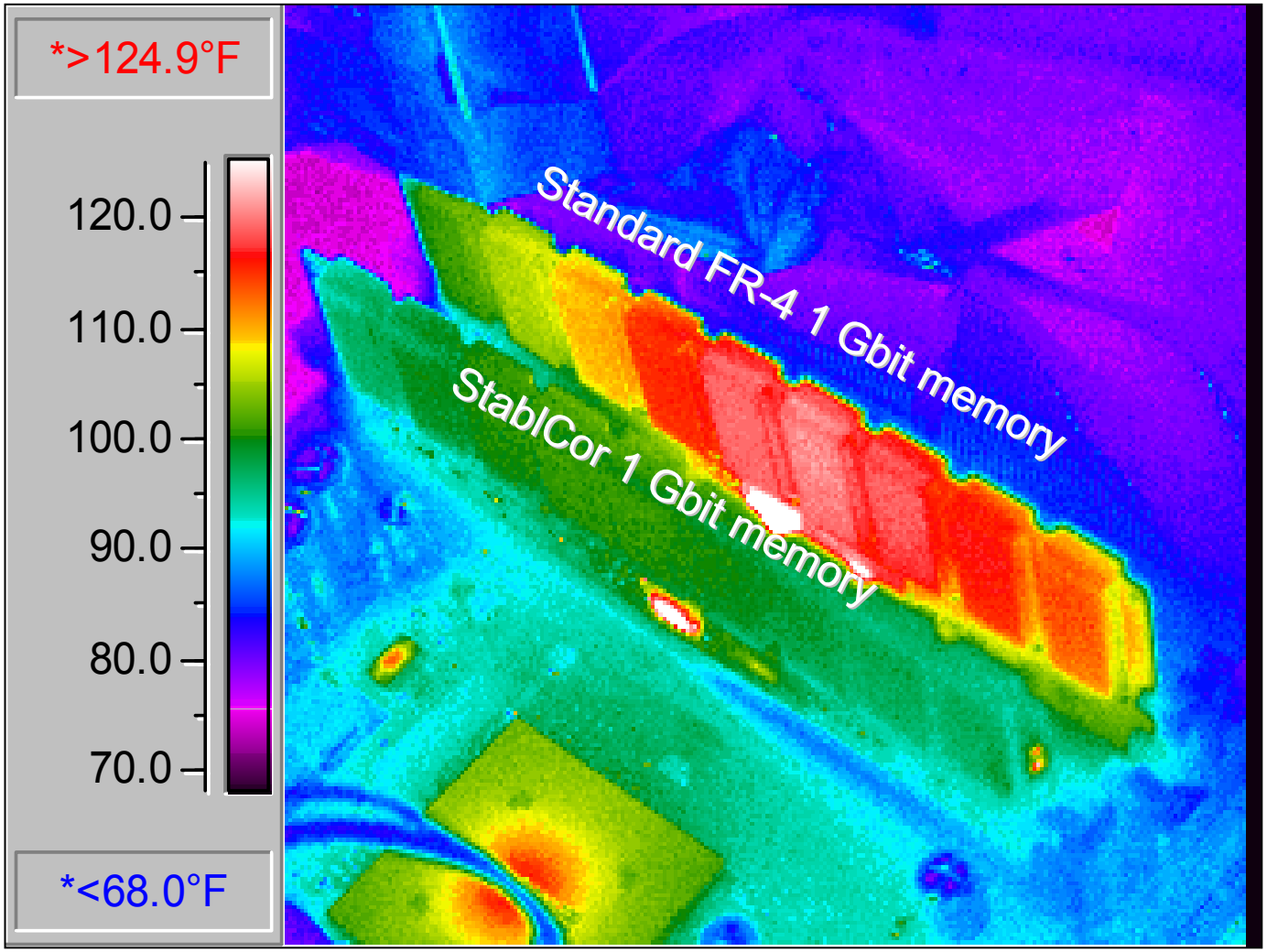
# Low CTE Conduction Cooled Circuit Constructions

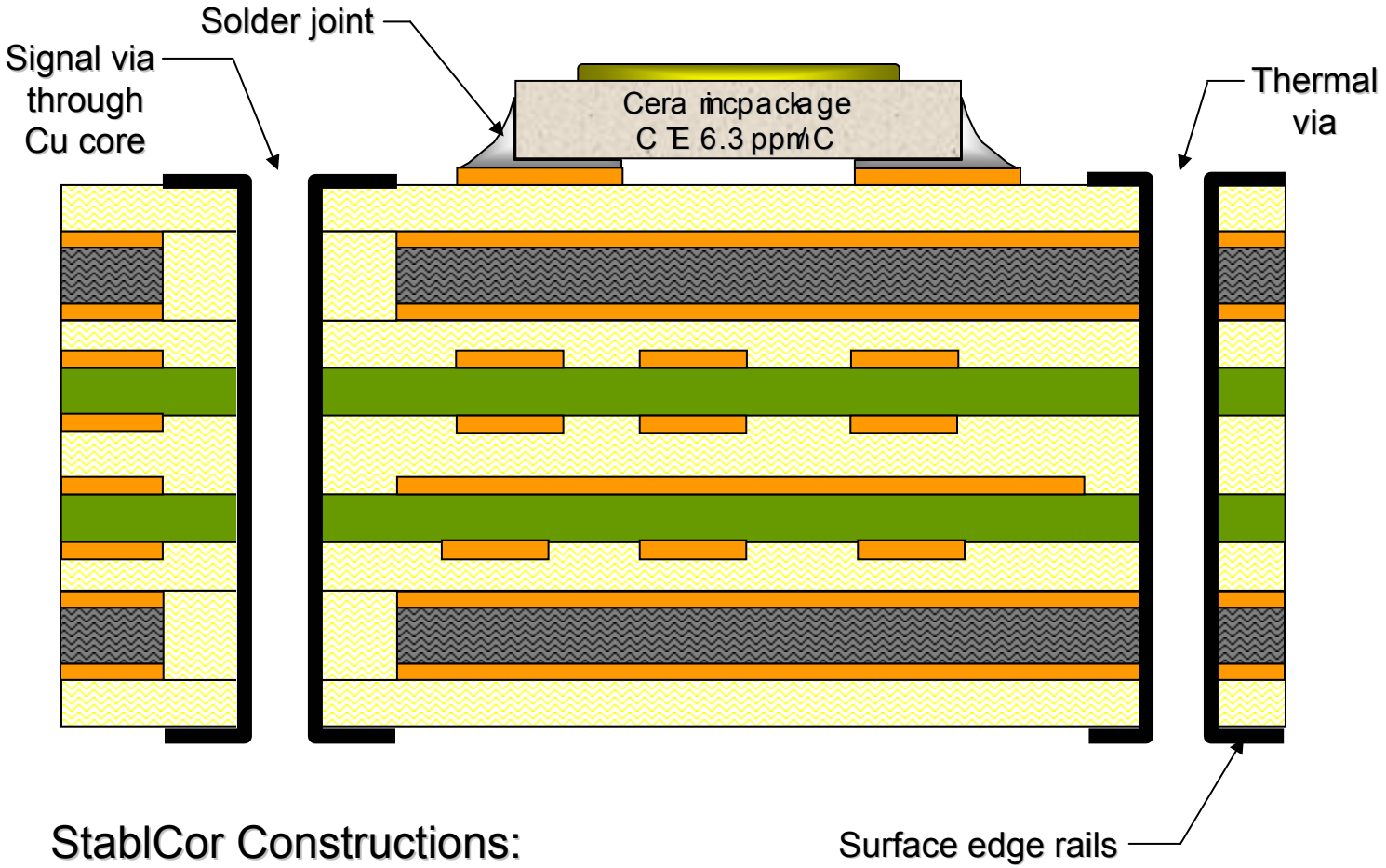
Enabling Technologies




Graphic Source: Thermal Works

# Low CTE Conduction Cooled Circuit Constructions



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# Dynamic Details, Inc.

Enabling Technologies

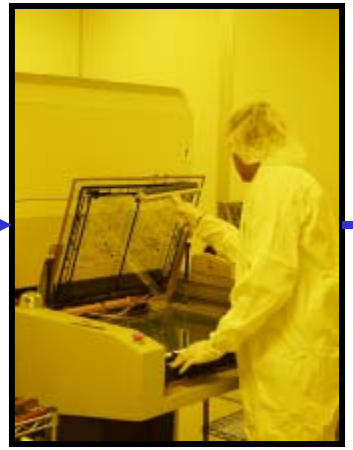
## Overview

- Technology Drivers
- Advanced Materials
- Characterized FR-4
- Hybrid Constructions
- Laser Direct Imaging
- High Aspect Ratio Copper Plating
- Laser Drilling
- Planar Via Technologies

# Dynamic Details, Inc.

## Conventional Photo Printing Process

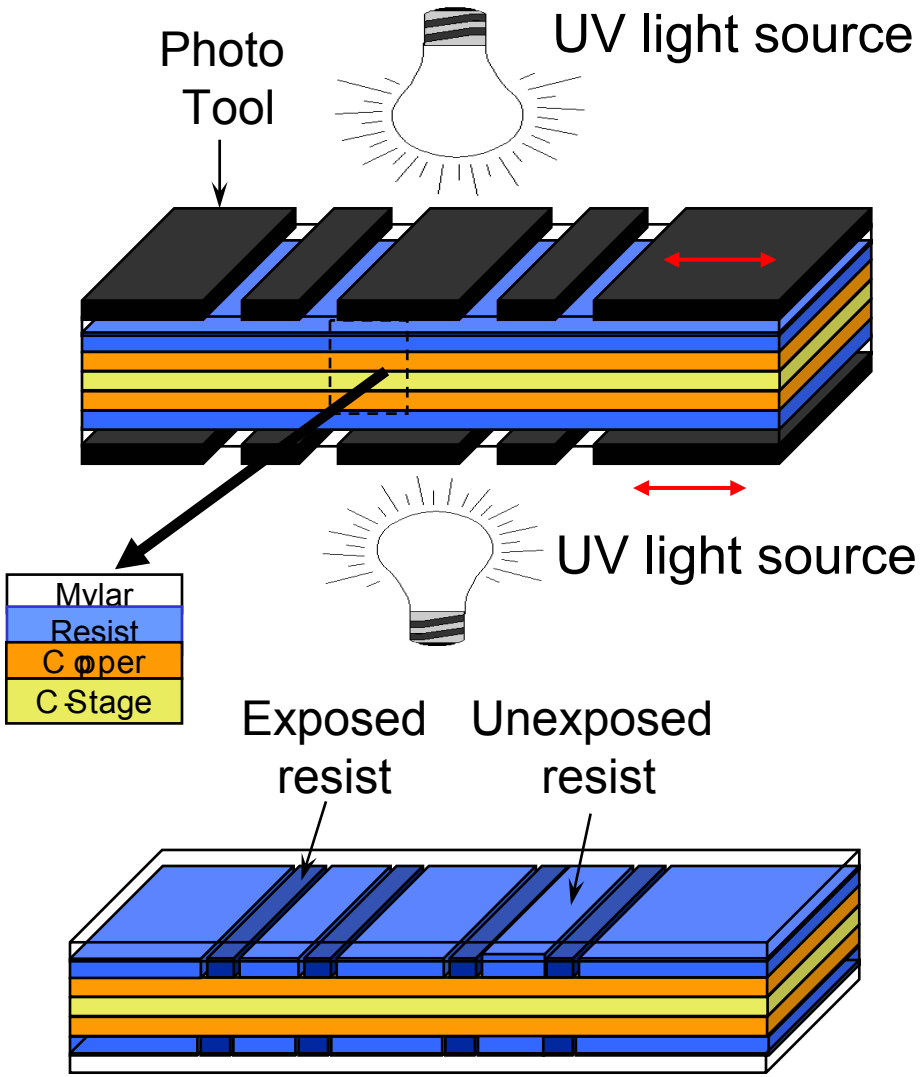
Laser plot Mylar photo tools



Expose circuit image using Mylar photo tools

# Conventional Photo Printing Process



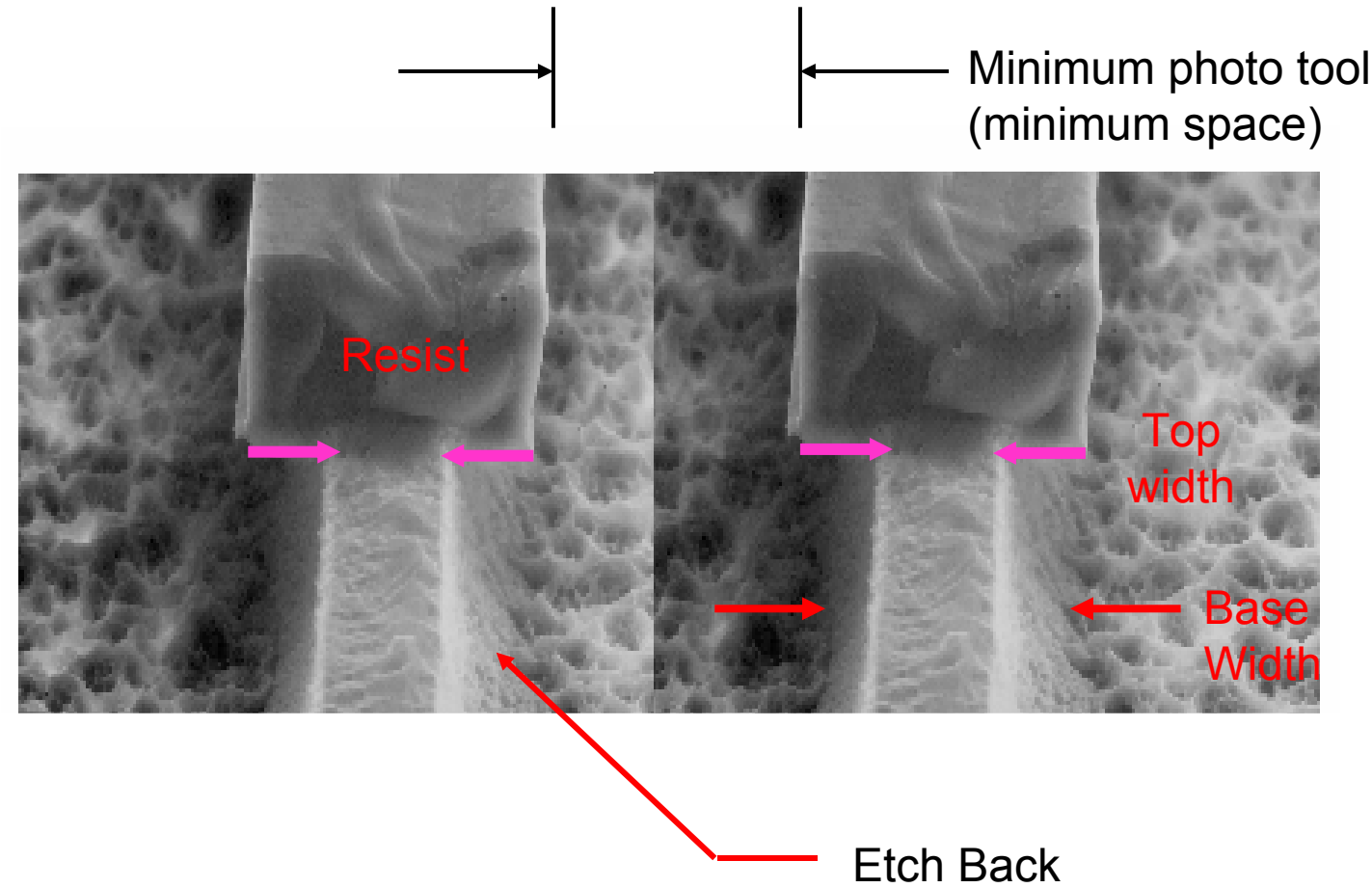



## Engineering Considerations

- Alignment of upper and lower tools
- Alignment of tools to substrate
- Scaling of photo tools
- Geometric compensation
- Temperature stability of tools while photo printing

# Conventional Photo Printing Process






The minimum photo tool opening is limited by the ability to fully remove un-exposed resist in the narrow gap between traces

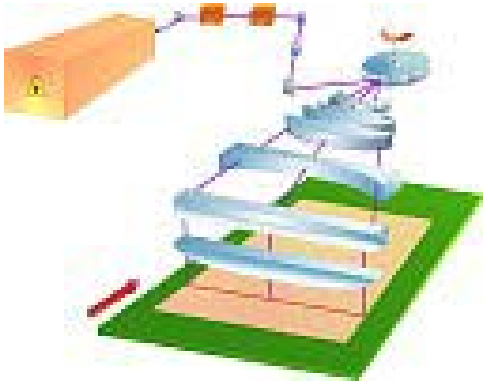
# Dynamic Details, Inc.

## Laser Direct Imaging (LDI)

Orbotech DP-100

Elimination of Photo Tools

- No Film/Artwork Movement
- Quick Turn Made Easy
  - Run product as soon as Engineering releases data to the floor
- Reduction in Defect Count.
  - Direct Write = No Film related defects
  - No issues related to loss of vacuum



Scanning Optics

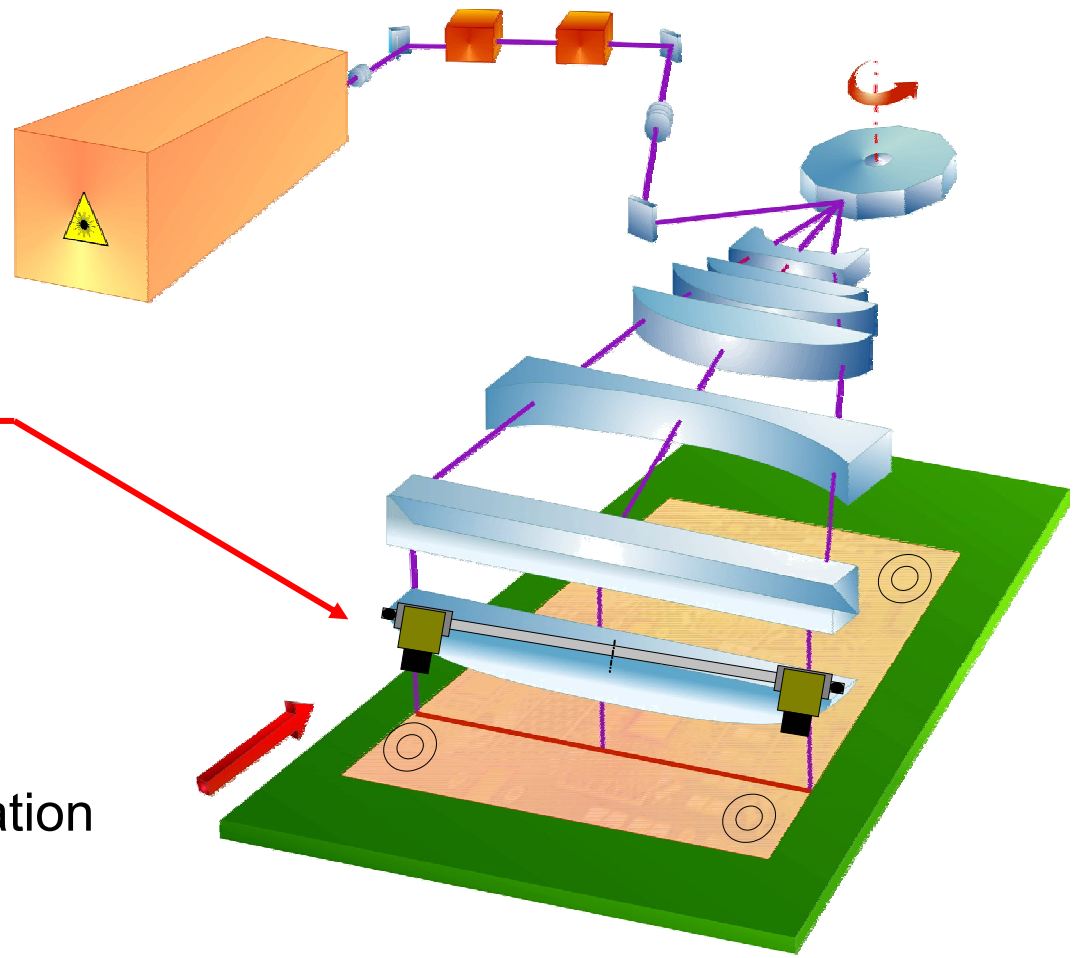
# Laser Direct Imaging (LDI)



- Improved Resolution
  - System Resolution 4000 dpi
  - System Capability: 50µm/50µm (.002”/.002”) Line & Space
- Improved Registration
  - CCD Camera System & Target Fiducials
    - Through Holes Drilled
    - 24 Hole Pattern of Laser Drilled Microvia
  - System capability
    - Positional Accuracy +/-25µm
- LDI Solder Mask
  - Beta testing is in progress on Taiyo LDI SM

# Laser Direct Imaging (LDI)



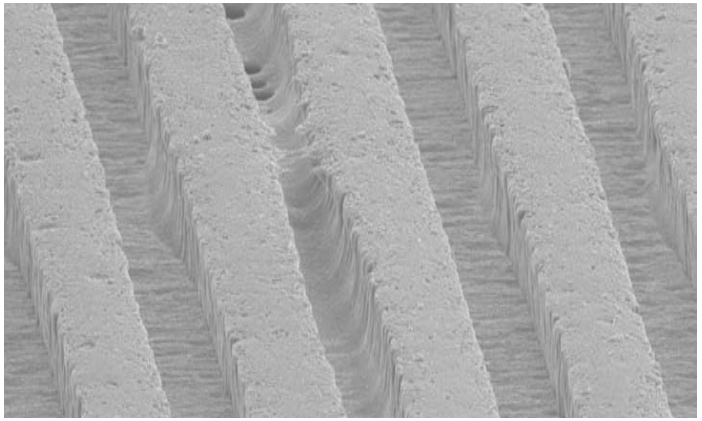


Using CCD Cameras and Mechanical or Laser Drilled Fiducials it is possible to get perfect registration every time.

# Laser Direct Imaging (LDI)

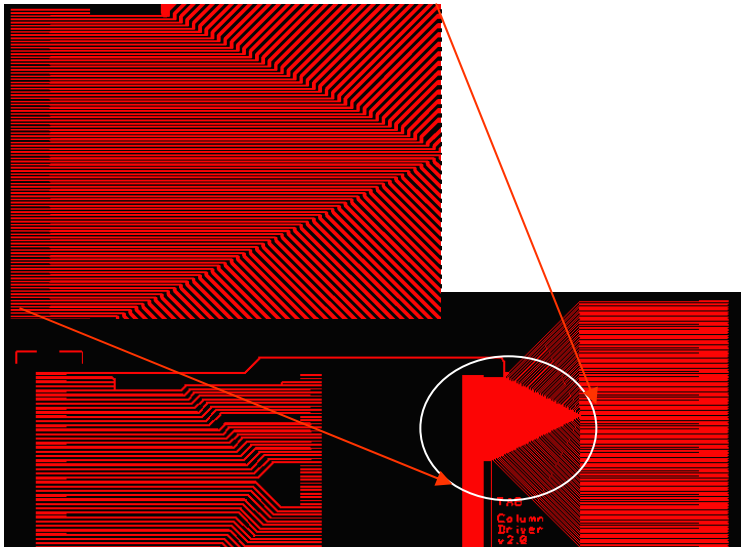


Using Laser Imaging it is possible to achieve finer resolution without the impact to yield that is experienced in contact printing using Photo Tools.



Printing Defects Using a Photo Tool


Improved Image Quality with LDI

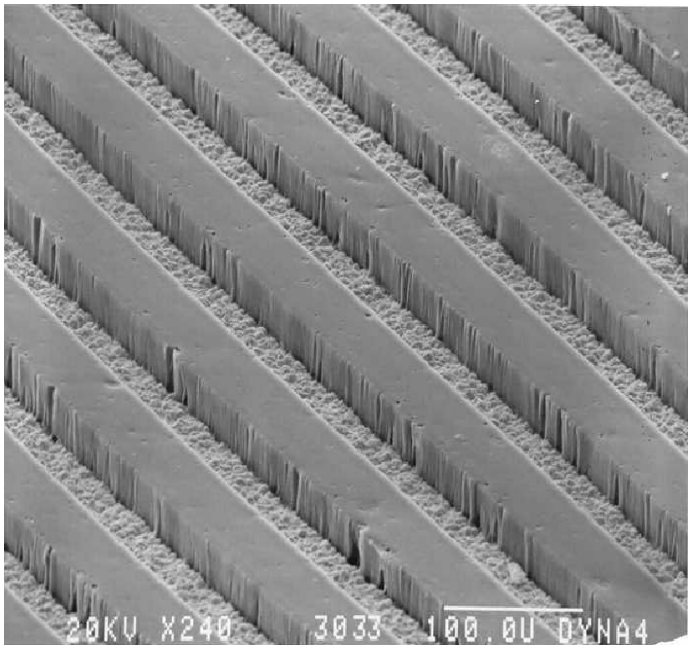


1.5 mil Track and Gap in Manufacture

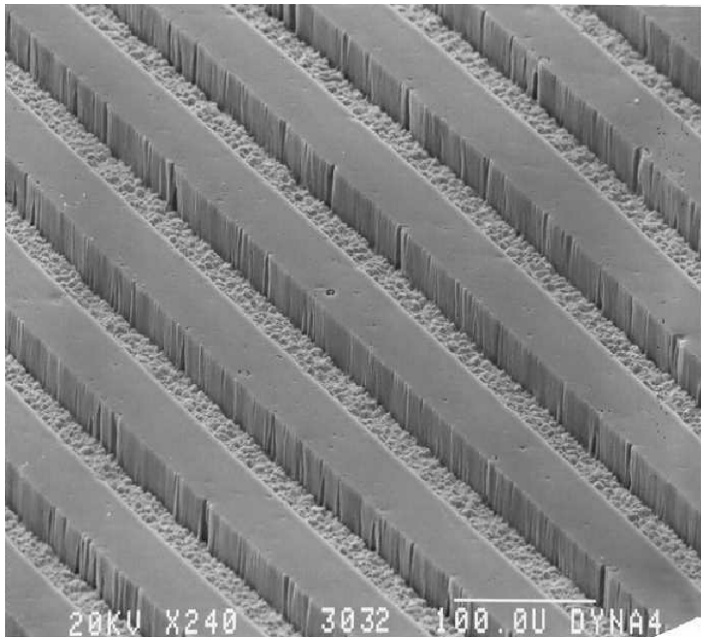
# Dynamic Details, Inc.

## Laser Direct Imaging (LDI)

Vertical




Horizontal




50µm/50µm (.002”/.002”)

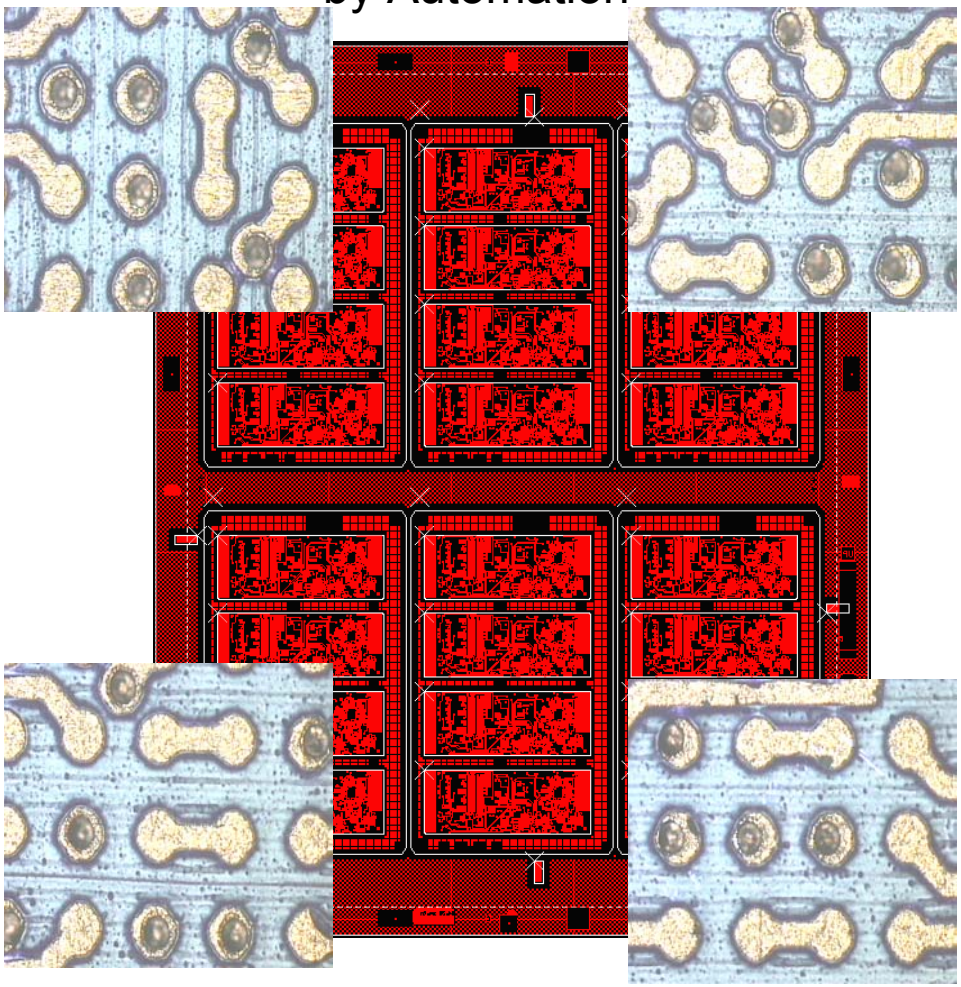
Shipley LD 730 Photo Resist

# Laser Direct Imaging (LDI)



Using the DP-100 Registration Features and Data Scaling Option it is possible to register a 4 mil pad to a 2 mil via without 'Break Out' in production using a 20 x 16" manufacturing panel

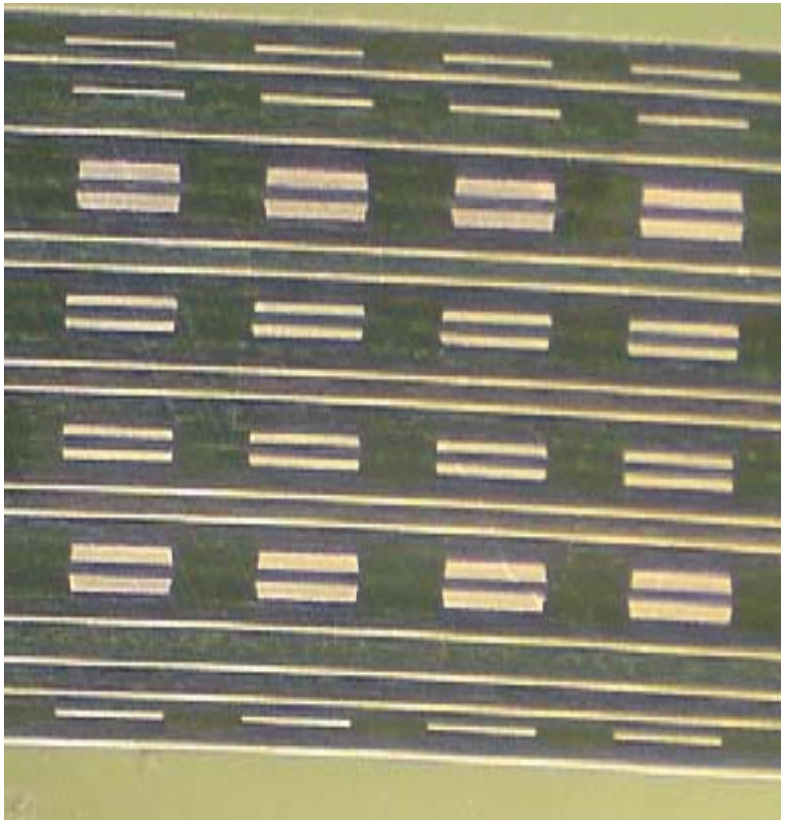
Better Registration by Automation



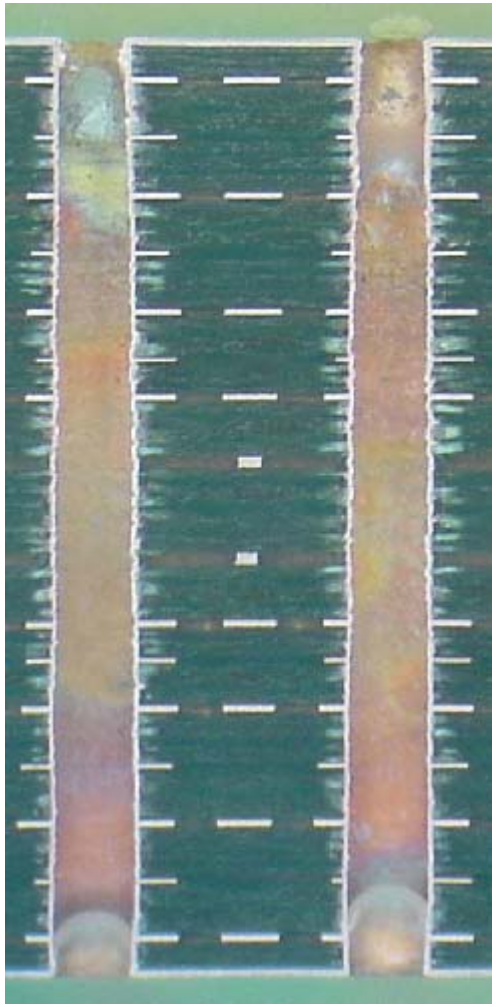
# Dynamic Details, Inc.

## Laser Direct Imaging (LDI)

Precise Inner Layer Registration



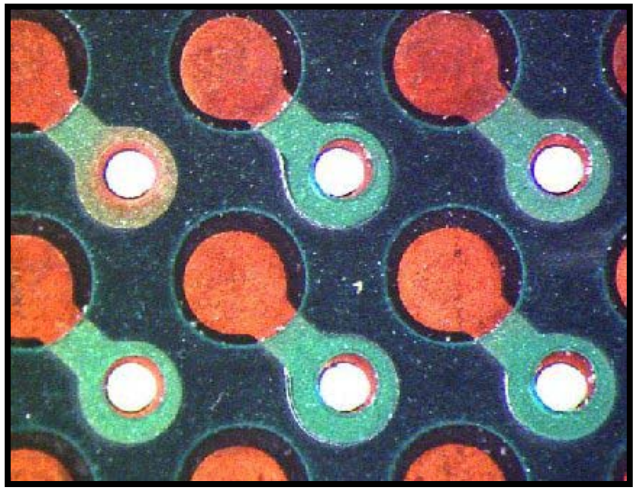
24 Layer PCB Cross-Section



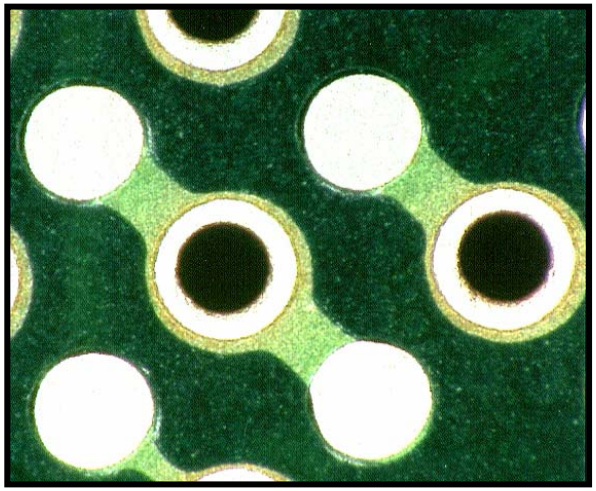
# Laser Direct Imaging (LDI) Solder Mask



- Laser Direct Imaged Solder Mask
  - Adaptively tooled
  - Improved Registration +/- 0.001” vs +/- 0.003”



Standard LPI Solder Mask
+/- 0.003”



Laser Defined Solder Mask
+/- 0.001”

# Dynamic Details, Inc.

Enabling Technologies

## Overview

- Technology Drivers
- Advanced Materials
- Characterized FR-4
- Hybrid Constructions
- Laser Direct Imaging
- High Aspect Ratio Copper Plating
- Laser Drilling
- Planar Via Technologies

# High Aspect Ratio Pulse Plating



## High Aspect Ratio Copper Plating

- Equipment — Complex Waveform (WST) Pulse
- Process — Mixed Frequency WST
  - Max effect on mixed feature on boards
  - Wide operating window
- Chemistry — MACuSPEC from MacDermid

# Conventional Copper Electroplating



## Typical Plating Capabilities

| Description | Aspect ratio | Via/Hole Diameter | Dielectric/ Board Thickness |
|---|---|---|---|
| **Microvia** | 0.5:1 | 100 µm (.004”) | 50 µm (.002”) |
| **PTH** | 8:1 | 200 µm (.008”) | 1.75 mm (.062”) |
| **PTH** | 10:1 | 337.5 µm (.0135”) | 3.4 mm (.135”) |

# High Aspect Ratio Pulse Plating



## Pulse Plating Capabilities

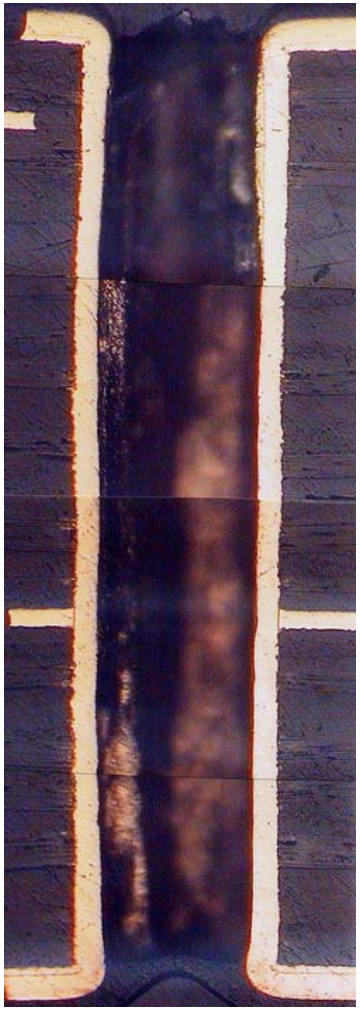
| Description | Aspect ratio Advanced | Aspect ratio Emerging[1] | Via/Hole Diameter | Dielectric/ Board Thickness |
|---|---|---|---|---|
| **Microvia** | 0.6:1 | 1:1[2] | 100 µm (.004”) | 100 µm (.004”) |
| **PTH** | 11:1 | 14:1 | 200 µm (.008”) | 2.8 mm (.112”) |
| **PTH** | 14:1 | 16:1 | 337.5 µm (.0135”) | 5.4 mm (.216”) |

Notes:

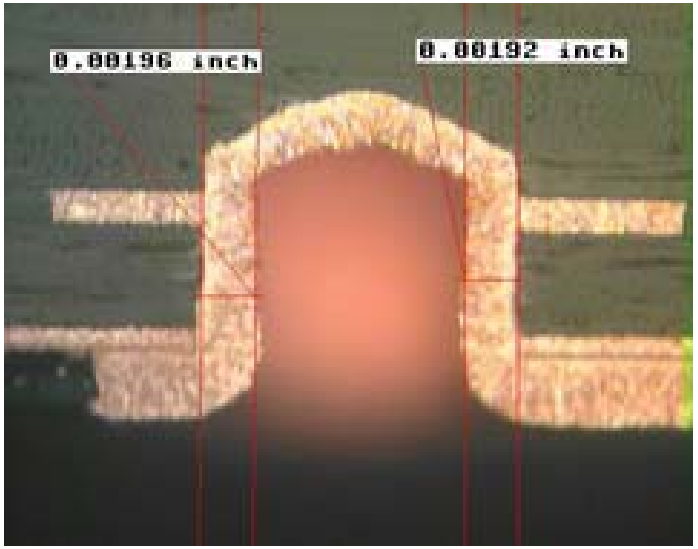
1- Capabilities have been proven ! Consult DDI engineering
2- Requires special electroless process and may not work on all applications

# High Aspect Ratio Pulse Plating





Aspect Ratio = 14:1
Thickness 2.8mm (.112”)
Drill dia. 200 µm (.008”)



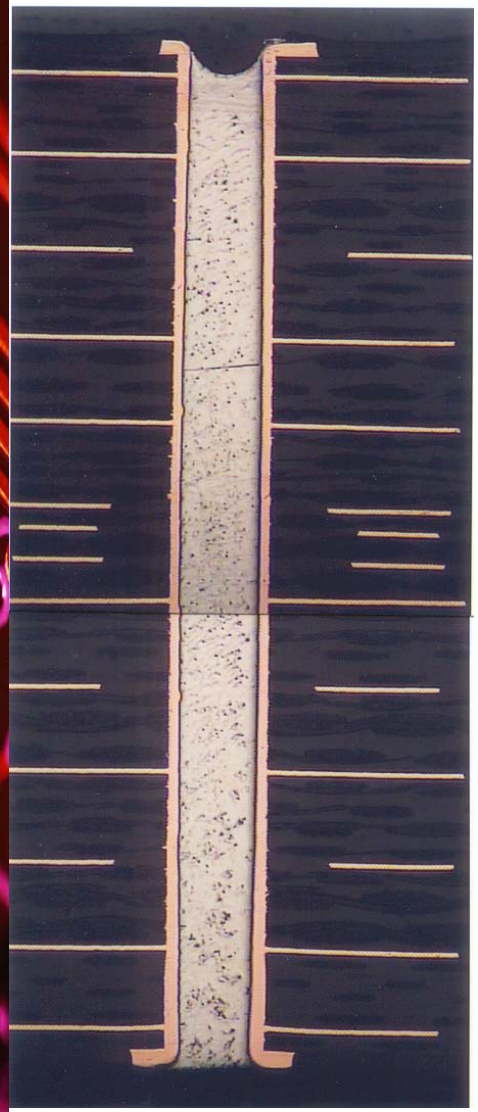

Controlled depth mechanical drilling

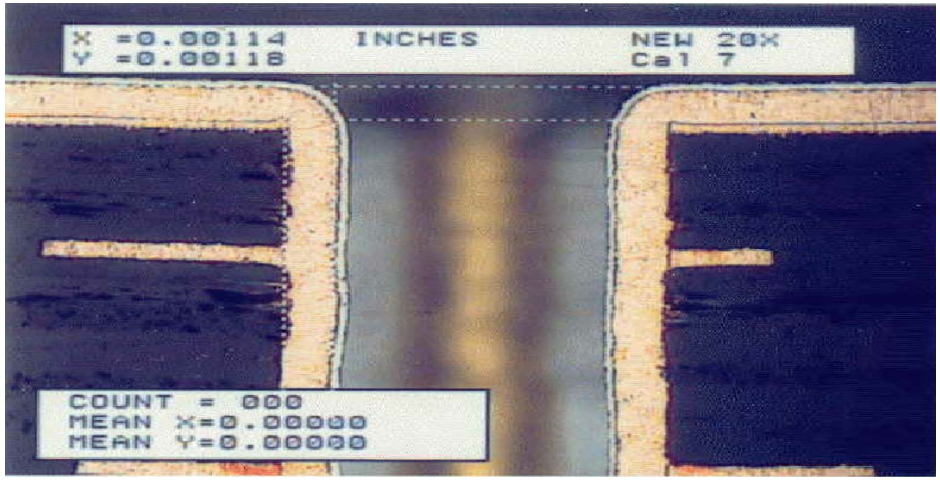
# Dynamic Details, Inc.

## High Aspect Ratio Pulse Plating

Enabling Technologies

Aspect Ratio = 16:1  Thickness = 5.4mm (.216”) Drill dia. = 337.5 µm (.0135”)

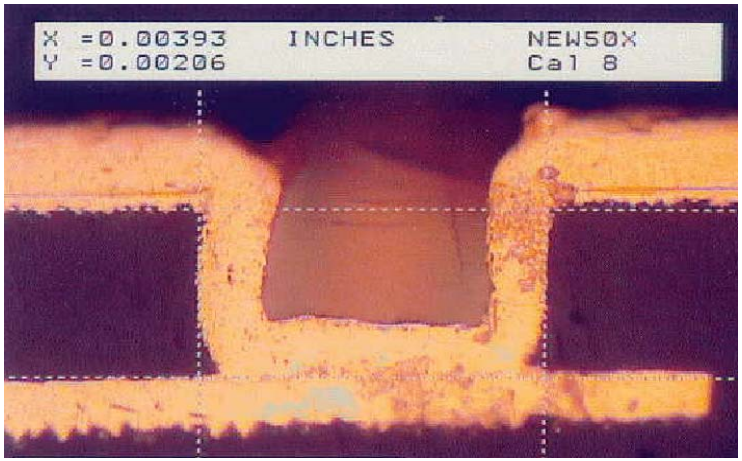


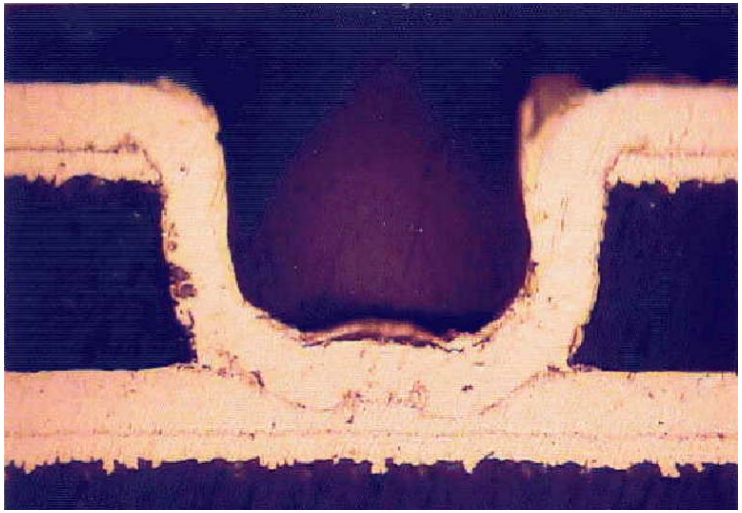



36 Layer MLB

# High Aspect Ratio Pulse Plating

Enabling Technologies



Laser drilled microvia's
Aspect Ratio 0.5:1

# Dynamic Details, Inc.

Enabling Technologies

## Overview

- Technology Drivers
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- Characterized FR-4
- Hybrid Constructions
- Laser Direct Imaging
- High Aspect Ratio Copper Plating
- Laser Drilling
- Planar Via Technologies

# Laser Drilling Technology & Microvias



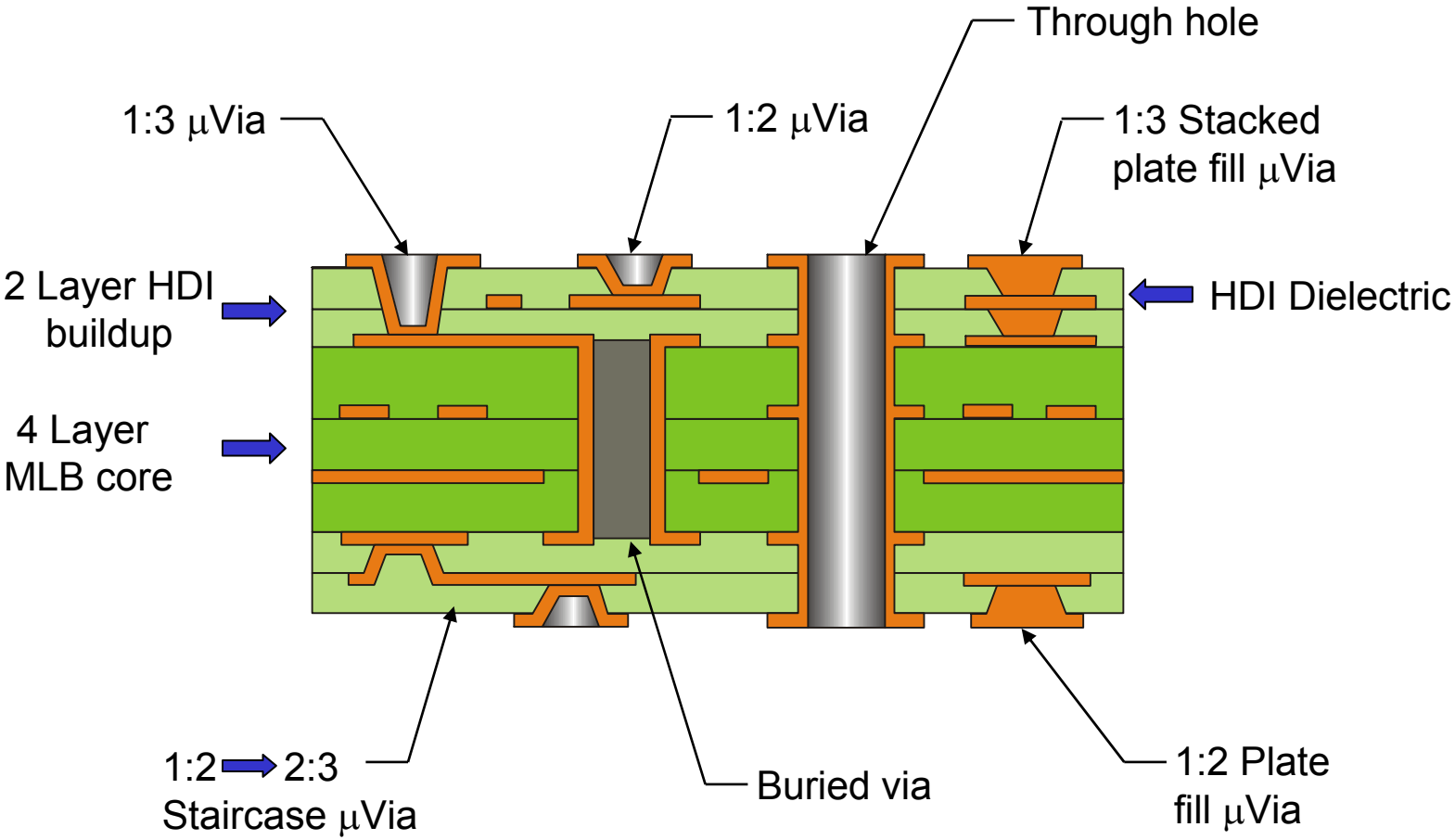
## What is considered a Microvia ?

- Generally microvia's are considered to be blind holes that terminate to a lower layer without the need to generate a sub-lamination
- Hole diameters range from 3 to 8 mils and are typically in the 4 to 6 mil range
- Hole depth is limited by copper plating aspect ratio, typically 0.5: to 0.6:1 however higher aspect ratios have been achieved
- Most common method for hole formation is laser drilling with YAG lasers
- Microvia's terminate to the underlying pad without penetrating the copper

# Laser Drilling Technology



## Common High Density Via Structures




2-4-2 HDI Substrate

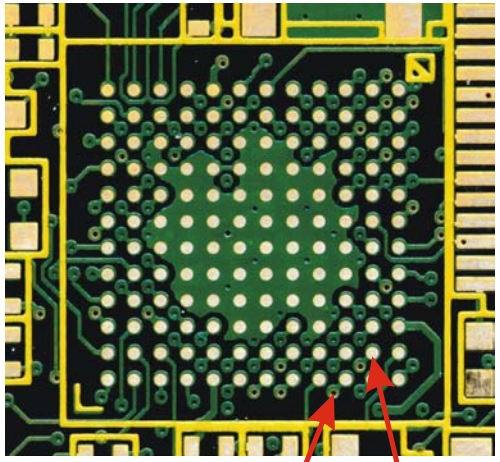
# Laser Drilling Technology



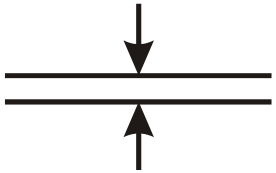
## Conventional MLB vs HDI

0.8 mm µBGA

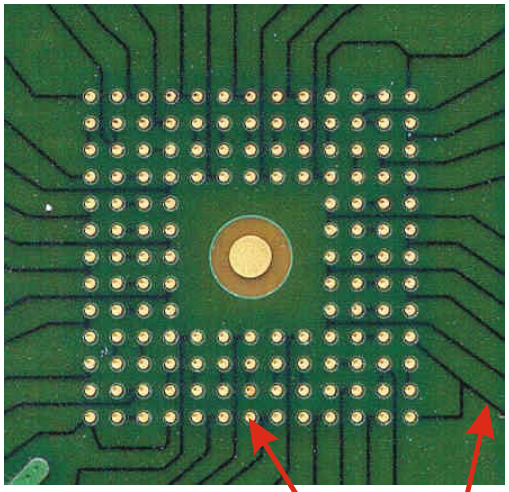
Conventional MLB Substrate



0.8 mm



HDI Substrate



Mechanical drilled via's offset from attachment pad

Solder mask defined pad

Laser drilled via in pad (Solder mask defined attachment pad layer # 1)

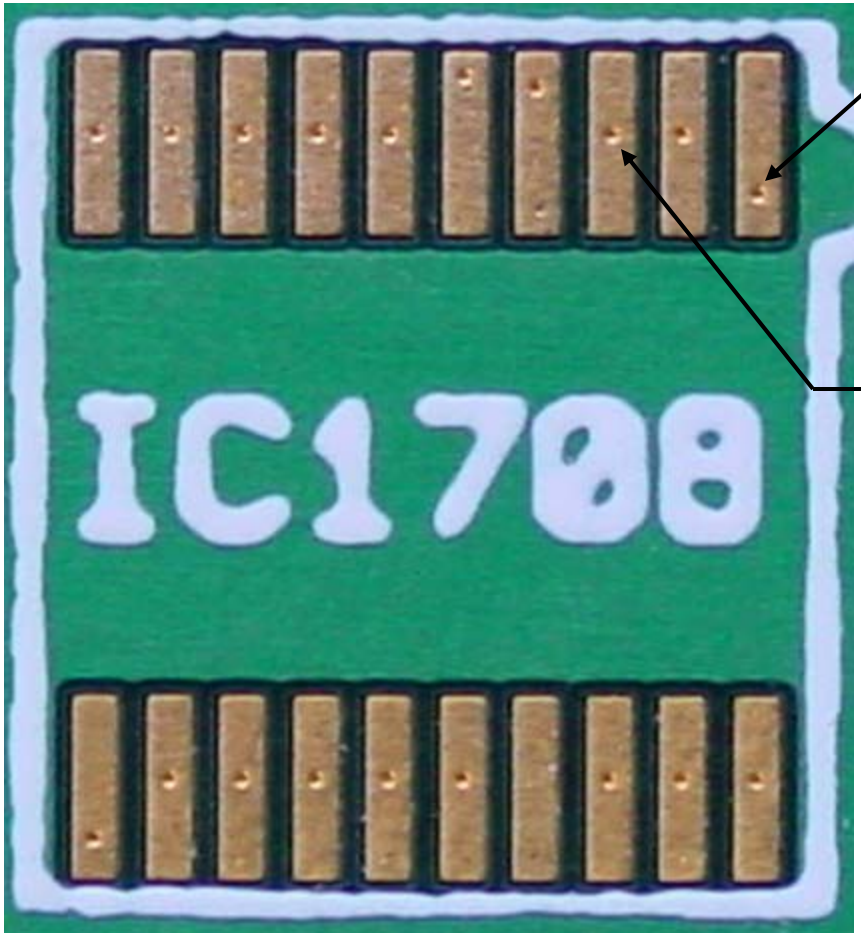
Signal routing on layer # 2

# Dynamic Details, Inc.

## Laser Drilling Technology

0.5 mm

### Microvias in SMT Pads



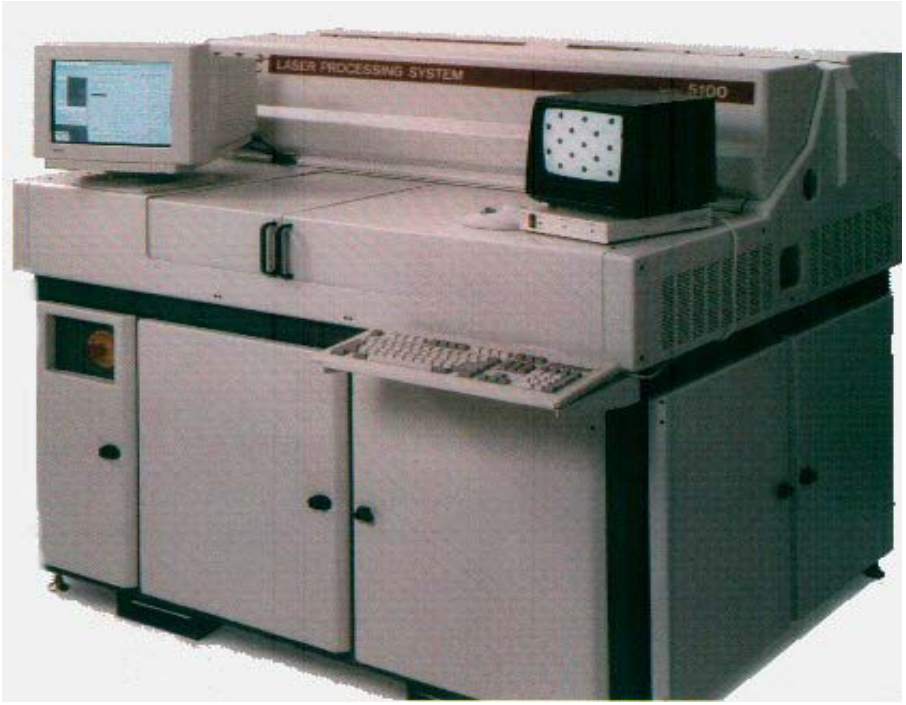

Laser Drilled Microvias

Via location does not impact assembly due to it's extremely small volume

# Laser Drilling Technology



## Common Laser Drilling Techniques



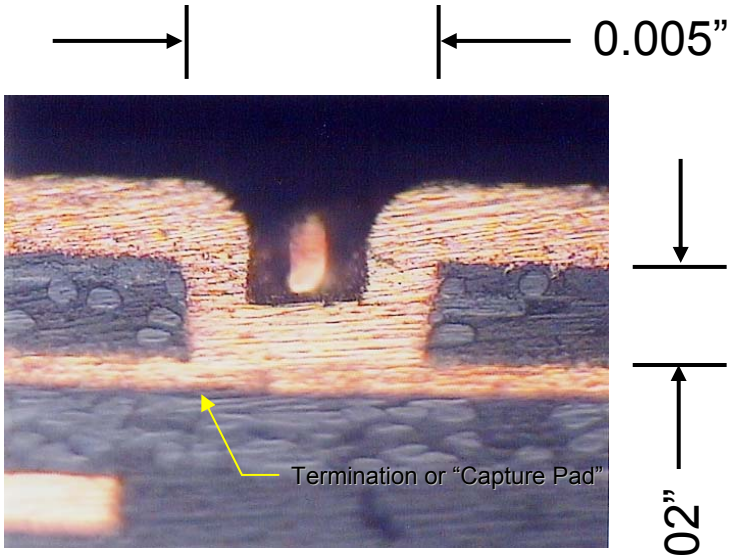

**ESI ND:YAG Drilling System**

- **ND:YAG (Ultra-Violet)** Capable of drilling copper, all re-enforcing materials and all laminate resin systems. 25 to 50 micron beam forms holes by spiraling of trepaning the beam
- **$C0_2$ (Infrared) Capable of** drilling most re-enforcing materials and laminate resin systems. Not effective for drilling copper (copper is reflective in the infrared spectrum) Forms holes by pulsing a larger high energy beam
- **Combination ND:YAG $CO_2$ forms** holes by removing copper with the ND:YAG laser and the dielectric and re-enforcing material with the $CO_2$ laser

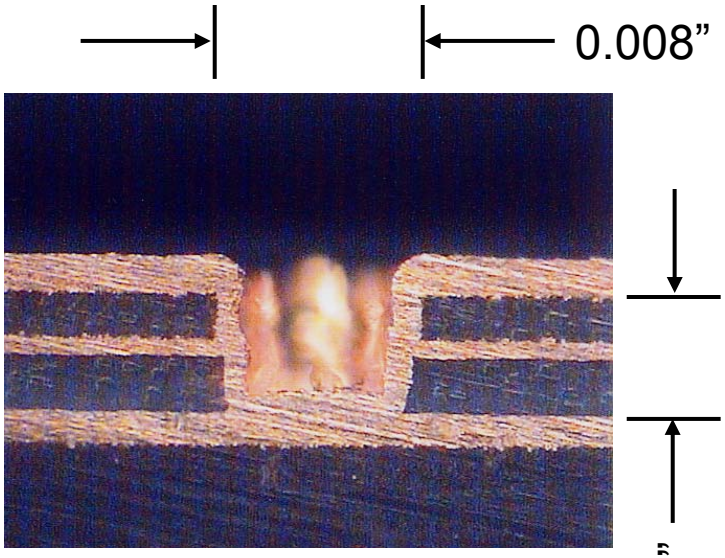
# Laser Drilling Technology



Typical laser drilled Microvia geometry




Laser drilled Microvia
Layer 1 to 2




Laser drilled Microvia
Layer 1 to 3

Note: Typical aspect ratio on laser drilled holes is 0.5:1 to 0.7:1 max

# Laser Drilling Technology



## Factors Impacting Laser Drilling Time & Cost

- Copper foil thickness
- Dielectric thickness
- Hole diameter
- Dielectric composition
  - Non-reinforced resin (RCC)
  - Non-woven reinforcement (Thermont ®)
  - Woven (106 , 1080 glass)
- System Optimization = increases velocity and power

# Laser Drilling Technology



## Typical ND:YAG Laser Drilling Speeds

| Cu Thick. | Via Dia. | Drilling Speed Holes/sec. | | | |
|---|---|---|---|---|---|
| 9 µm | 100 µm | 76 | 97 | 94 | 57 |
| 9 µm | 150 µm | 47 | 54 | 53 | 38 |
| 9 µm | 200 µm | 30 | 32 | 30 | 28 |

1080 Epoxy/glass prepreg
Epoxy Resin Coated Copper (50 µm)
Random Aramid fiber (50 µm Thermont®)
Laser drillable prepreg (1080 LD Prepreg)

# Routing Channel Density vs. Via Structure



Standard through hole technology:
Channel density limited by via density, geometry and pitch

Microvias:
Channel density enhanced through smaller geometry
Limited Z axis connectivity

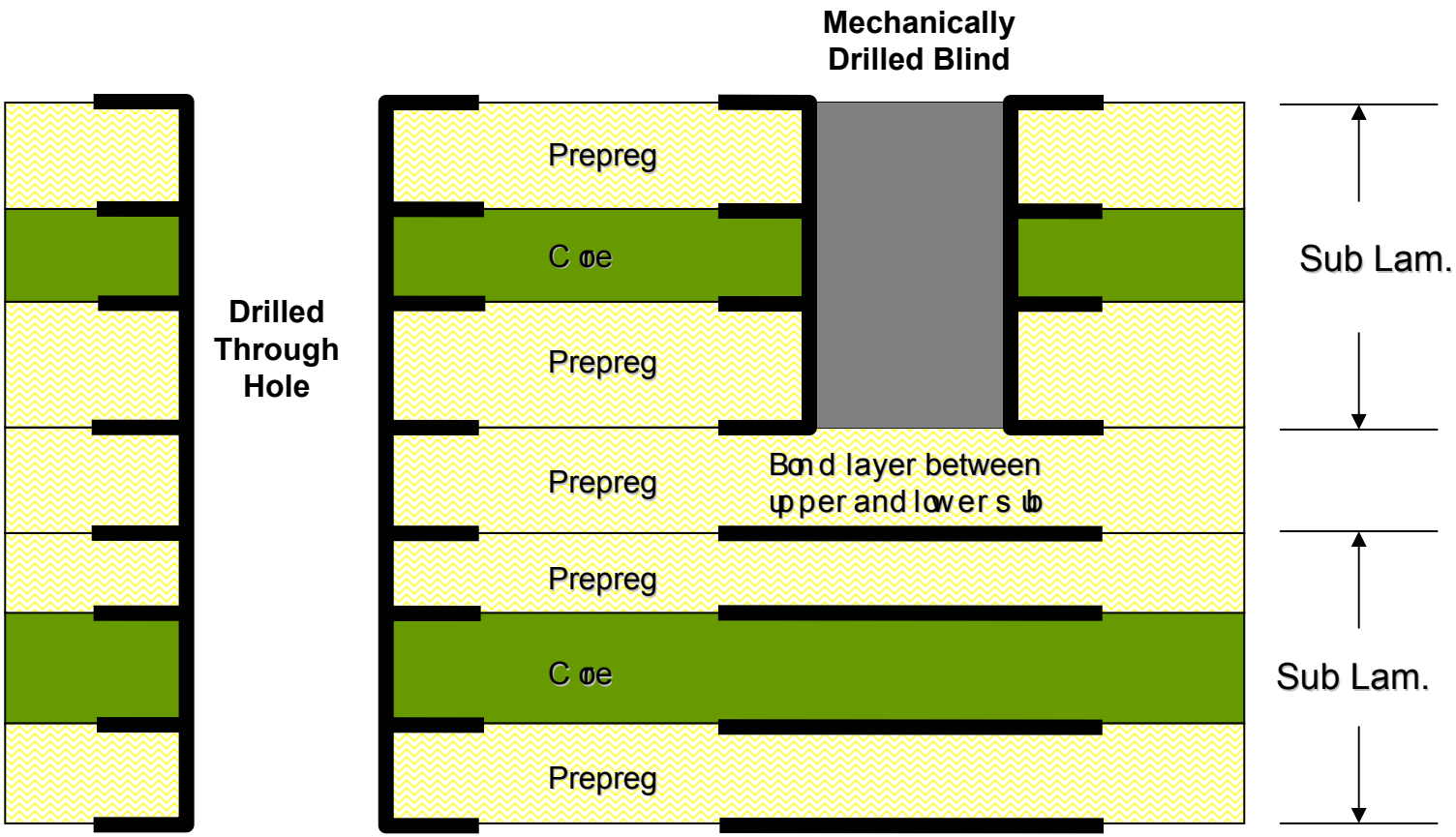
Blind & Buried via's:
Channel density enhanced
Still geometry limited
Limited Z axis connectivity

SMV:
Channel density enhanced through smaller geometry
Unlimited Z axis connectivity

Once you leave through hole designs the goal is to find the via combination that maximizes routing channel density at the lowest cost

# Routing Channel Density vs. Via Structure

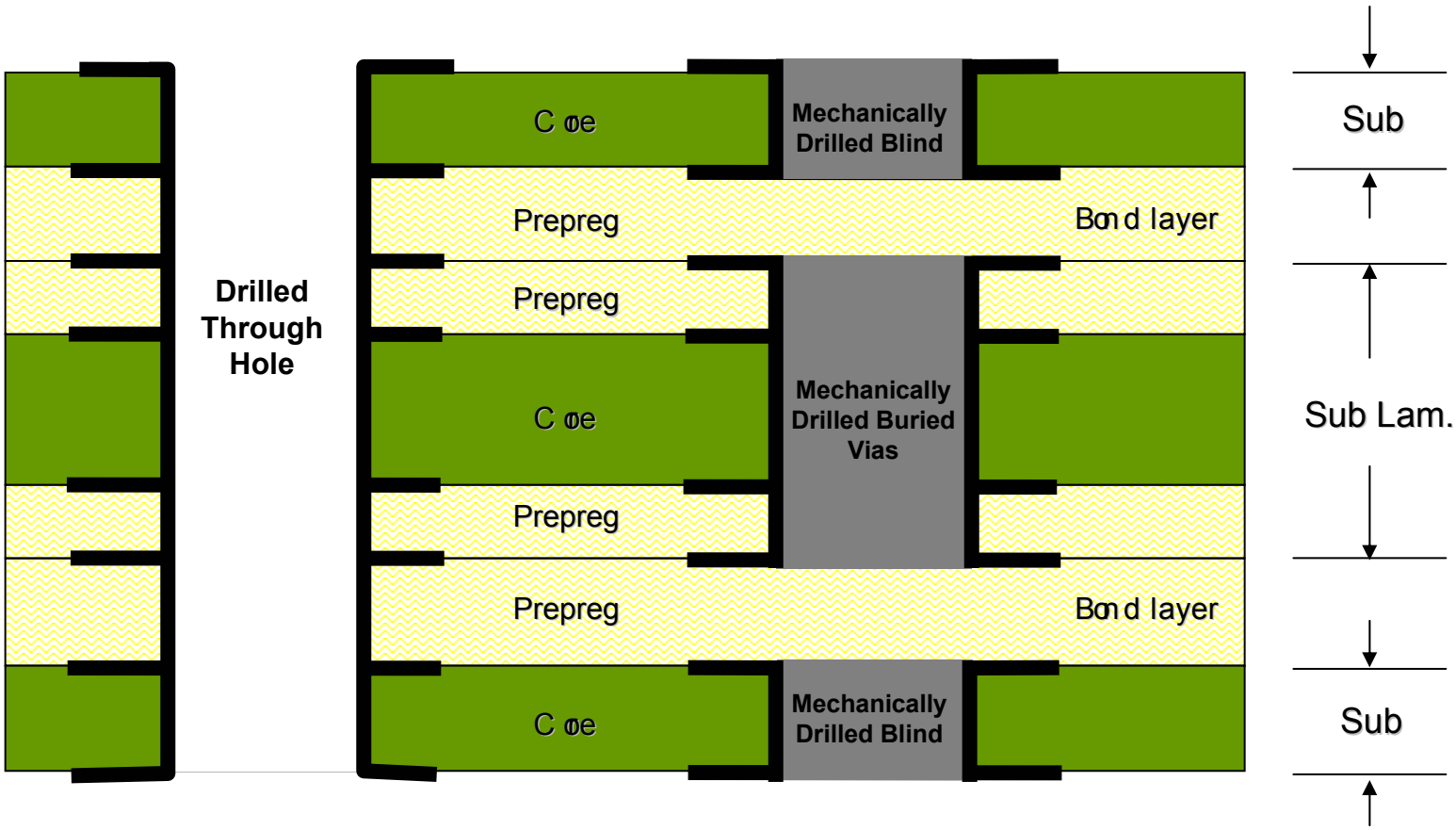





- Increased channel density on lower sub lamination
- Standard PTH geometry apply, reduced aspect ratio on sub drill
- Anti-pad diameter must account for tolerance buildup in multiple laminating cycles

# Routing Channel Density vs. Via Structure

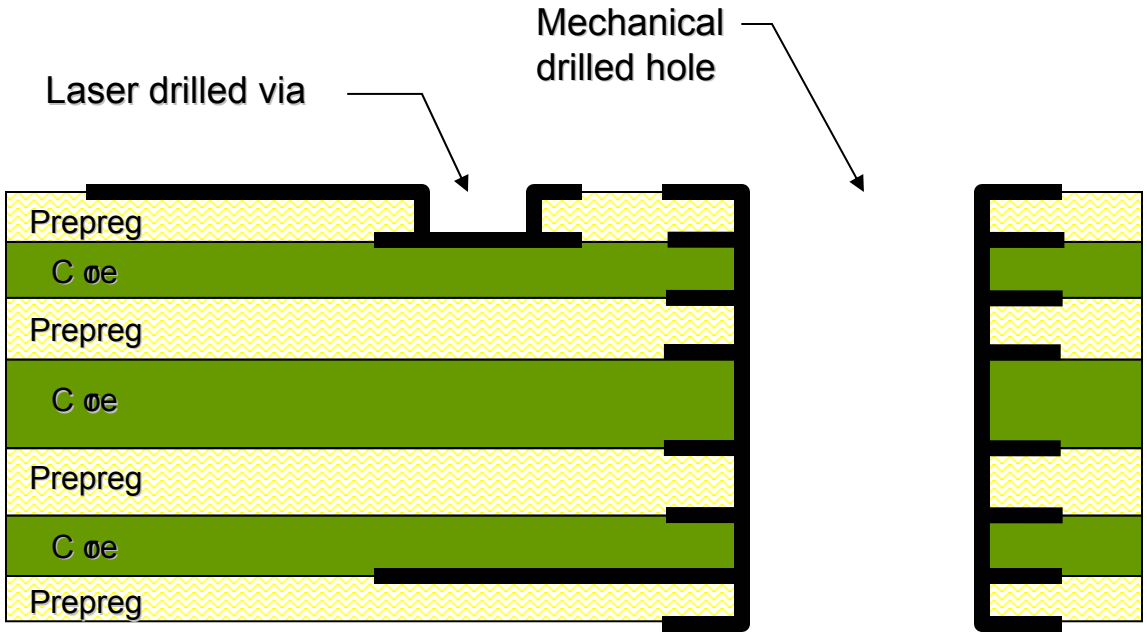
Enabling Technologies




- Increased channel density on sub lamination
- Standard PTH geometry apply, reduced aspect ratio on sub drill
- Anti-pad diameter must account for tolerance buildup in multiple laminating cycles
- No Z axis connectivity between adjacent sub-laminations

# Routing Channel Density vs. Via Structure

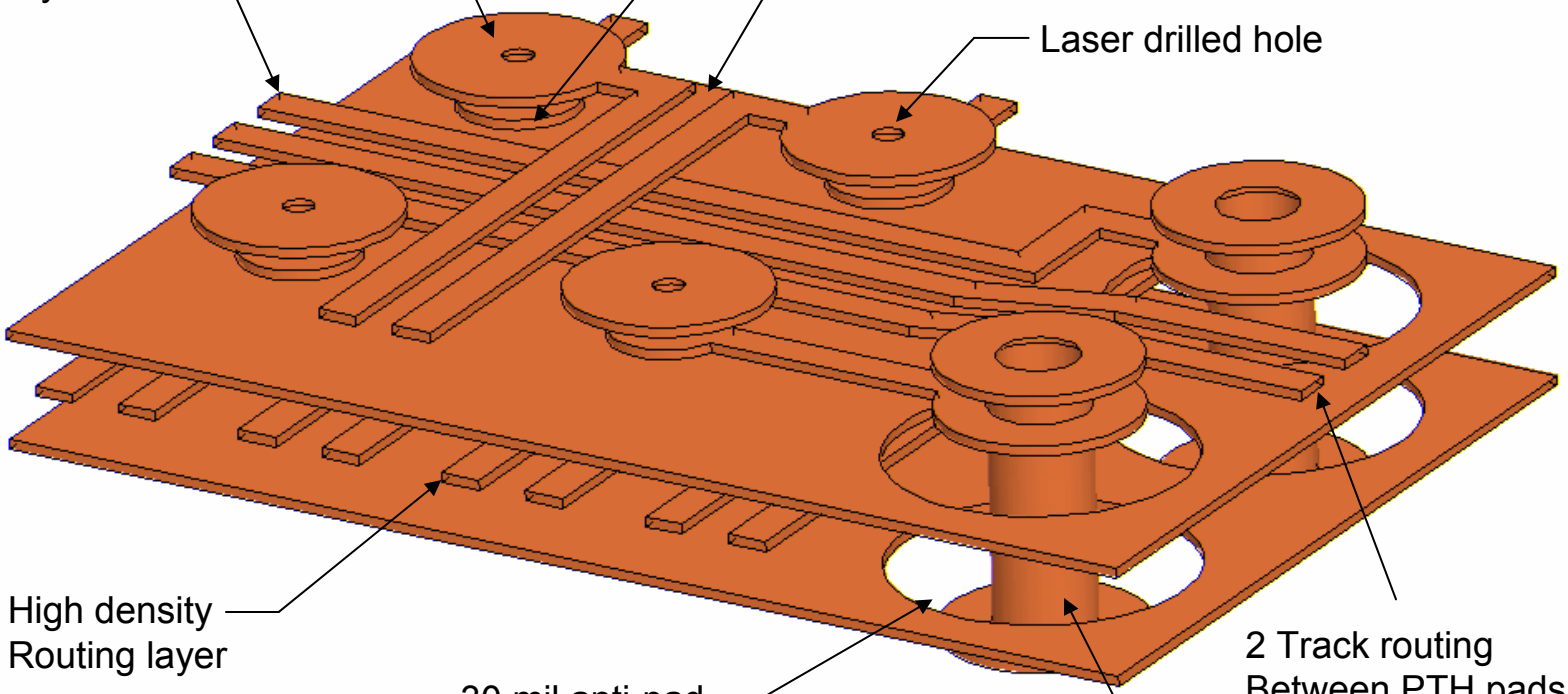





- Increased channel density on layer 1 and 2 from reduced geometry
- Increased channel density on layers n-1 to n resulting from a blind hole
- Standard PTH geometry apply to mechanical drilled holes
- Dielectric thickness layer 1:2 limited by plating aspect ratio (0.5:1 to 0.6:1)

# Dynamic Details, Inc.

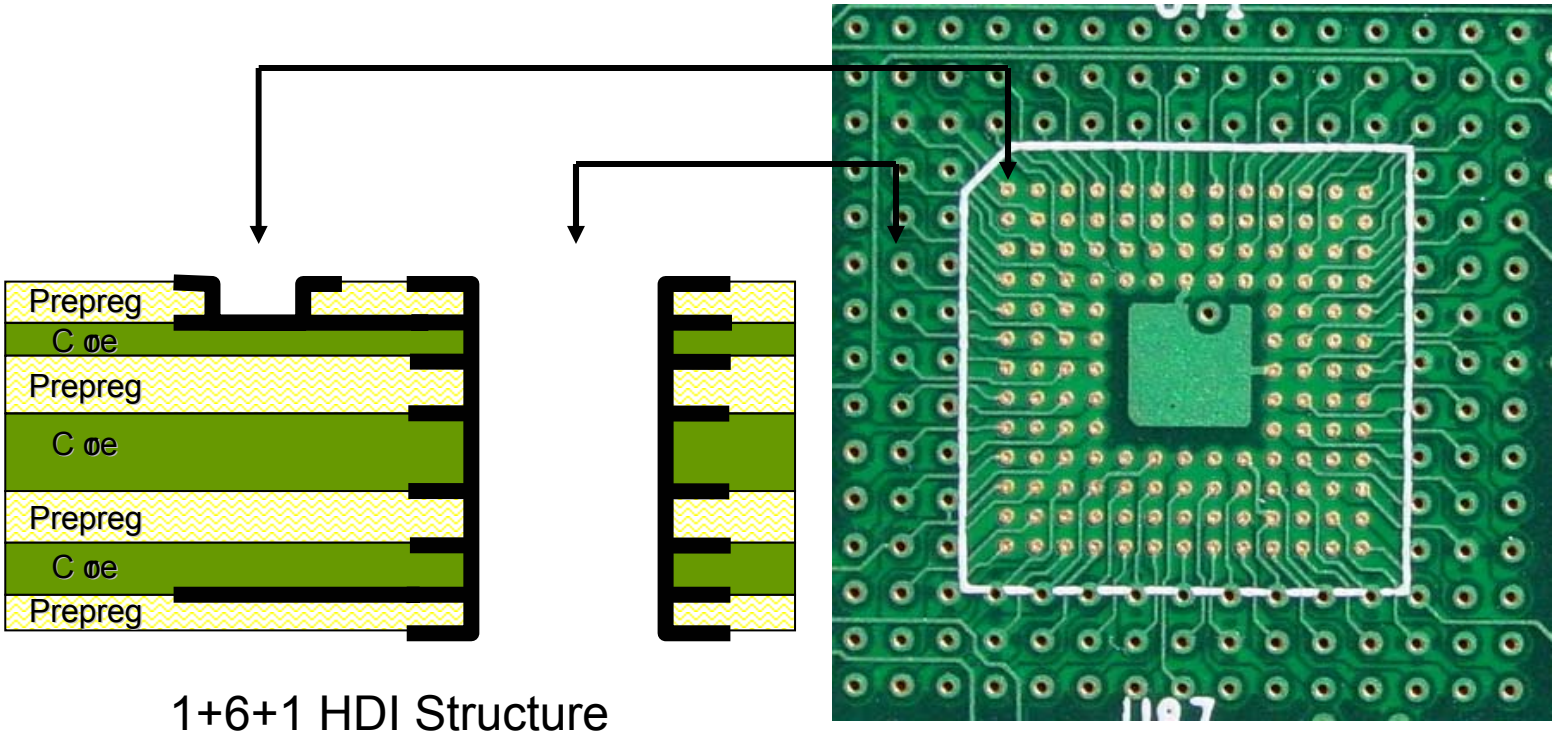
## Microvia Through Hole Combo 1.0 mm



# Microvia: 0.8 mm BGA Signal Routing



Microvia in pad used to enhance escape on high density BGA's

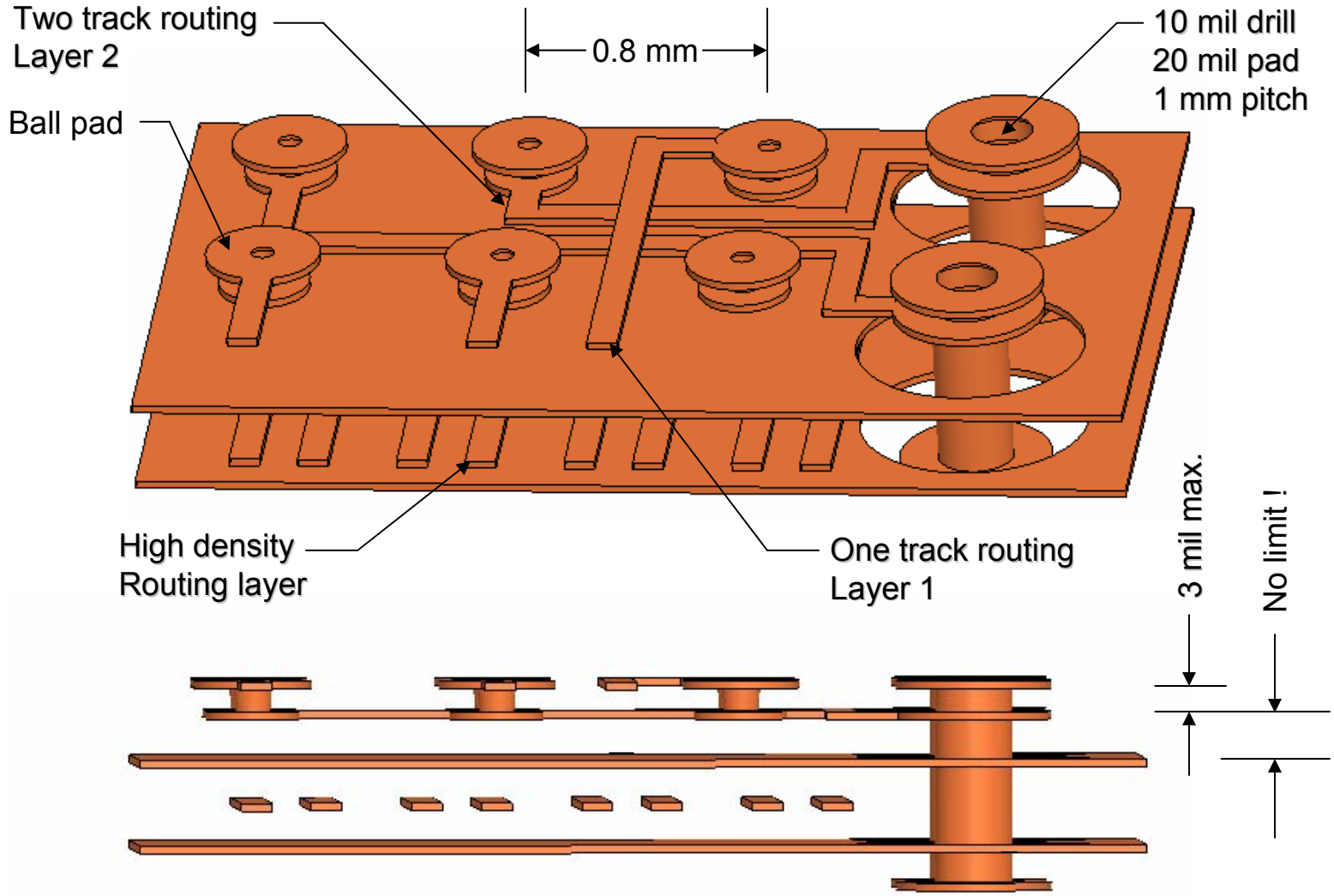



1+6+1 HDI Structure

0.8 mm BGA

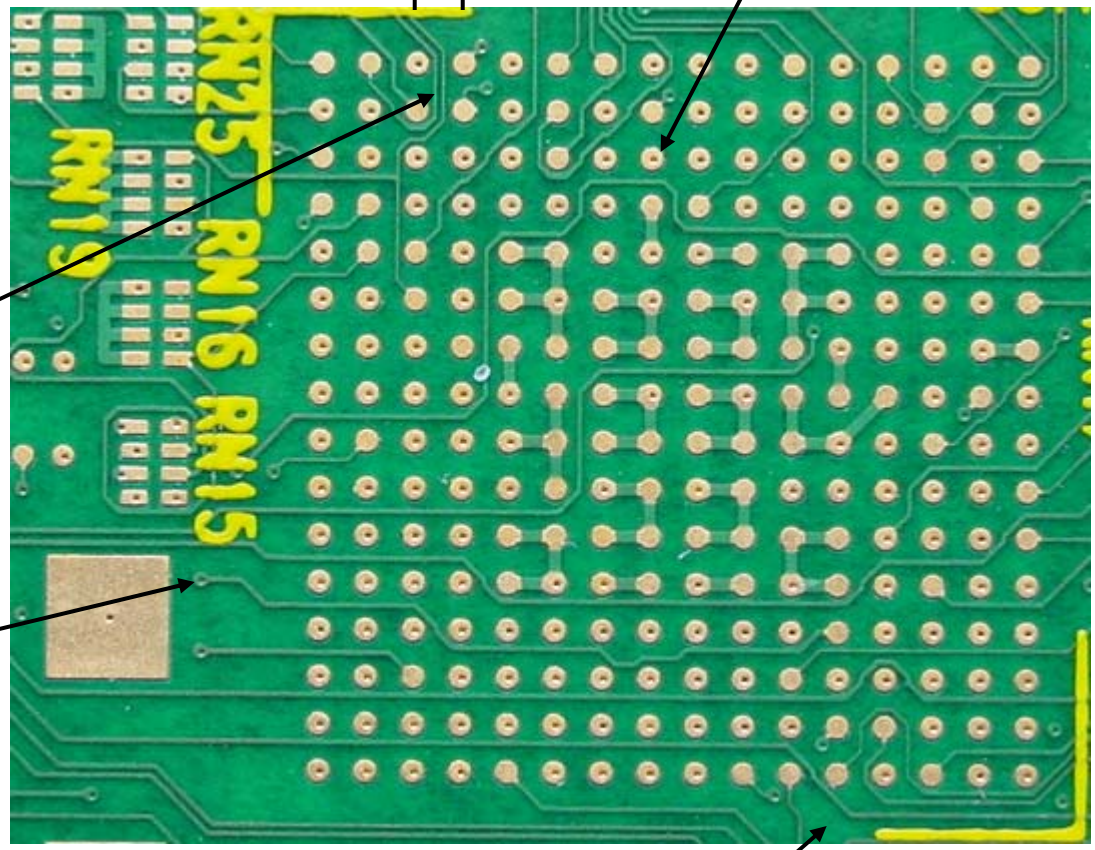
# Microvia Through Hole Combo 0.8 mm

Enabling Technologies



# Dynamic Details, Inc.

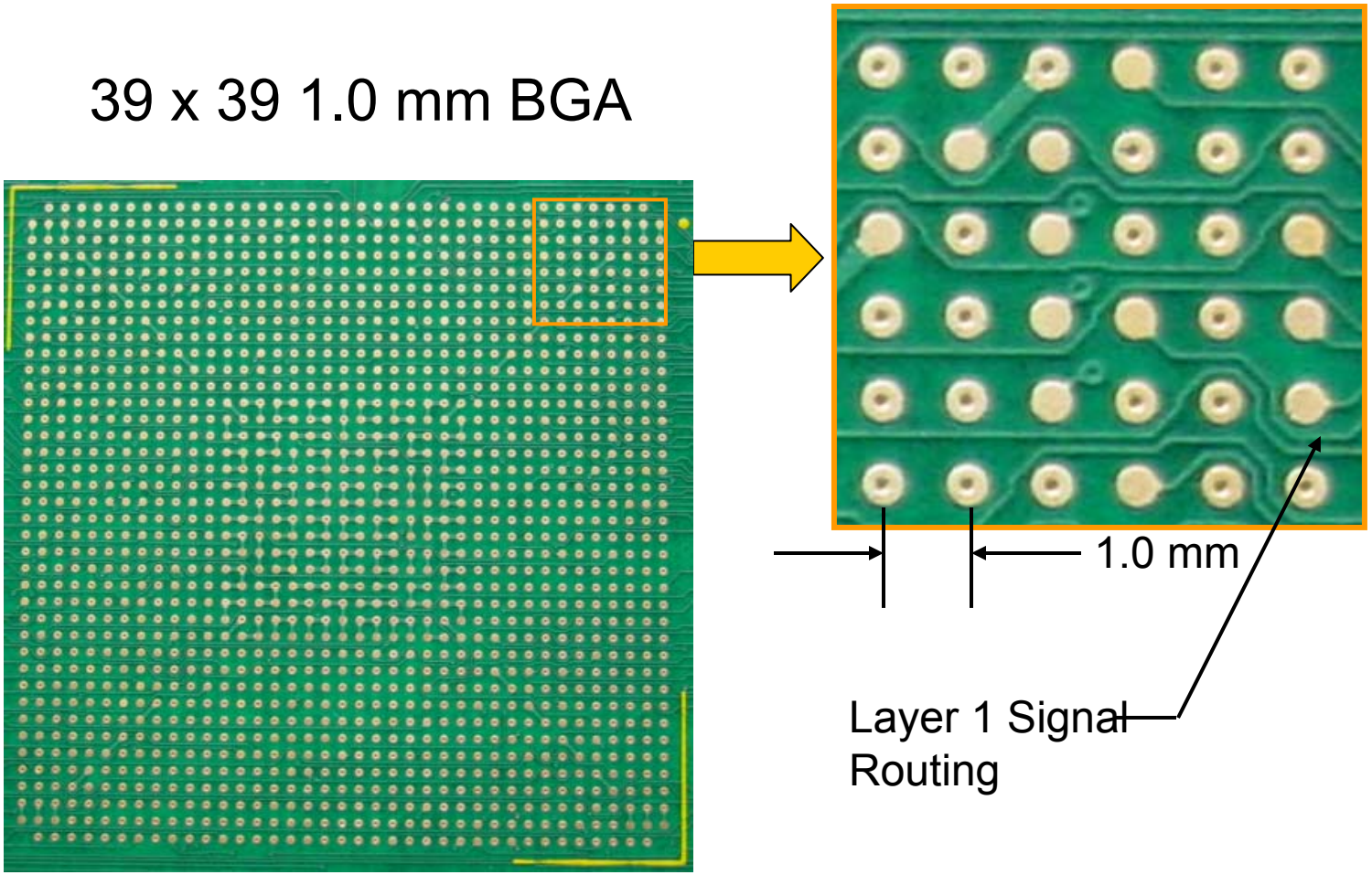
## Laser Drilling Technology



# Laser Drilling Technology

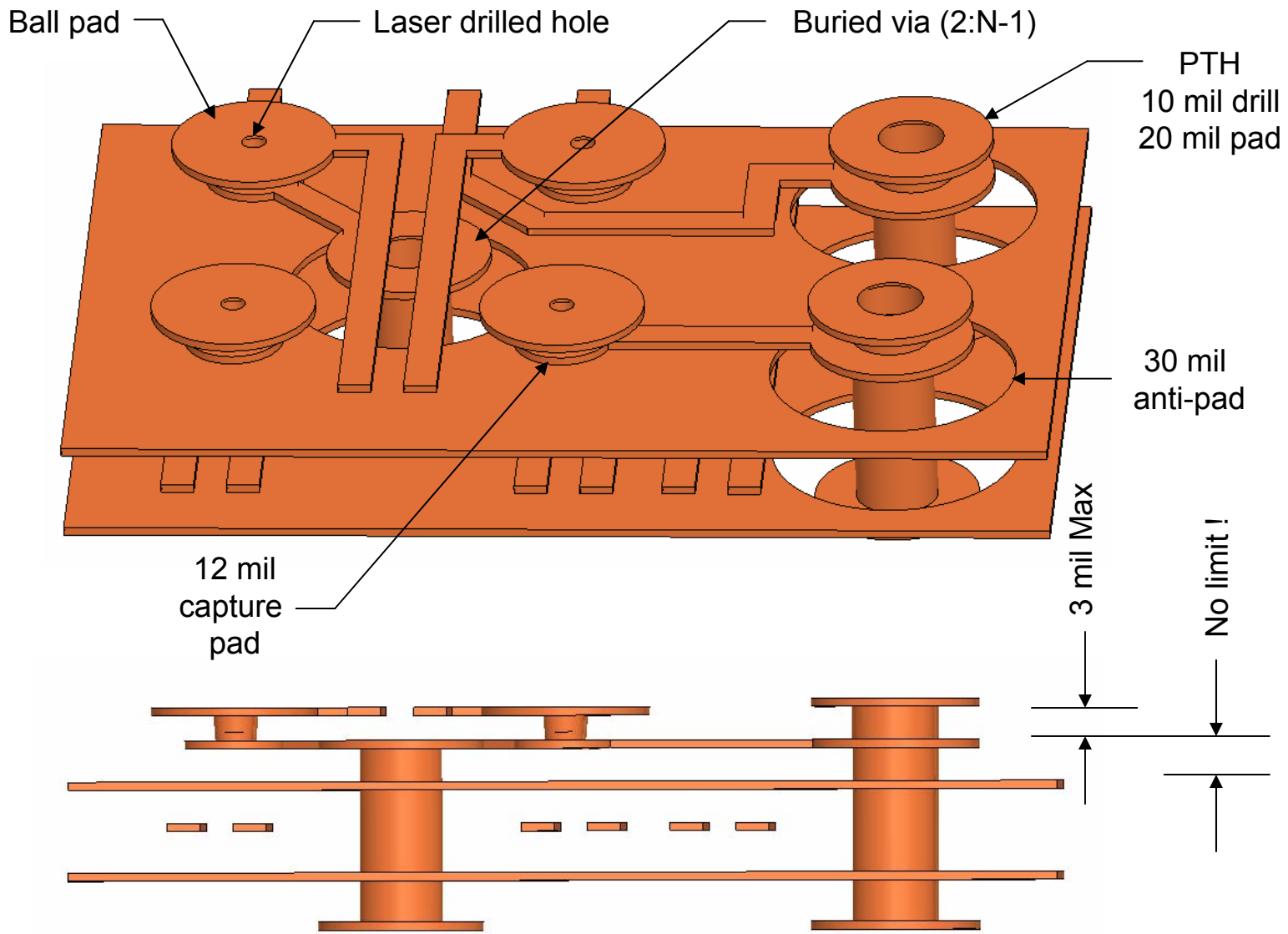


39 x 39 1.0 mm BGA



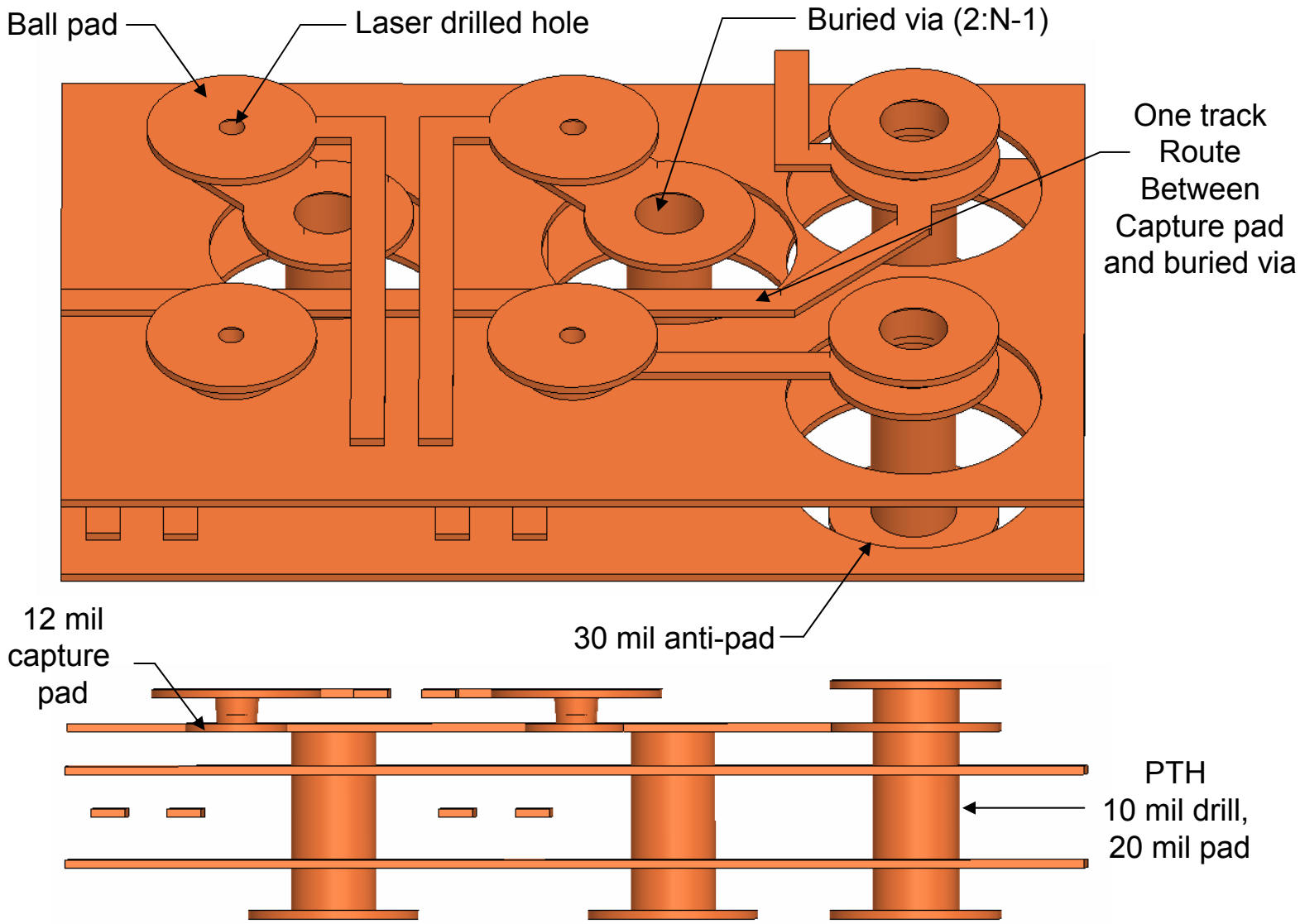
# Dynamic Details, Inc.

## µvia & Buried & PTH 1.0 mm Pitch (Full Offset)



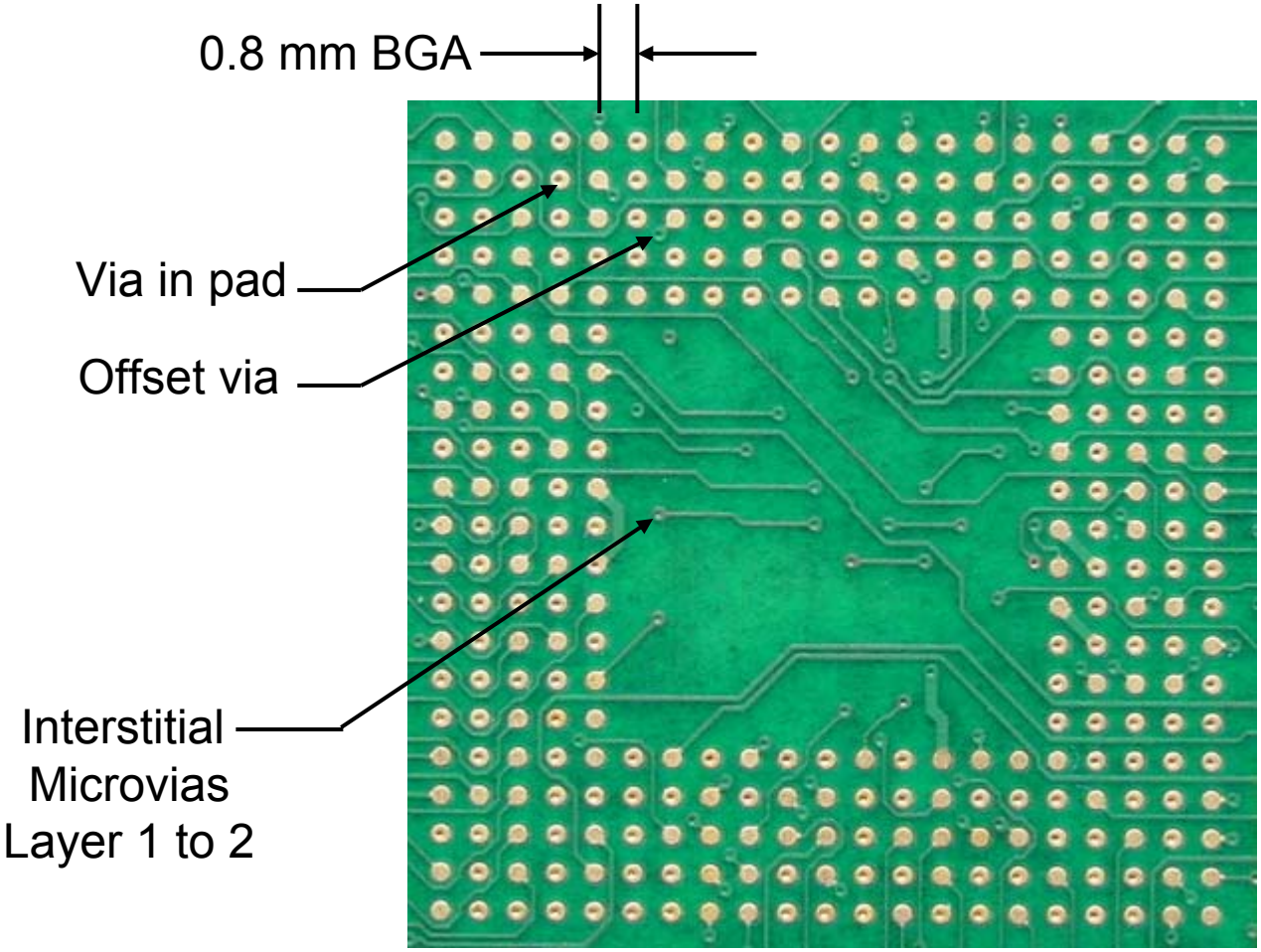
# Dynamic Details, Inc.

## µvia & Buried & PTH Via's 1.0 mm (Min Offset)



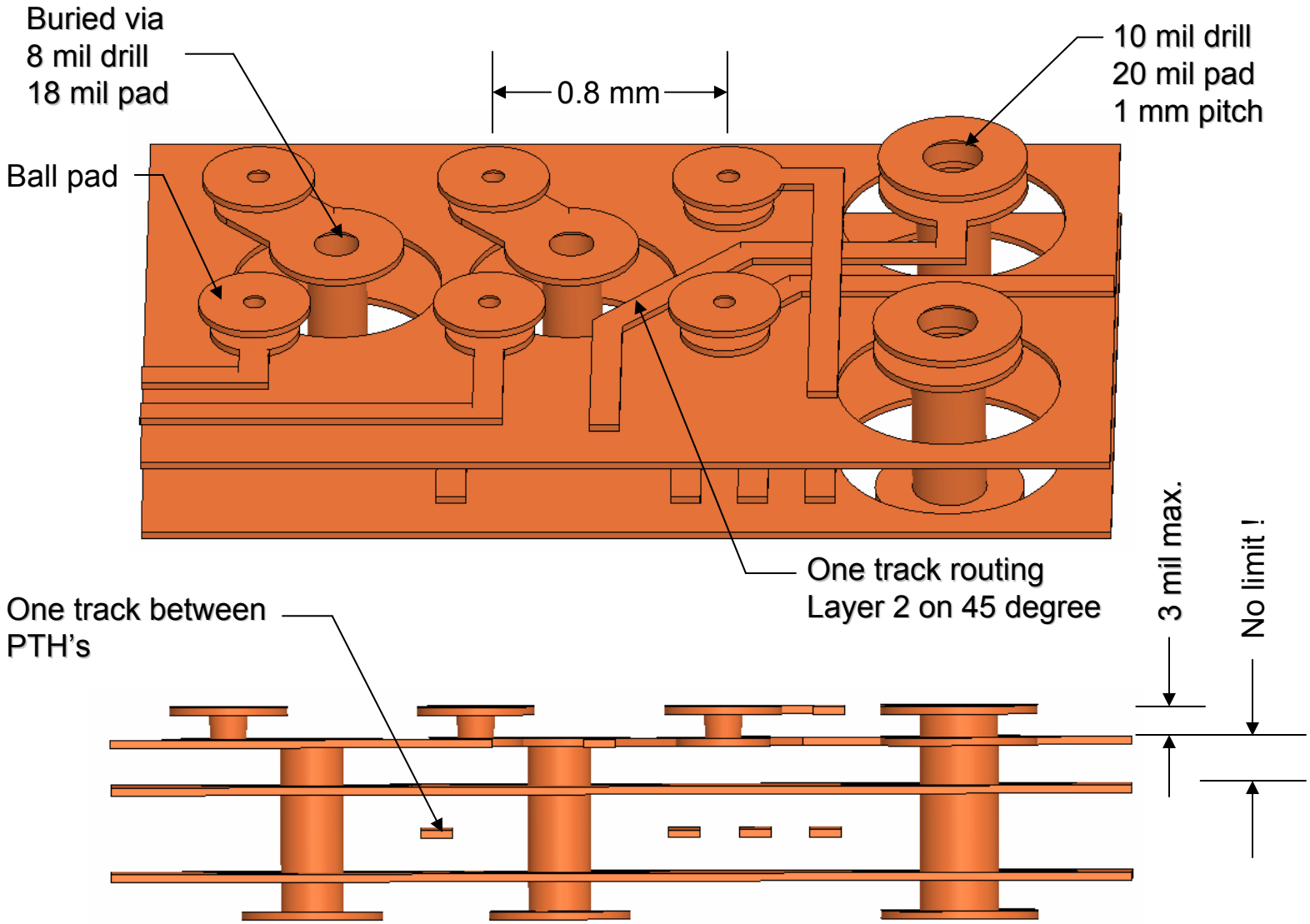
# Laser Drilling Technology





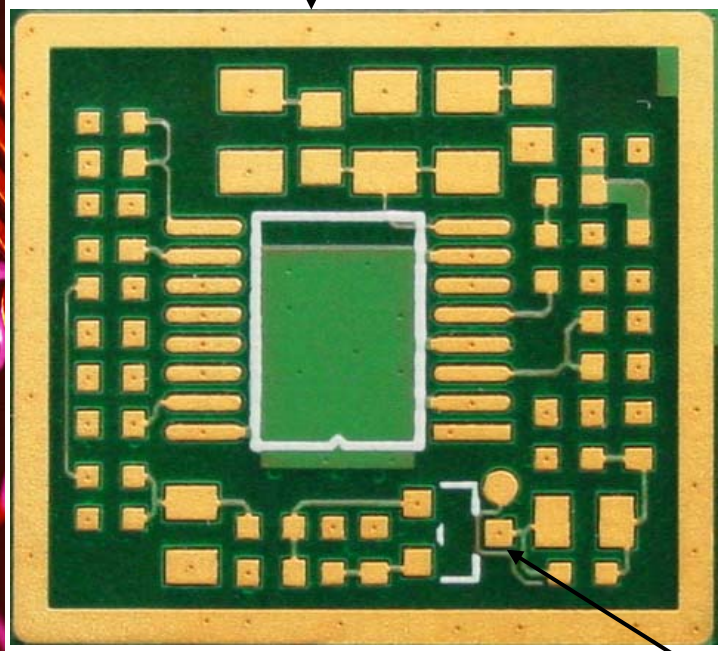
# Microvia Through Hole & Buried Combo 0.8 mm

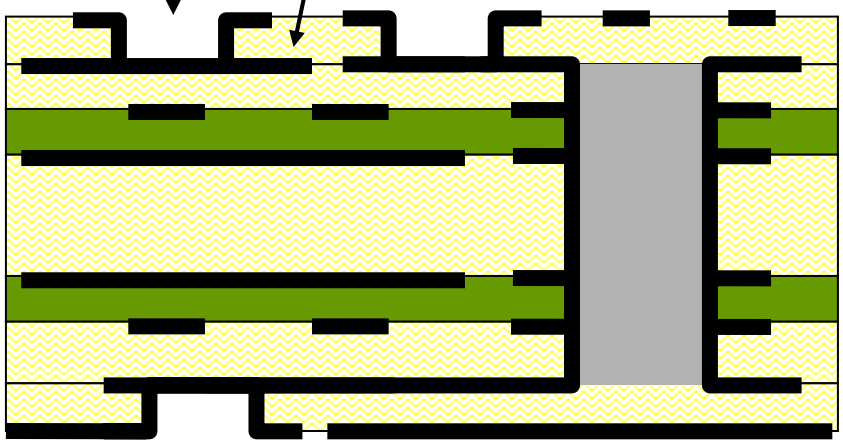
Enabling Technologies



# Microvia Applications For Power and Ground

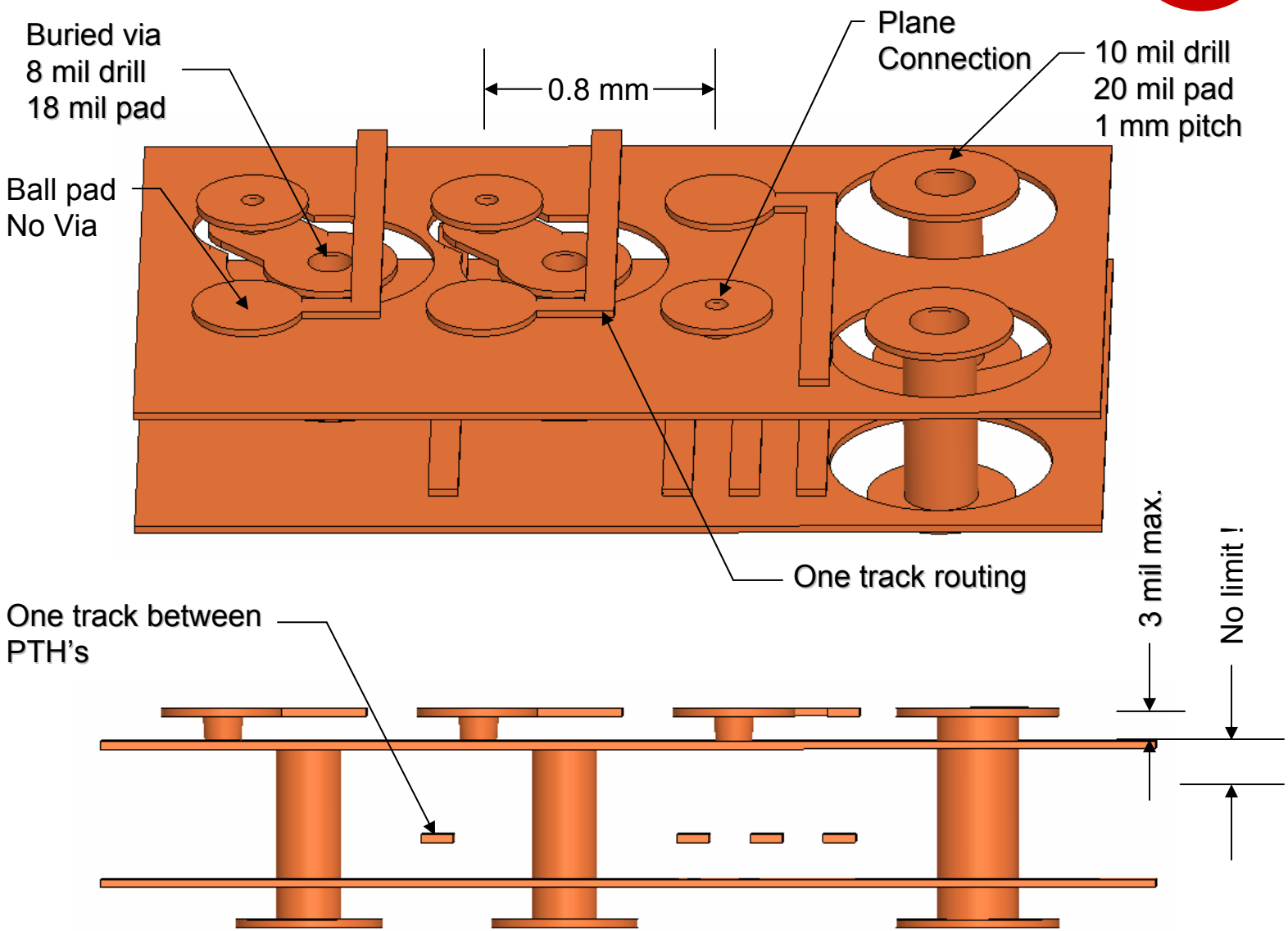






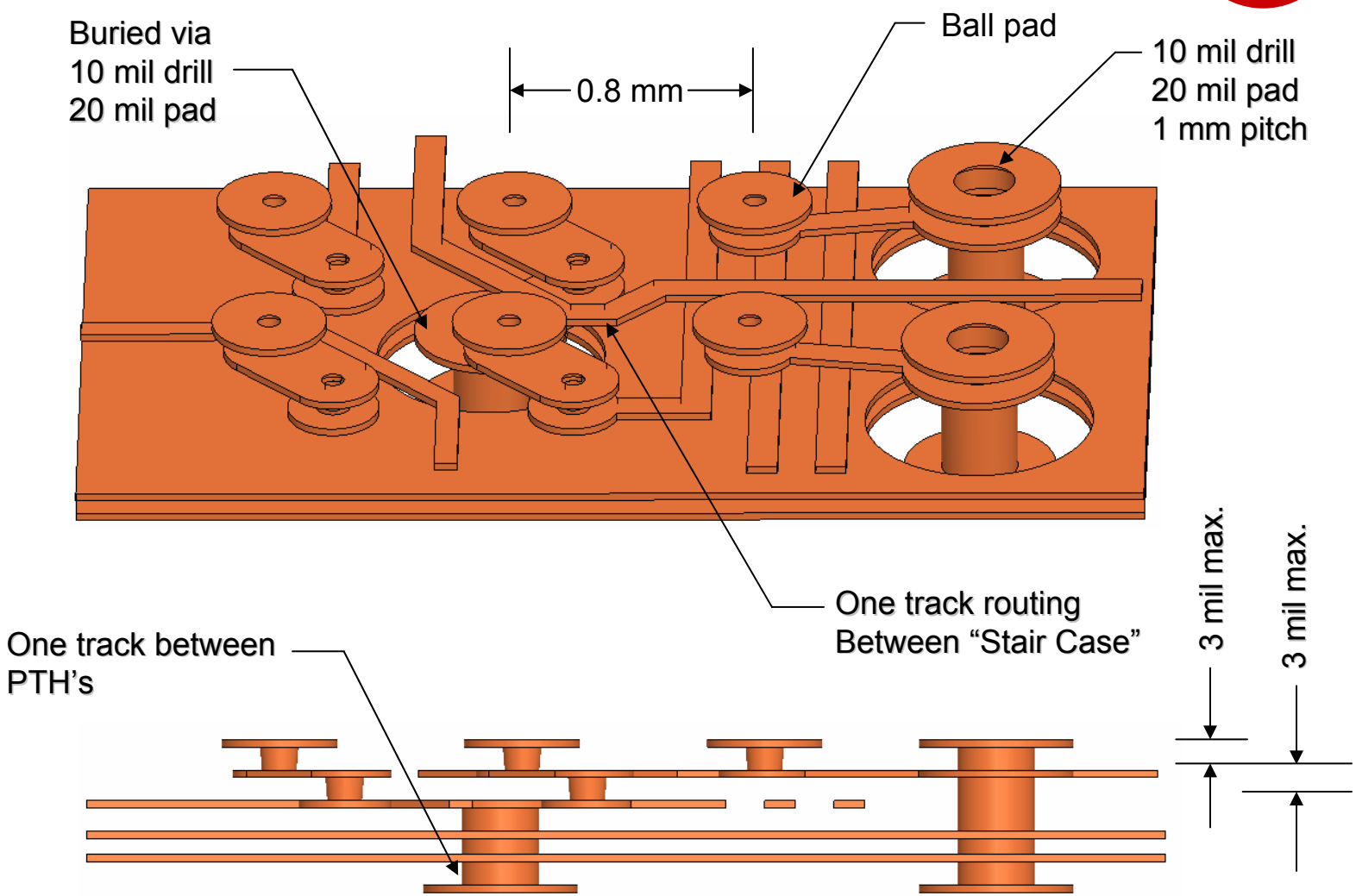
# Microvia Through Hole & Buried Combo 0.8 mm

Enabling Technologies



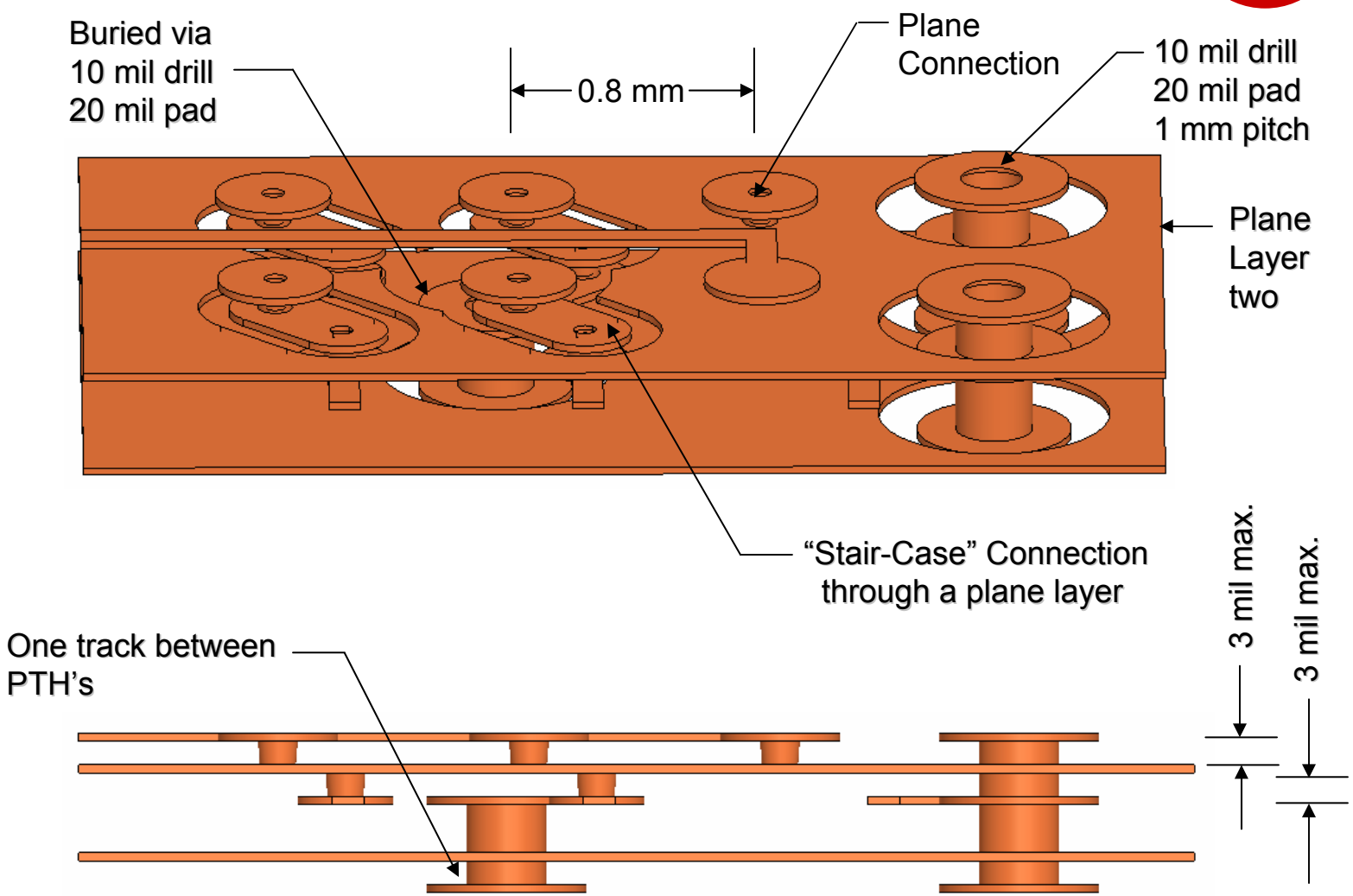
# Microvia "Stair Case" & Buried Combo 0.8 mm





# Microvia "Stair Case" & Buried Combo 0.8 mm



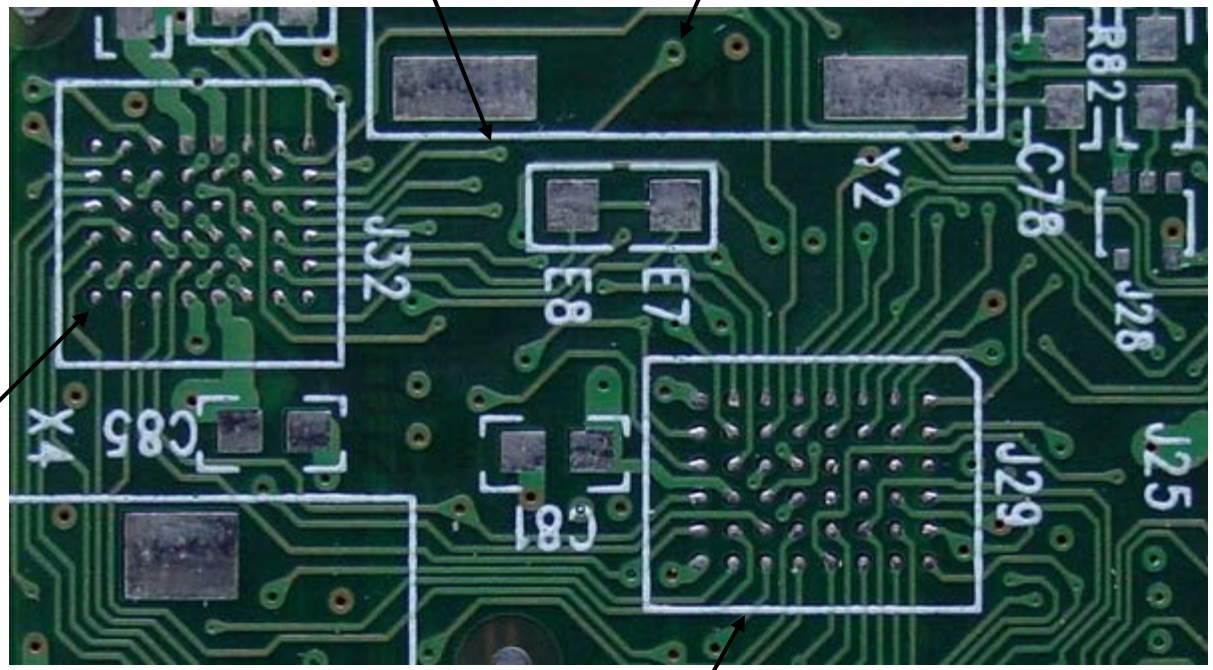


# Dynamic Details, Inc.

## Laser Drilling Technology

Laser drilled via's

Mechanically drilled via



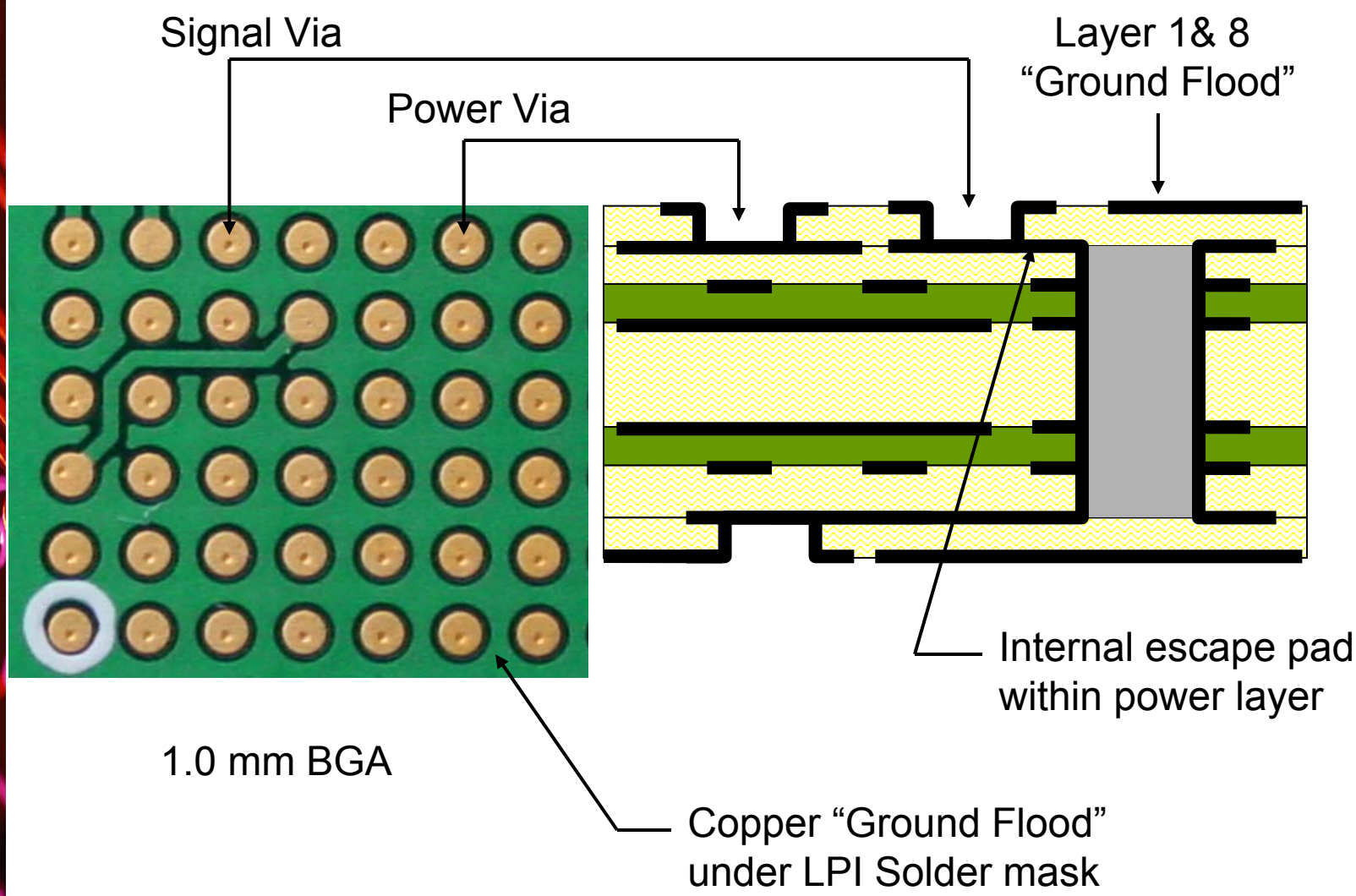

0.8 mm BGA

0.8 mm BGA

Tin/Lead Surface Finish

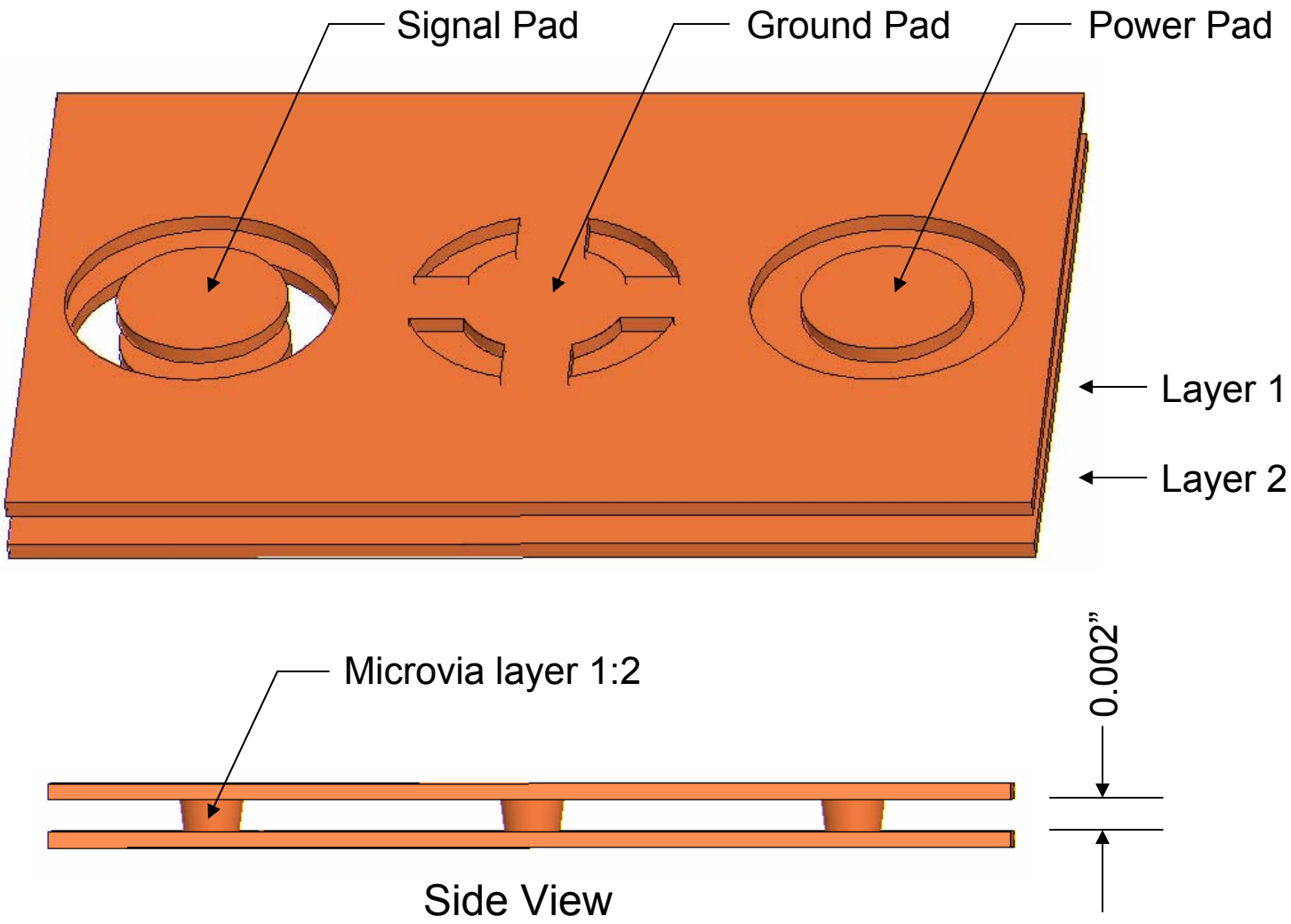
# Using Microvia's For Power & Ground





# Microvia Geometry (Surface Power And Ground)

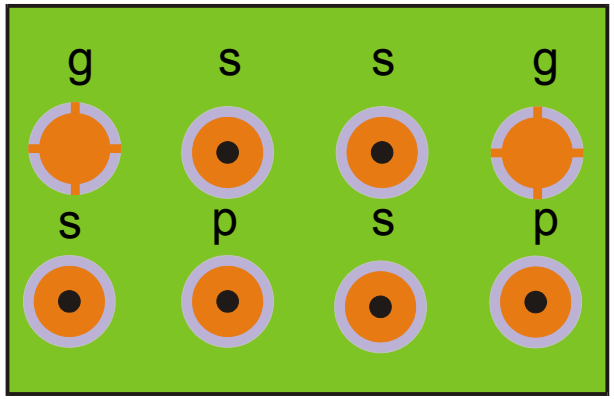




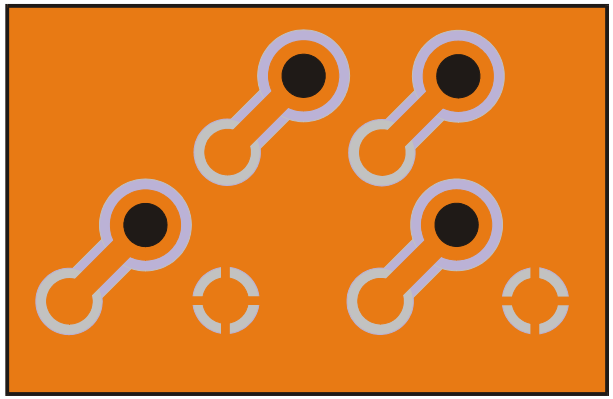
# Using Microvia's For Power & Ground



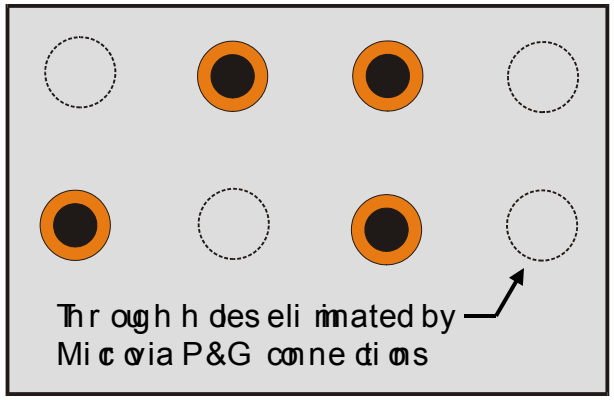
Layer 1: Ground



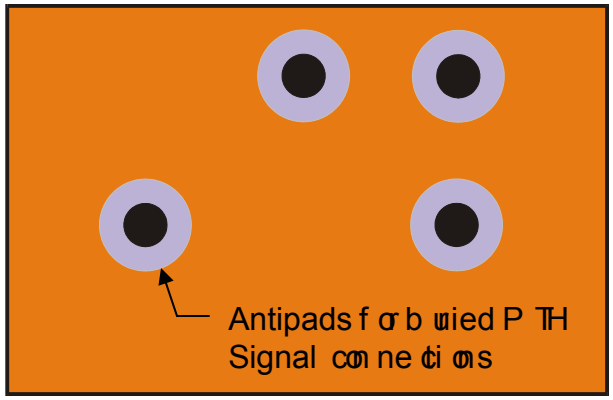

Layer 2: Power



Layer 3: Signal



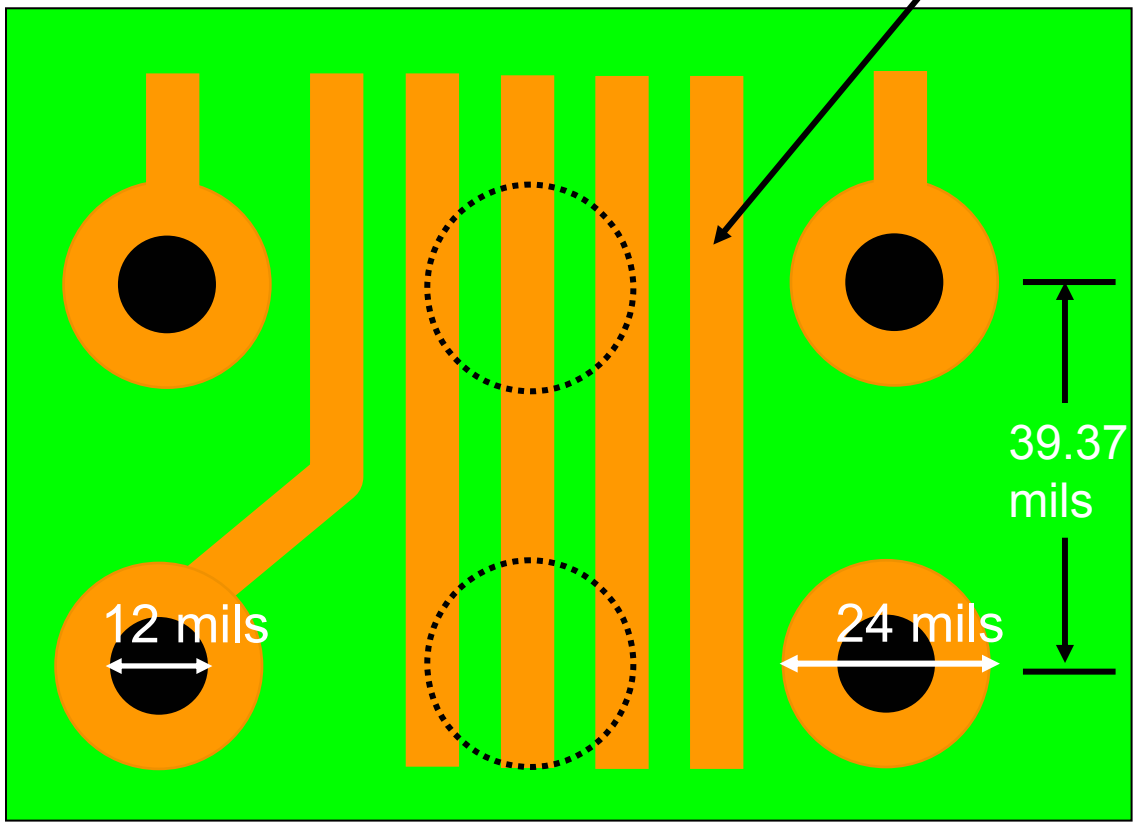

Layer 4: Ground



# Increased Density: Microvia's Replace PTH P&G



5 channels at 5/5 line/space or
6 channels at 4/4.5 lines/space




Microvia's used on External power and ground layers eliminate through holes and double
the effective pitch

# Dynamic Details, Inc.

Enabling Technologies

## Overview

- Technology Drivers
- Advanced Materials
- Characterized FR-4
- Hybrid Constructions
- Laser Direct Imaging
- High Aspect Ratio Copper Plating
- Laser Drilling
- Planar Via Technologies

# Laser Drilling Technology Via In Pad



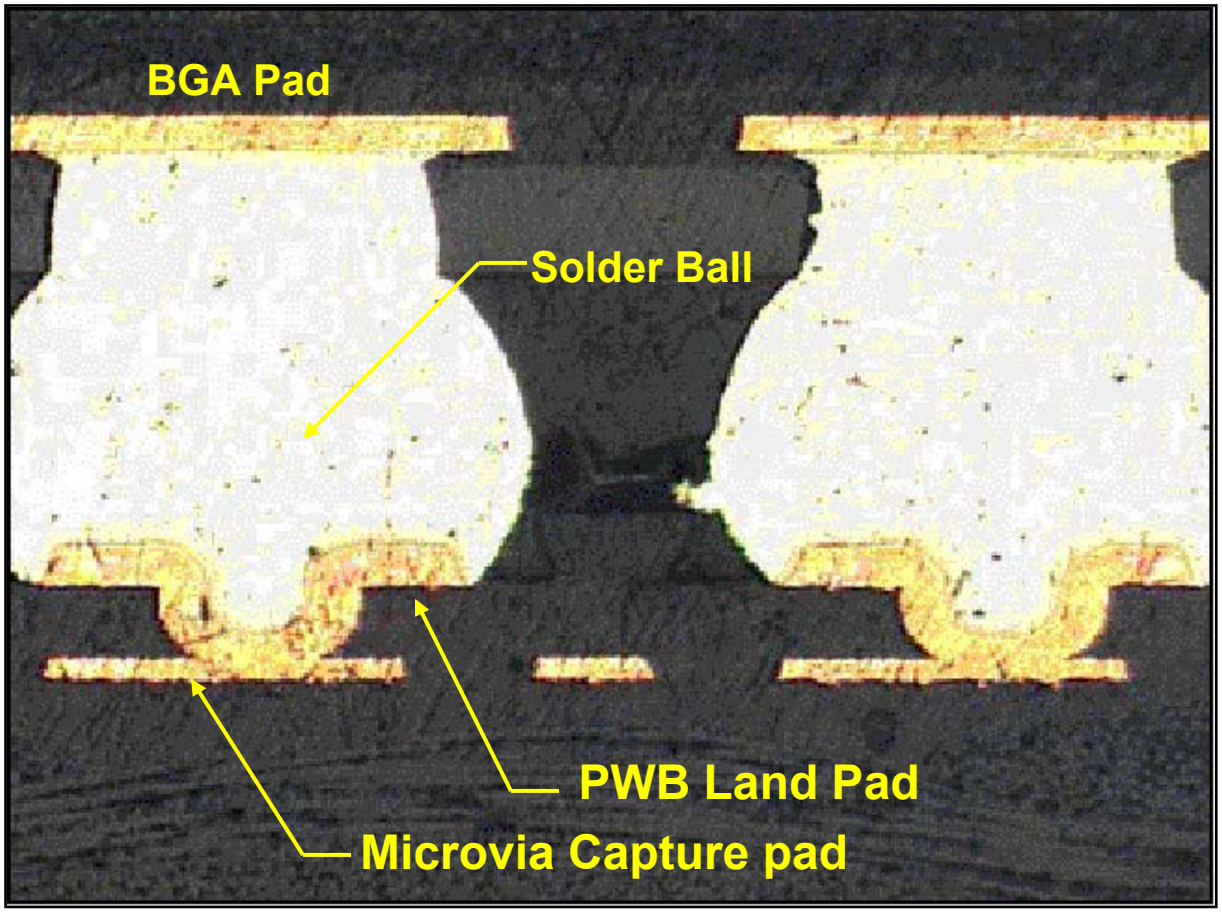
## Potential Assembly Issues With Via In Pad:

- Microvias vias in pad from layer 1 to 2 must have minimum volume after plating to prevent and or minimize solder voiding due to trapped volatiles
- Even with minimum microvia volume an optimized solder profile is often necessary
- Microvia diameters for connecting layer 1 to 3 or greater are in all cased too large for via in pad
- Potential joint reliability issue with large ceramic devices with via in pad when no escape pattern is used “Dog Bone” due to large CTE mismatch to the organic substrate

# Laser Drilling Technology Via In Pad



## Ideal Solder Joint

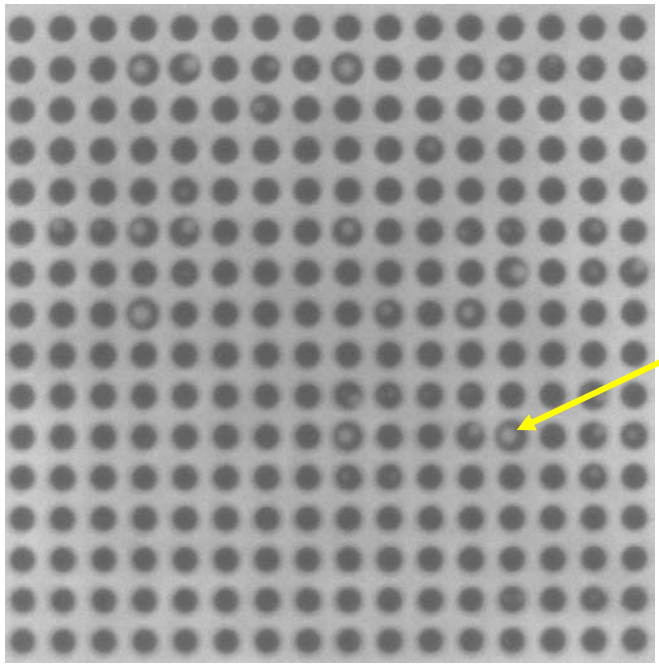


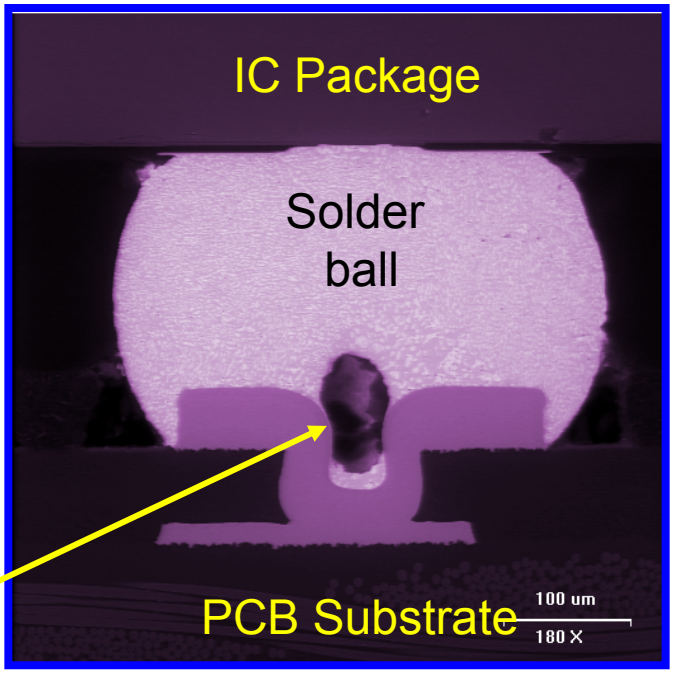

Chip Scale BGA Package with Microvia in Pad

# Laser Drilling Technology Via In Pad



X-Ray of BGA site



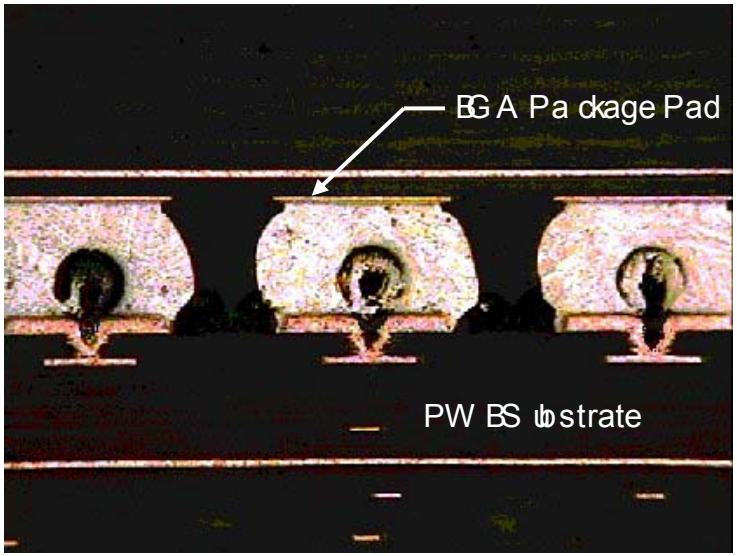


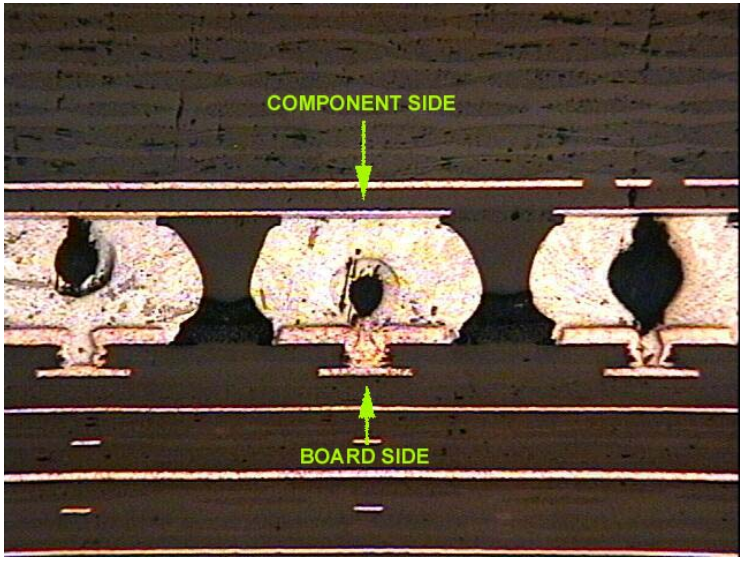

Solder void within a solder ball at via in pad location

# Laser Drilling Technology Via In Pad



## Unacceptable Via In Pad Solder Joints



# DDI Planar Via Technologies”



## Technology Drivers For Planar Via-In-Pad:

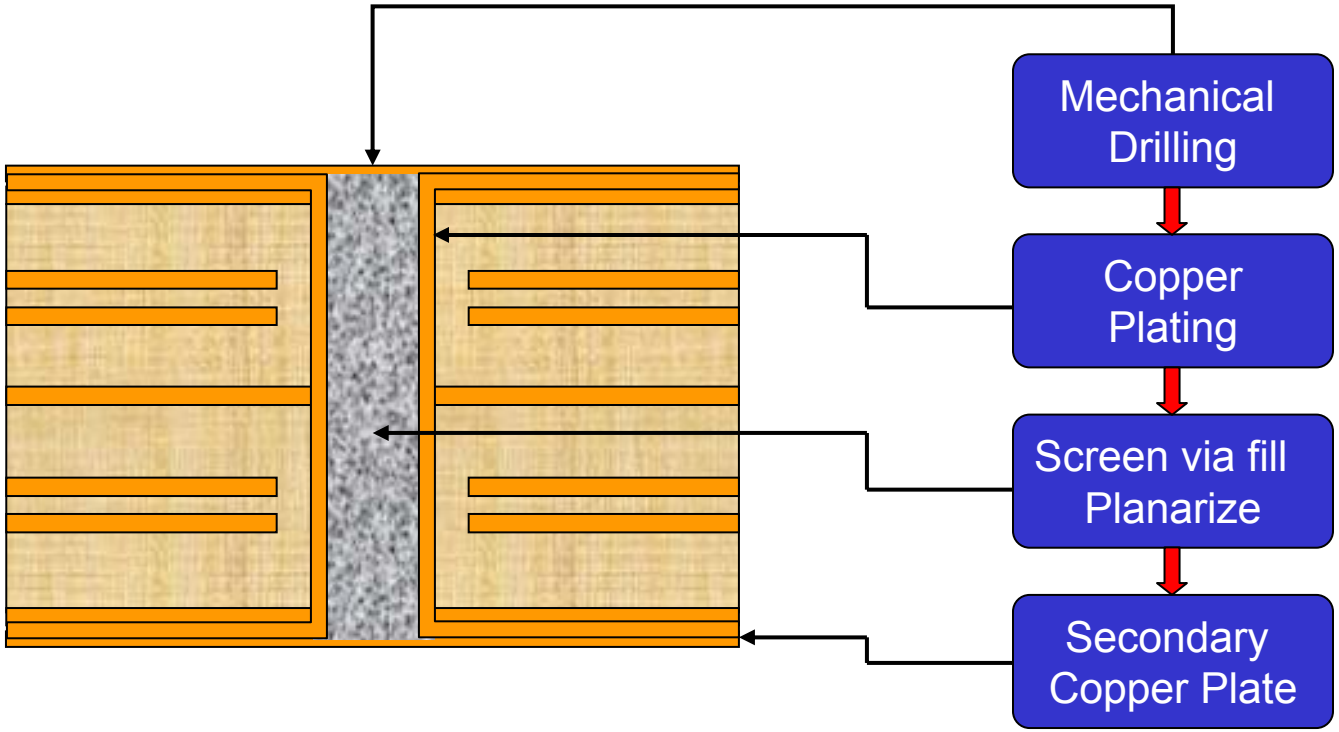
- Eliminate potential solder voiding in Via-In-Pad applications
- Address Via-In-Pad applications for multilayer HDI structures (i.e. 1:3, 1:4 ? connections) while maintaining low aspect ratio plating
- High capacitance low inductance HDI power structures
- Via-In-Pad capability with RF laminates greater than 0.002” thick
- Effective use of embedded resistors on HDI layers

- Process Technologies
  - PTH Conductive fill and Cu plate
  - PTH Non-Conductive fill and plate
  - Planar Cu fill microvia
  - Planar Cu fill Stacked MicroVia “SMV”

# VIA Fill For Plated Through Holes



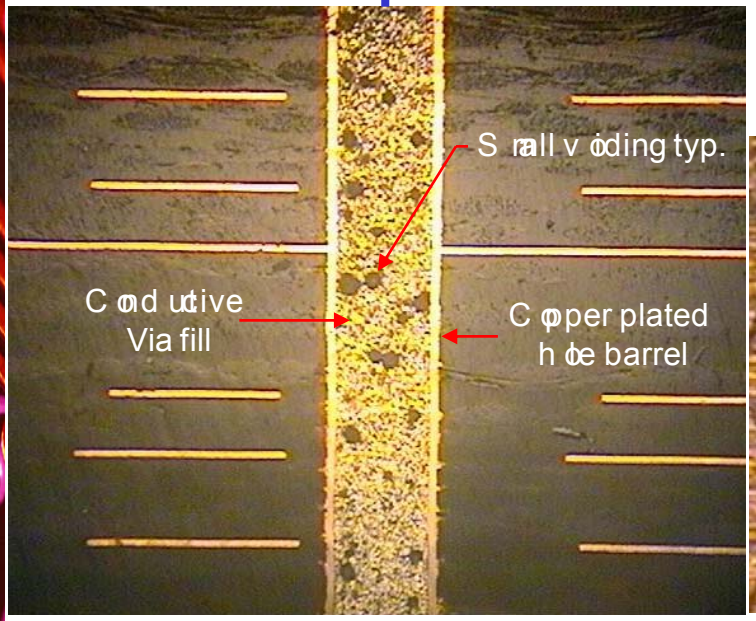
Via Filling Process



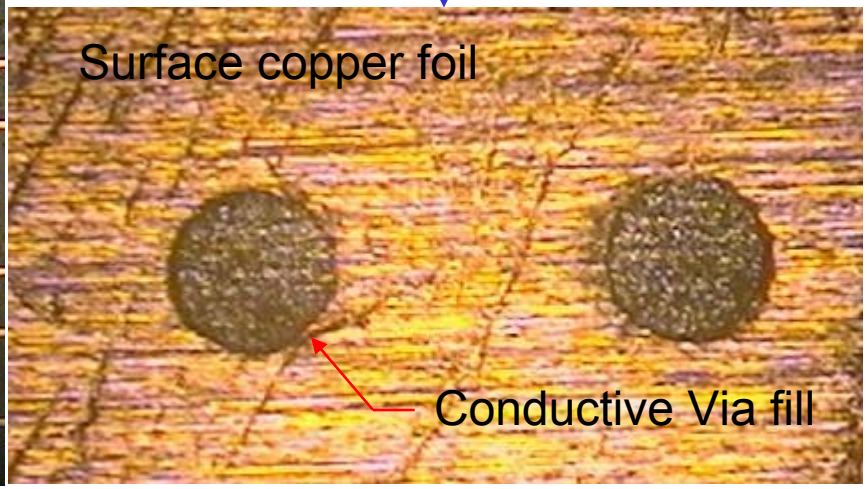

- Dupont CB100 Conductive via fill (sliver filler)
- Taiyo TR7901 Conductive via fill (silver filler)
- Methode 1210 Conductive via fill (silver filler)

# Dynamic Details, Inc.

## Conductive Via Fill For PTH




Cross-section with conductive via fill (Taiyo TR7901 Silver filled)

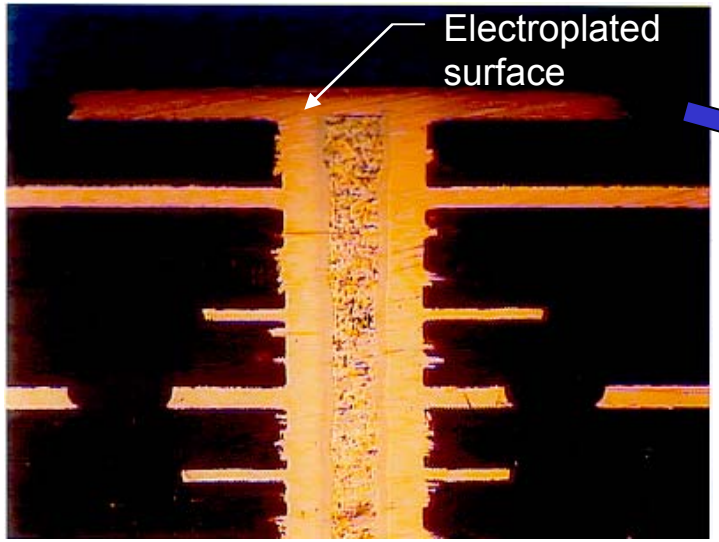



Surface view (X,Y) after via filling and before Cu plating

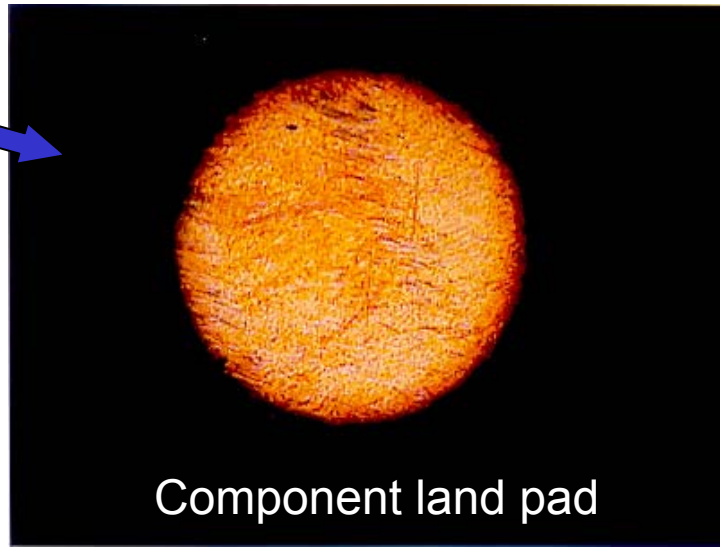
# Conductive Via Fill For PTH



Cross-Section




View of surface




CB-100 Conductive via fill

# DDI Stacked Microvia's "SMV"



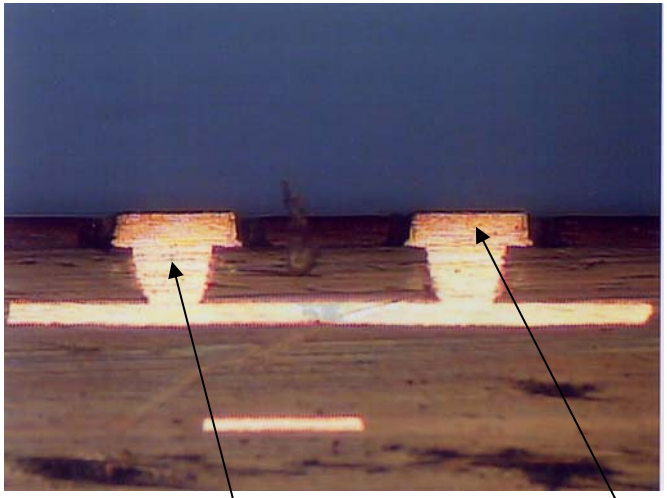
## Stacked Microvia's Attributes:

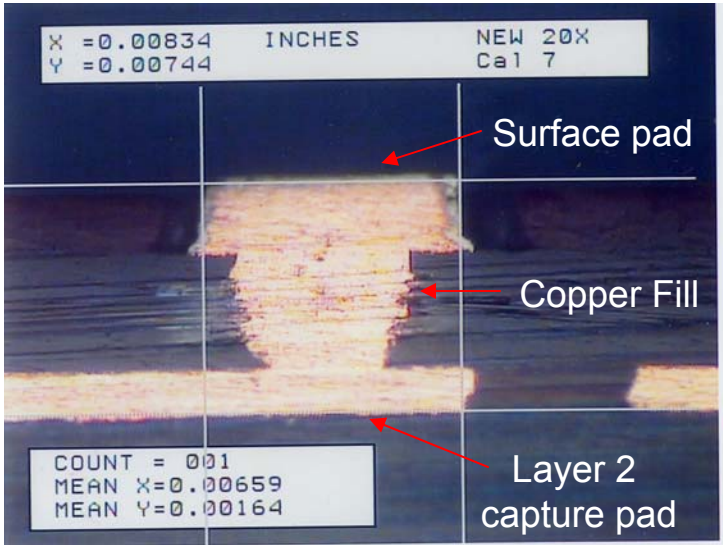
- Provides a solid copper fill eliminating potential solder voiding
- Improved assembly for Chip Scale components
- Improves routing density for Fine Pitch BGAs (0.65 mm & 0.5 mm)
- Allows routing out on multiple layers with 0.010" Pad diameters
- Maximize copper on plane layers
- Lower inductance when compared to "staircase" and offset via's

# Dynamic Details, Inc.

## Laser Drilled Via's: Plated Cu Fill

Laser drilled via's with Cu plate fill





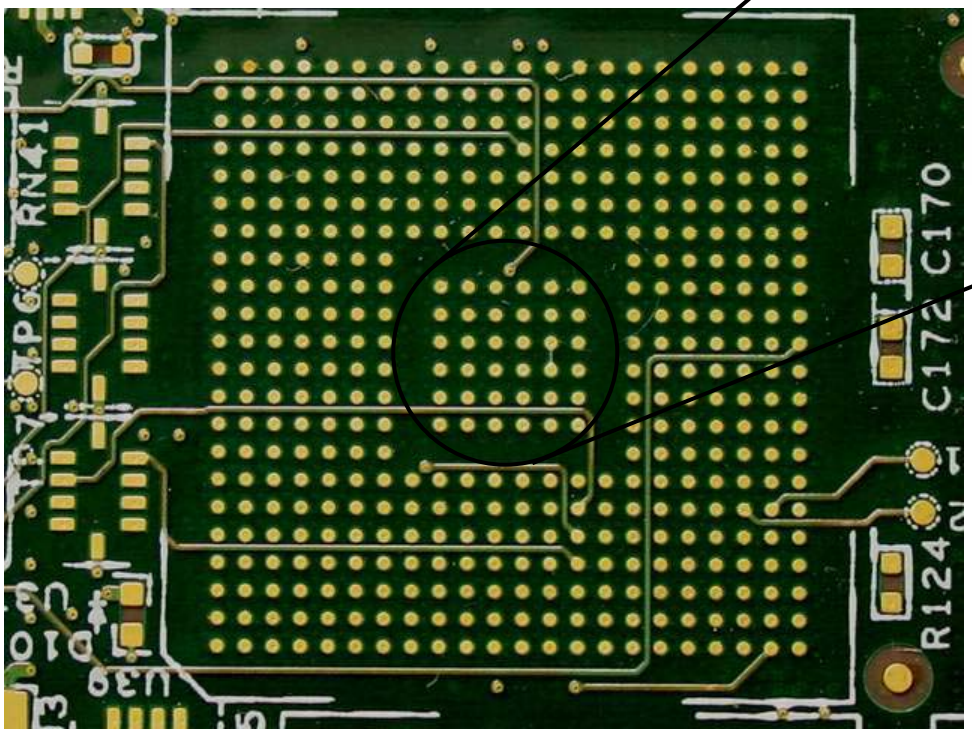

0.008" diameter surface pad

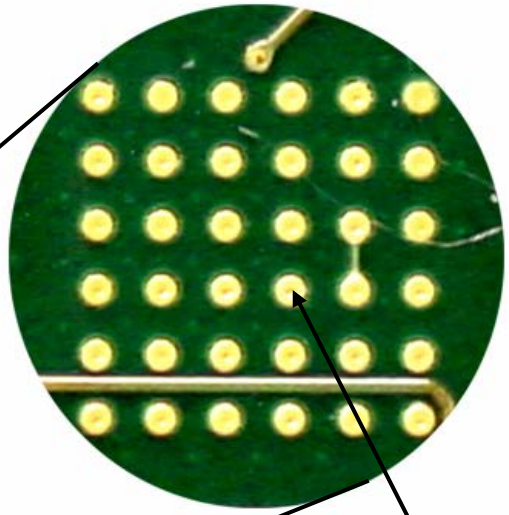
0.004" laser drilled via with Cu plate fill

# Laser Drilled Via's: Plated Cu Fill



BGA Land pads with planar copper surface & Immersion Nickel Gold



Planar Surface for 0.8 mm BGA

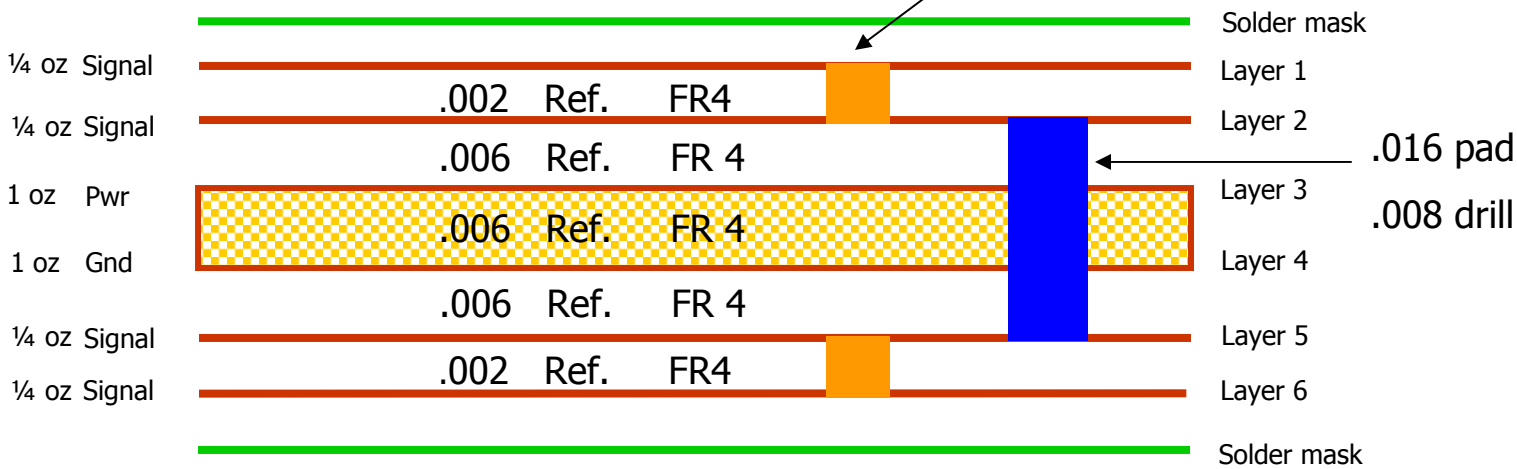
# Applications For Planar Cu filled Via's

Enabling Technologies

## 1 + 4 + 1: 0.4 mm Flip Chip Application

Microvia Technology with Planar Cu Fill
.002" trace & space
Laser Direct Image (LDI)

.004 Laser drill
Plate Fill
0.5:1 aspect ratio
L1 = .008 Pad
L2 & 5 = .010 Pad

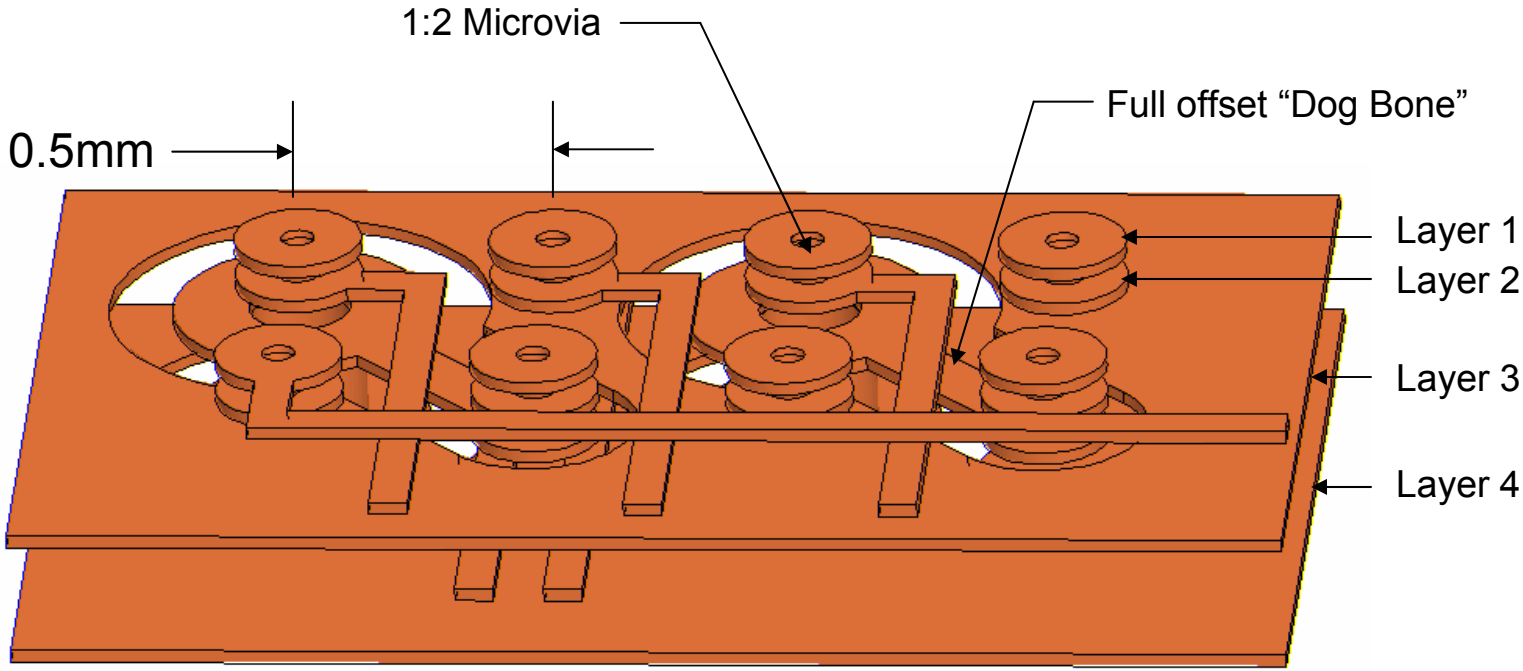


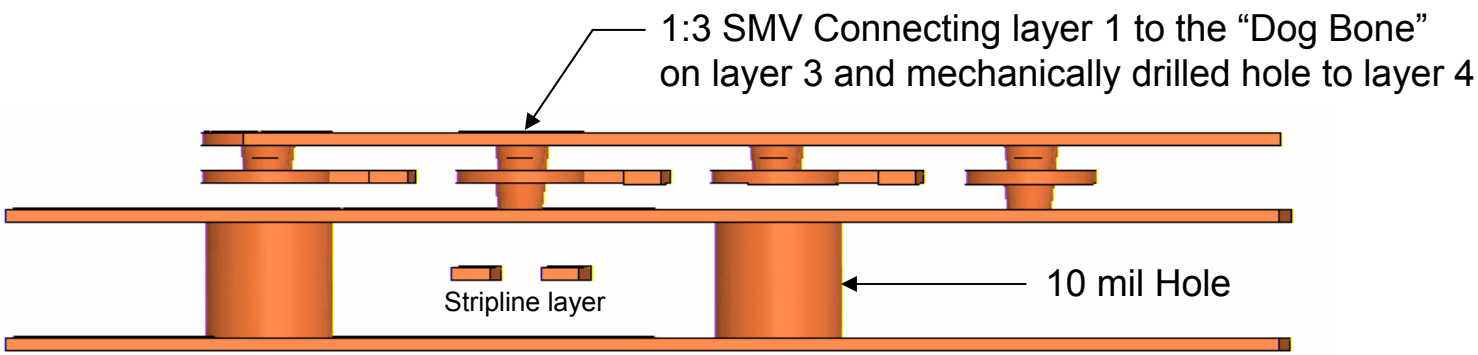

Finish Thickness = .036 +/- .003
Material N4000-13 Tg 210° C

Solder mask clearance for Flip Chip Area .001/side
Utilize Laser Direct Image (LDI) Solder mask

# SMV Geometry (Offset Buried Via)





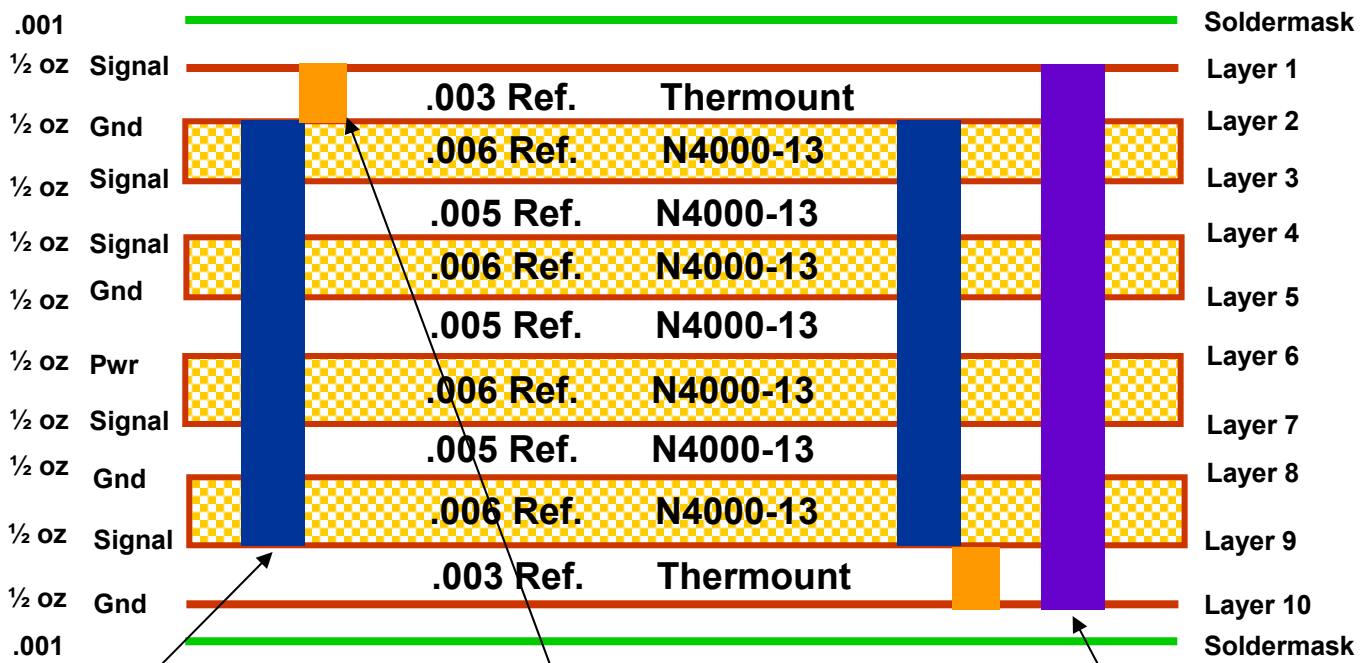




Side View

# Applications For Planar Cu filled Via's



1-8-1: Offset laser drilled via over conductive filled buried via's




Layer 2 - 9 = Buried Vias
0.020" pad & 0.010" drill
Conductive Via Fill

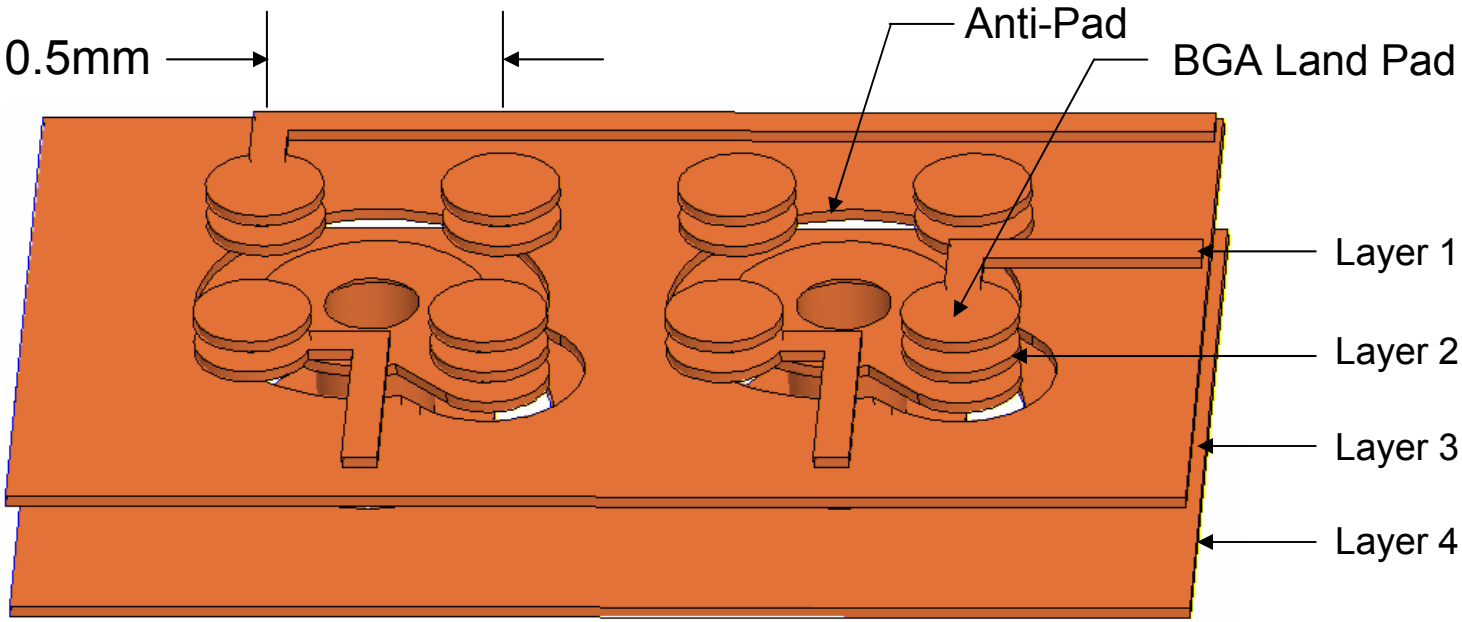
Layer 1 - 2 & 9 – 10
Microvias L1 & 10 = 0.010"
pad 0.006" laser drill

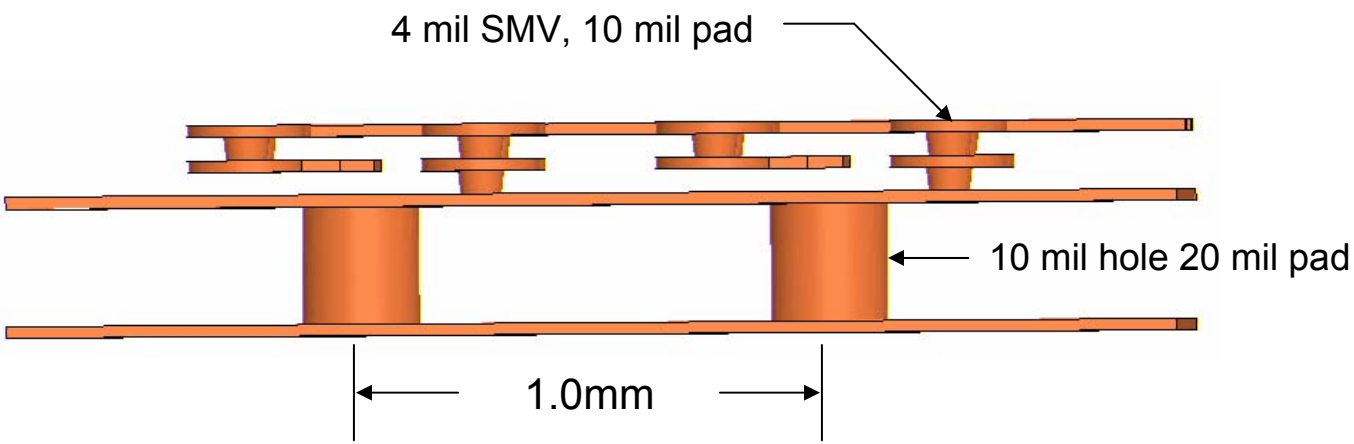
Layer 1 - 10 through Vias
0.020" pad & .010" drill

Layer 1 & 2 - 9 & 10 3/8 oz copper if trace and space <0.004"

# SMV Geometry (Minimum Offset)



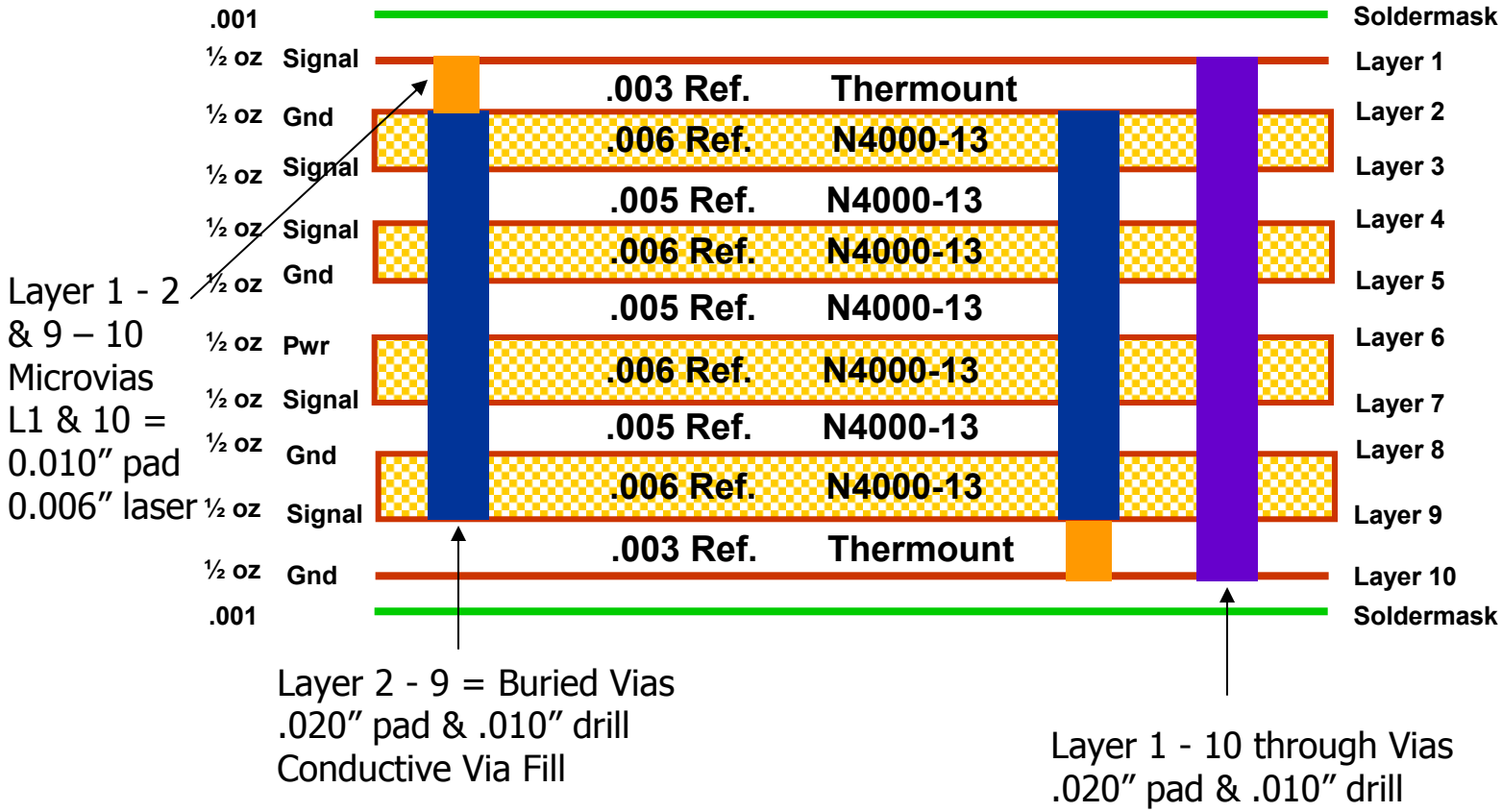


# Applications For Planar Cu filled Via's



1-8-1: Laser drilled via over conductive filled buried via's




Layer 1 - 2 & 9 – 10 Microvias
L1 & 10 = 0.010" pad
0.006" laser

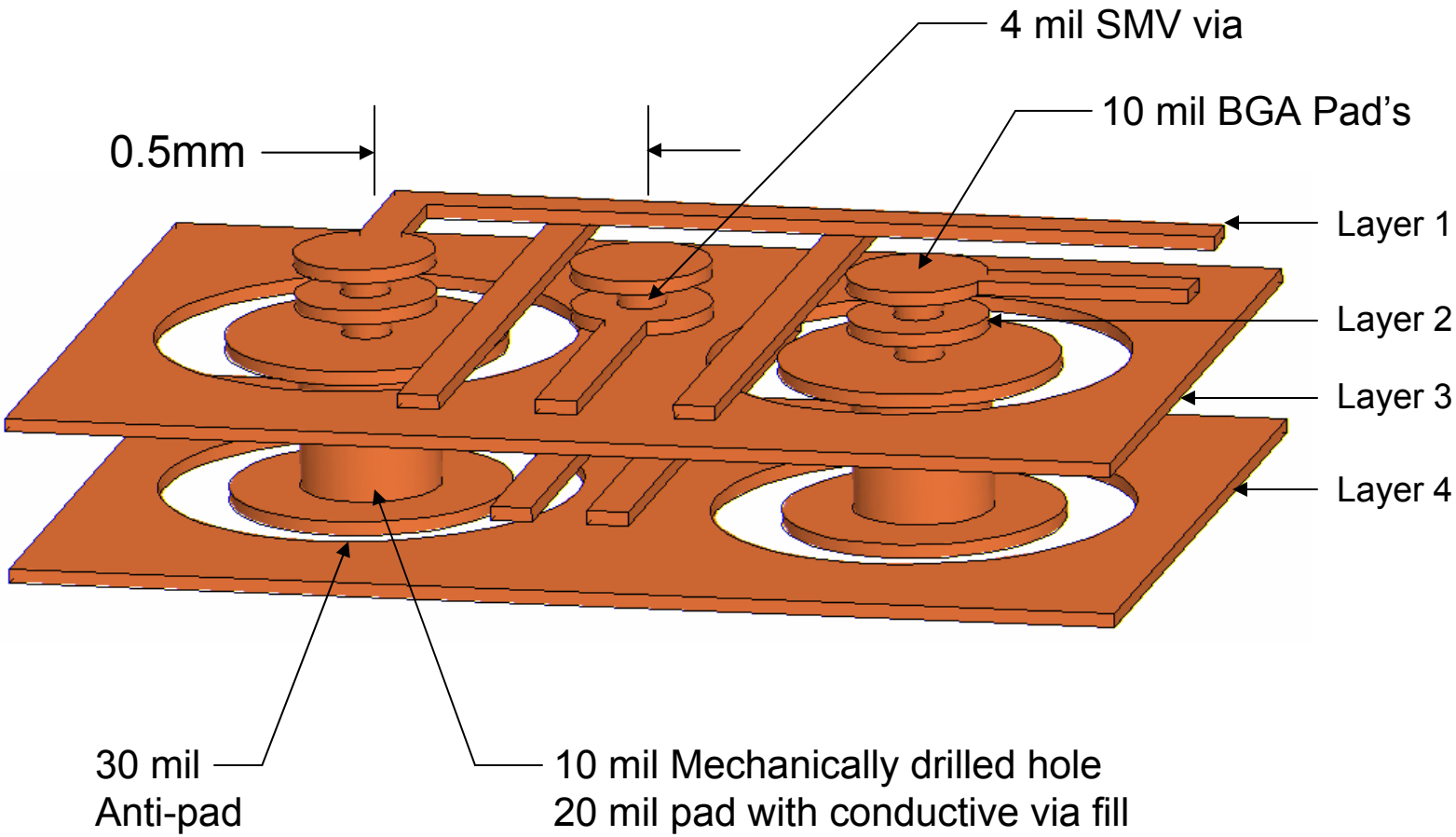
Layer 2 - 9 = Buried Vias
.020" pad & .010" drill
Conductive Via Fill

Layer 1 - 10 through Vias
.020" pad & .010" drill

Layer 1 & 2 - 9 & 10
3/8 oz copper if trace and space <.004"

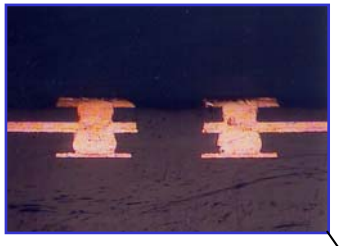
# SMV Geometry (Conductive Via Fill And Plate)





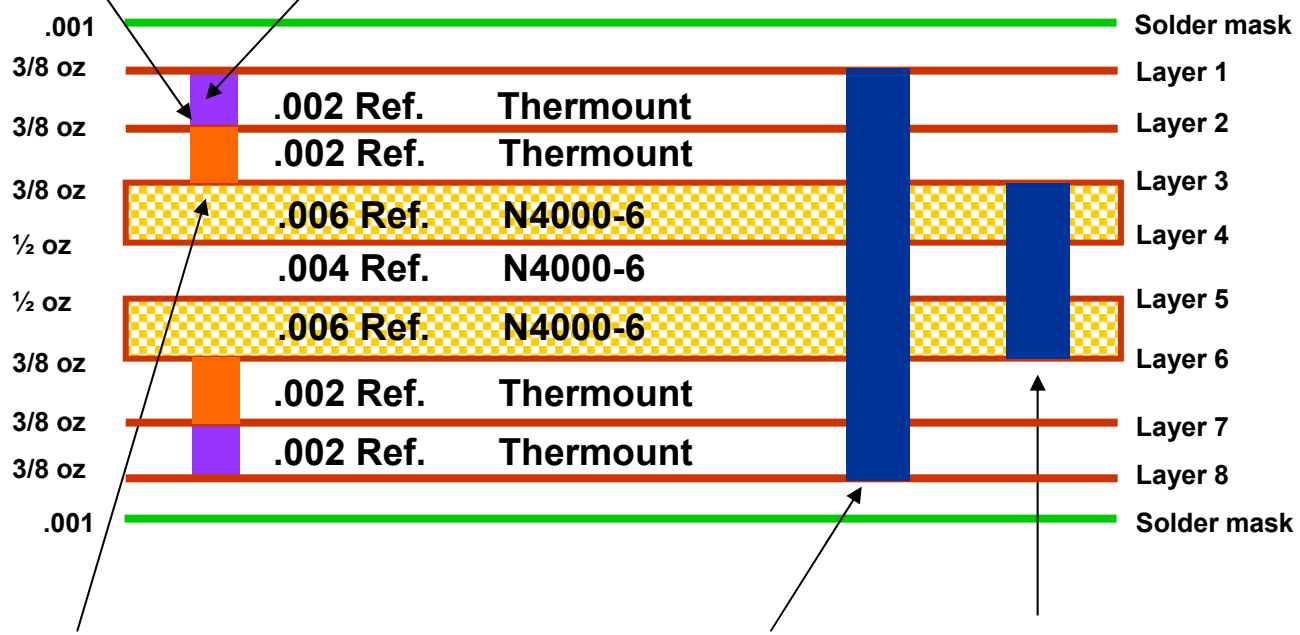
# Applications For SMV Technology





## 2-4-2: Stacked microvia using planar Cu fill

Layer 1 - 2 & 8-7 = Microvias
L1 .010" pad & .004" laser drill




Layer 2 – 3 & 6 - 7 = Microvias
0.010" pad & 0.004" laser drill

Layer 1 - 8 = Through-hole
0.022" pad & 0.012" drill

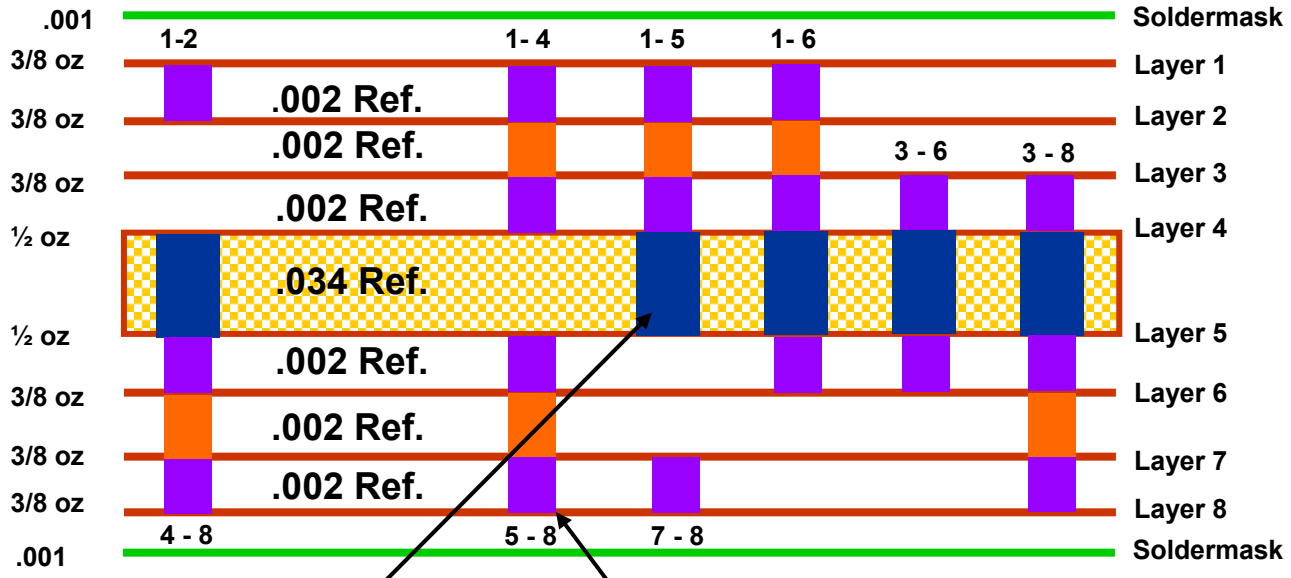
Layer 3 - 6 = Buried Vias
0.022" pad & 0.010" drill

Buried via holes to be filled with non-conductive epoxy

# Applications For SMV Technology



## 3-2-3: Stacked Planar Cu Filled Via's



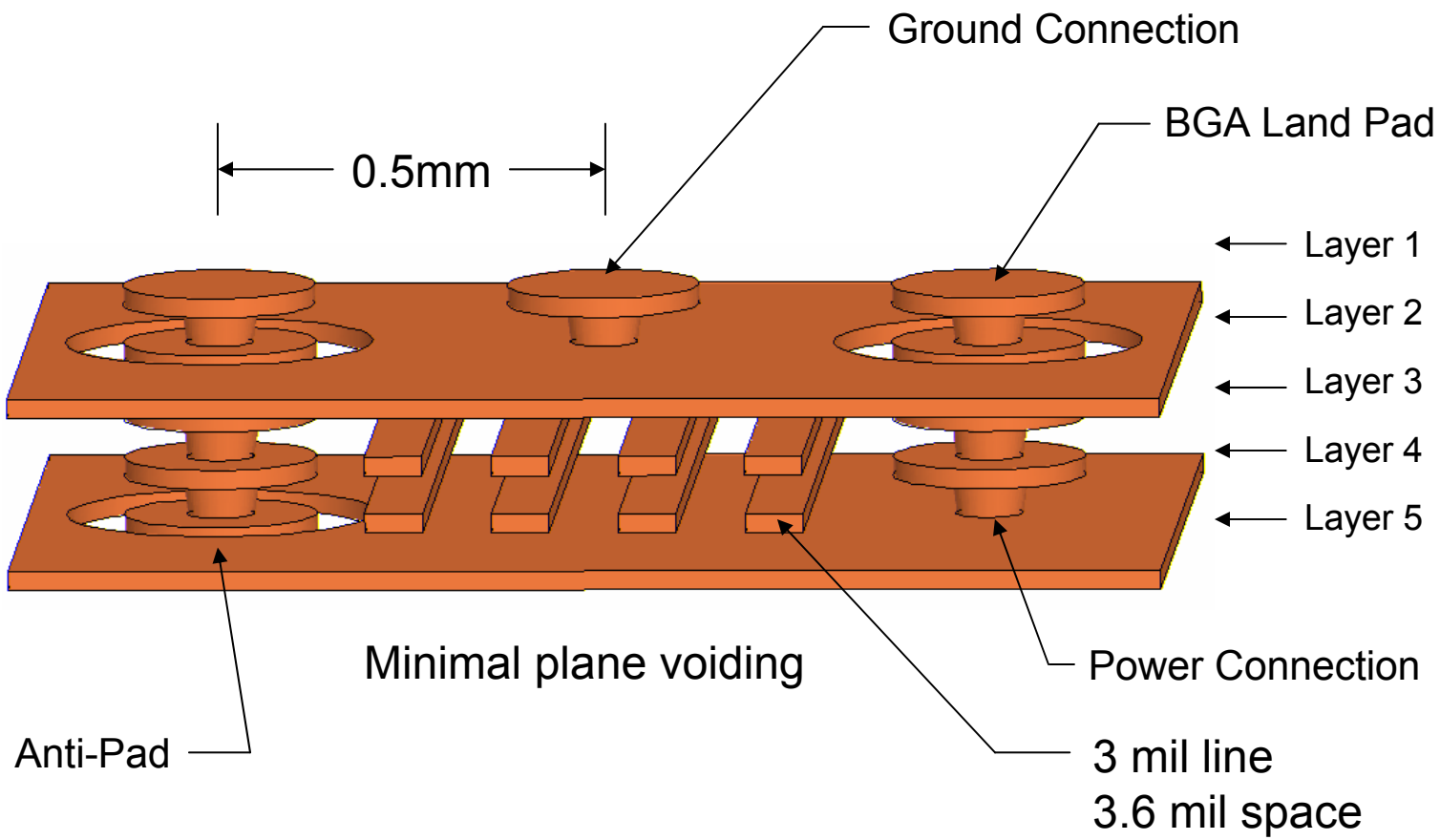

Layer 4 – 5 buried via
0.016" pad &0 .008" drill
Conductive Fill
Planar & Plate

Stacked Microvias
Laser drilled 0.004"
0.008" pad
Plate – Filled

Finish Thickness = 0.062 +/- 0.005 Material = Nelco N4000-6FC 175° C Tg

# SMV Geometry (Multilayer signaling)

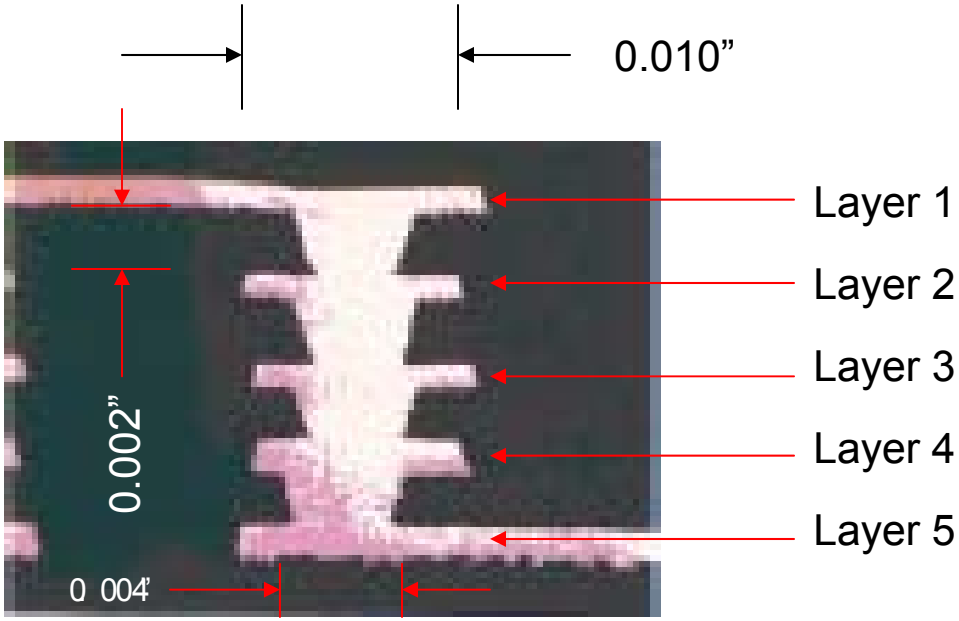




# Applications For SMV Technology



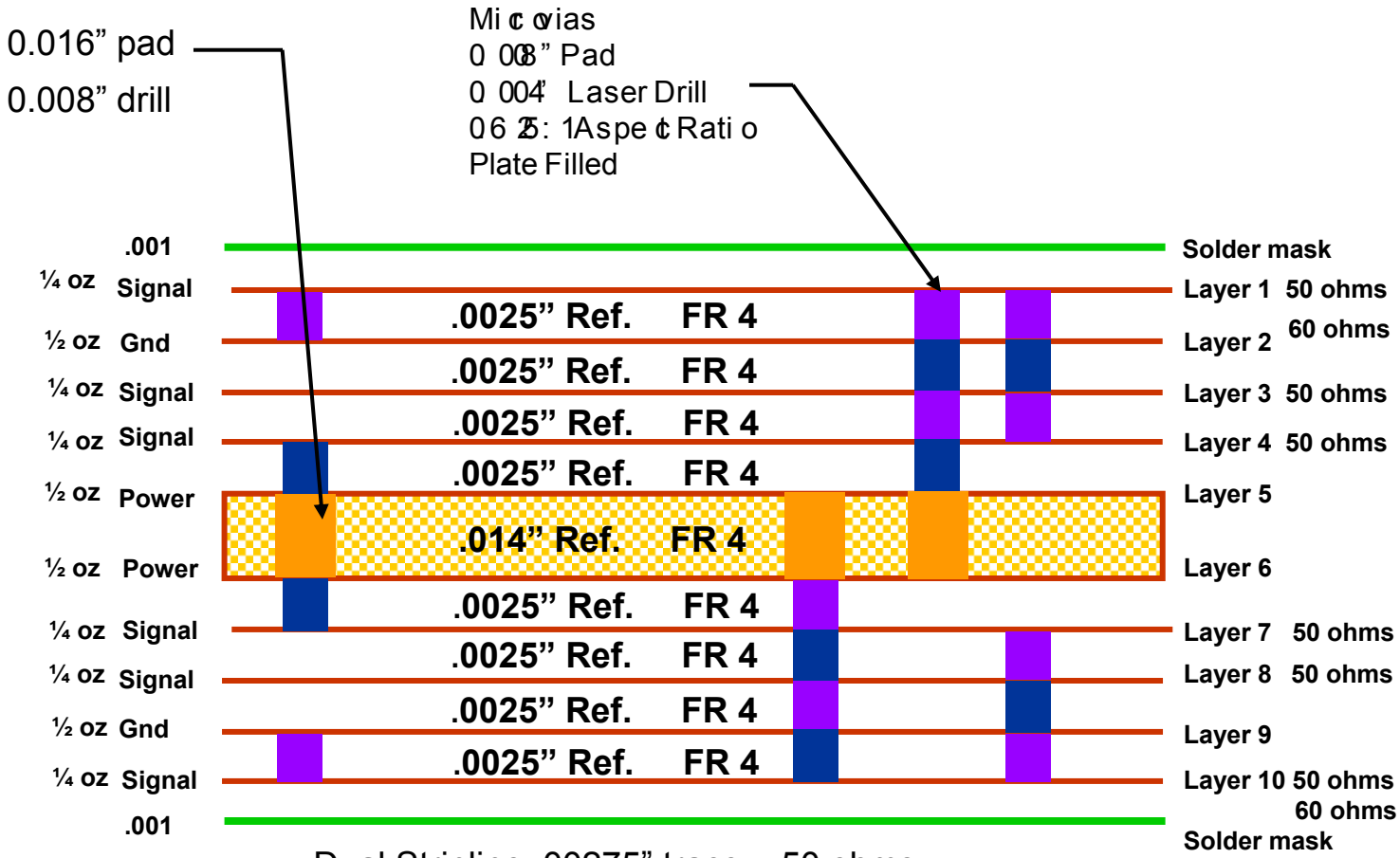
## +4 Stacked Microvia Construction




Vertical stacked via’s access 5 interconnect layers

# Dynamic Details, Inc.

## Applications For SMV Technology




Dual Stripline .00275" trace = 50 ohms

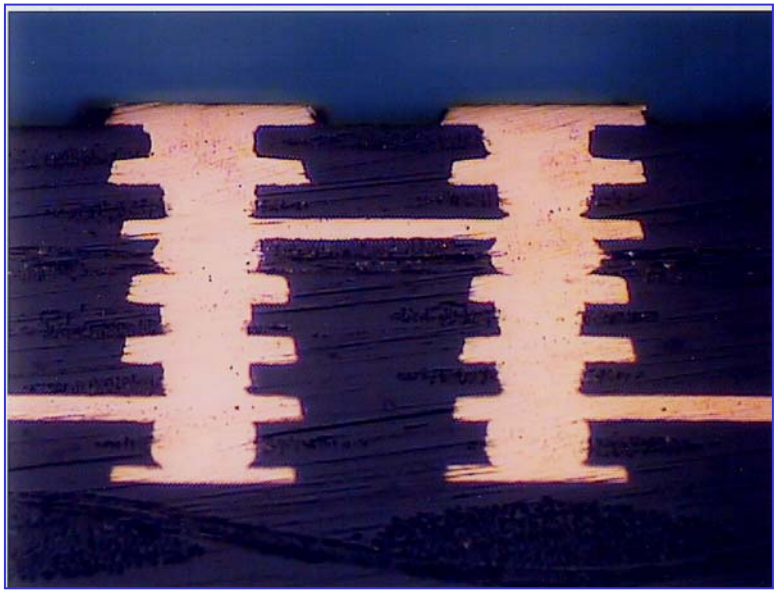
Coated Microstrip 0.0025" trace = 60 ohms

0.004" trace = 50 ohms

Finish Thickness = 0.065 0+/- 0.005 Material = High Performance FR 4 210° C Tg

# Applications For SMV Technology





- Seven layers for fan-out of 0.65 mm, 0.5 mm & 0.4mm BGAs
- 0.5 mm = .010” diameter pad using a .004” laser drill, 0.003” trace & 0.0033 space
- 0.008” diameter pad using .004” laser drill is also available
- 0.4 mm = .008” diameter pad, .004” laser drill, .0026” trace & space

Capable of creating a 14 Layer stacked configuration

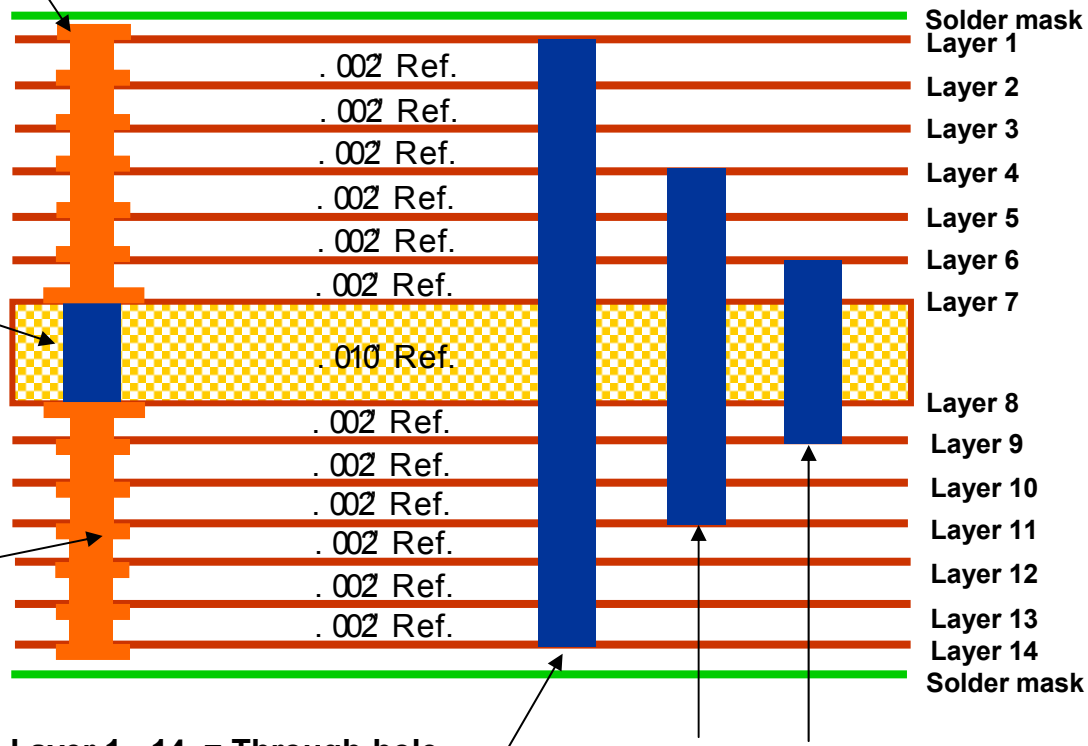
# Applications For SMV Technology

Enabling Technologies

**Stacked Microvias**
**Layer 1 - 2**
**Layer 2 - 3**
**Layer 3 - 4**
**Layer 4 – 5**
**Layer 5 – 6**
**Layer 6 - 7**
**0.010” pad**
**0.004” laser drill**

**Buried Vias**
**Layer 7- 8**
**0.016” pad**
**0.006” drill**
**Fill with**
**conductive epoxy**

**Stacked Microvias**
**Layer 9 - 8**
**Layer 10 - 9**
**Layer 11 - 10**
**Layer 12 – 11**
**Layer 13 – 12**
**Layer 14 - 13**
**0.010” pad**
**0.004” laser drill**




**Layer 1 - 14 = Through-hole**
**0.020” pad & 0.010” drill**

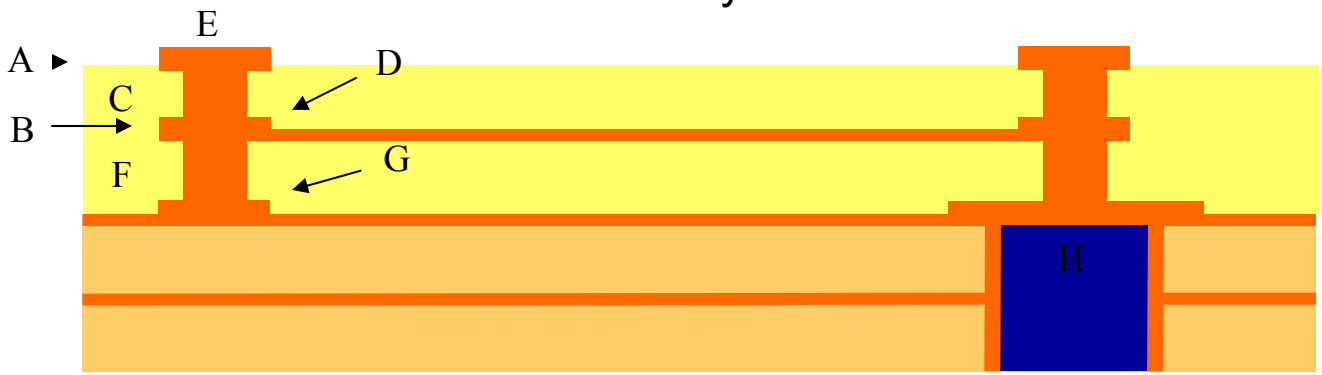
**Layer 4 - 11 = Buried Vias**
**Layer 6 – 9 = Buried Vias**
**0.022” pad & 0.010” drill**

Finish Thickness = .062” +/- .006”
Material = High Temperature FR4 175° C Tg

# SMV Design Rules

Enabling Technologies

## Laser Drilled SMV Layer 1 to 2 & 2 - 3




Gil White 5/04

| # | Description | Standard SMV | | Advanced SMV | |
|---|---|---|---|---|---|
| | | Mils | +/- | Mils | +/- |
| A | Minimum Layer 1 copper thickness | 1.8 | 20% | 1.8 | 10% |
| B | Minimum Layer 2 copper thickness | 1.6 | 20% | 1.6 | 10% |
| C | Layer 1 – 2 dielectric thickness | 2.0 | 10% | 3.0 | 10% |
| D | Minimum Layer 2 pad for Layer 1 to 2 Microvia | 10 | NA | 8 | NA |
| E | Minimum Layer 1 pad for Layer 1 to 2 Microvia | 8 | NA | 8 | NA |
| F | Minimum Layer 1 pad for Stacked Microvia | 8 | NA | 8 | NA |
| G | Minimum Layer 2 pad for Stacked Microvia | 10 | NA | 8 | NA |
| H | Minimum drill diameter for buried via | 10 | NA | 10 | NA |
| I | Minimum Pad diameter for buried via | 18 | | 16 | NA |
| J | Laser drilled Microvia dia. from layer 1 to 2 & 2 -3 | 4 | NA | 4 | NA |
| K | Aspect ratio | 0.5: 1 | NA | 0.75:1 | NA |
| | | | | | |

# Summary & Conclusions

- Increasing device I/O & speed are driving traditional plated through hole technology to the limits of performance both physically and electrically. What's needed ?
  - High performance well characterized dielectric materials
  - Advanced imaging techniques (Laser Direct Imaging)
  - Alternate via structures (Laser drilled, Blind & buried)
  - Filled via technologies
  - Stacked laser drilled via structures
  - High aspect ratio copper plating capability
- Chip scale components are migrating from hand-held devices to large scale electronic systems with increasing I/O's and they are here today!!!

# Design Considerations With Microvias



With aspect ratio's limited to 0.5 to 0.6 and typical hole diameters of 4 to 6 mils, dielectric thickness are respectively 2 mils to 3 mils max.

Thin dielectric issues include:

- Dielectric layers are generally single ply constructions
- Thickness variations of 20 percent can be expected
- Impedance of 50 ohms and higher are difficult to achieve without using fine lines (i.e. < 5mils)
- Tolerance must be considered when lines are less than 5 mils
- Surface and buried via layers are plated increasing trace thickness and must be accounted for in the impedance model
- Parametric modeling is recommended for critical lines

# Electrical Properties Of Laser Drilled Via's

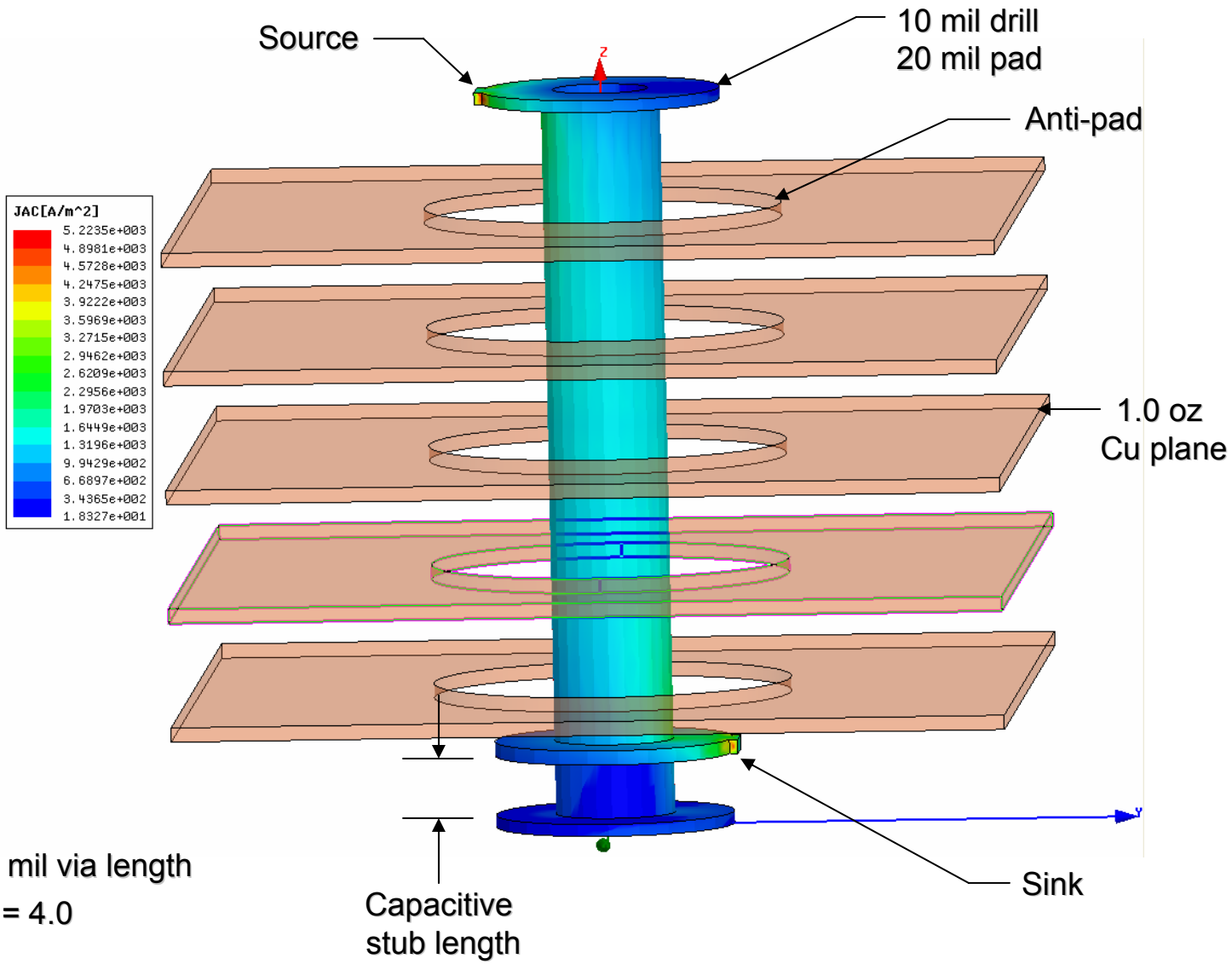


Properties of interest:

- Capacitance of via structure with respect to:
  - Adjacent return planes
  - Anti-pad geometries
- DC resistance
- AC resistance
- DC inductance
- AC inductance

# RLC Models: PTH Via & Pad

Enabling Technologies



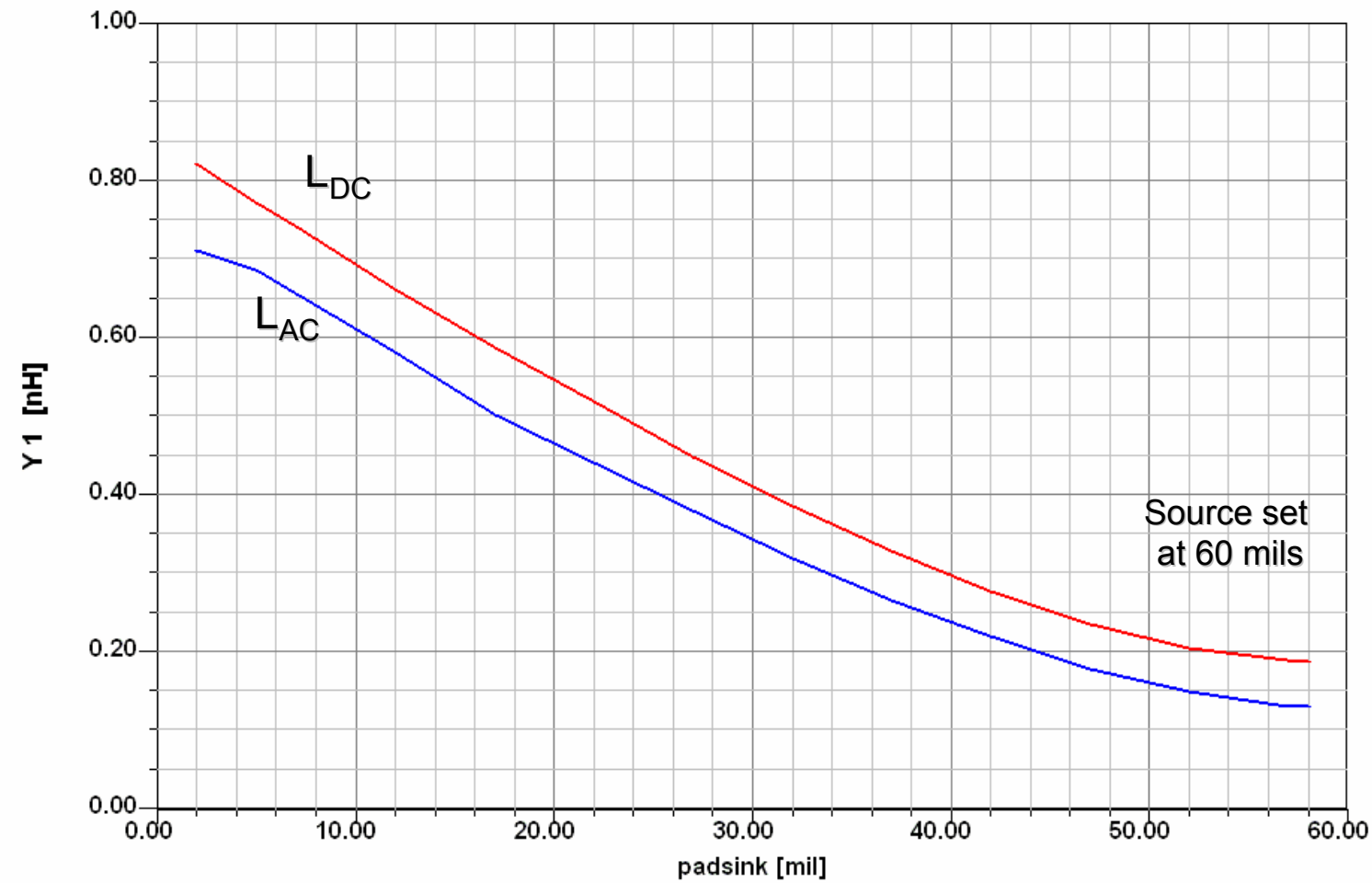

62 mil via length

$\varepsilon_r = 4.0$

# RLC Models: PTH Via & Pad

Enabling Technologies

Inductance: 10 mil via 20 mil pad
Current path sweep: Start Z=2 mil, Stop Z=58 mil

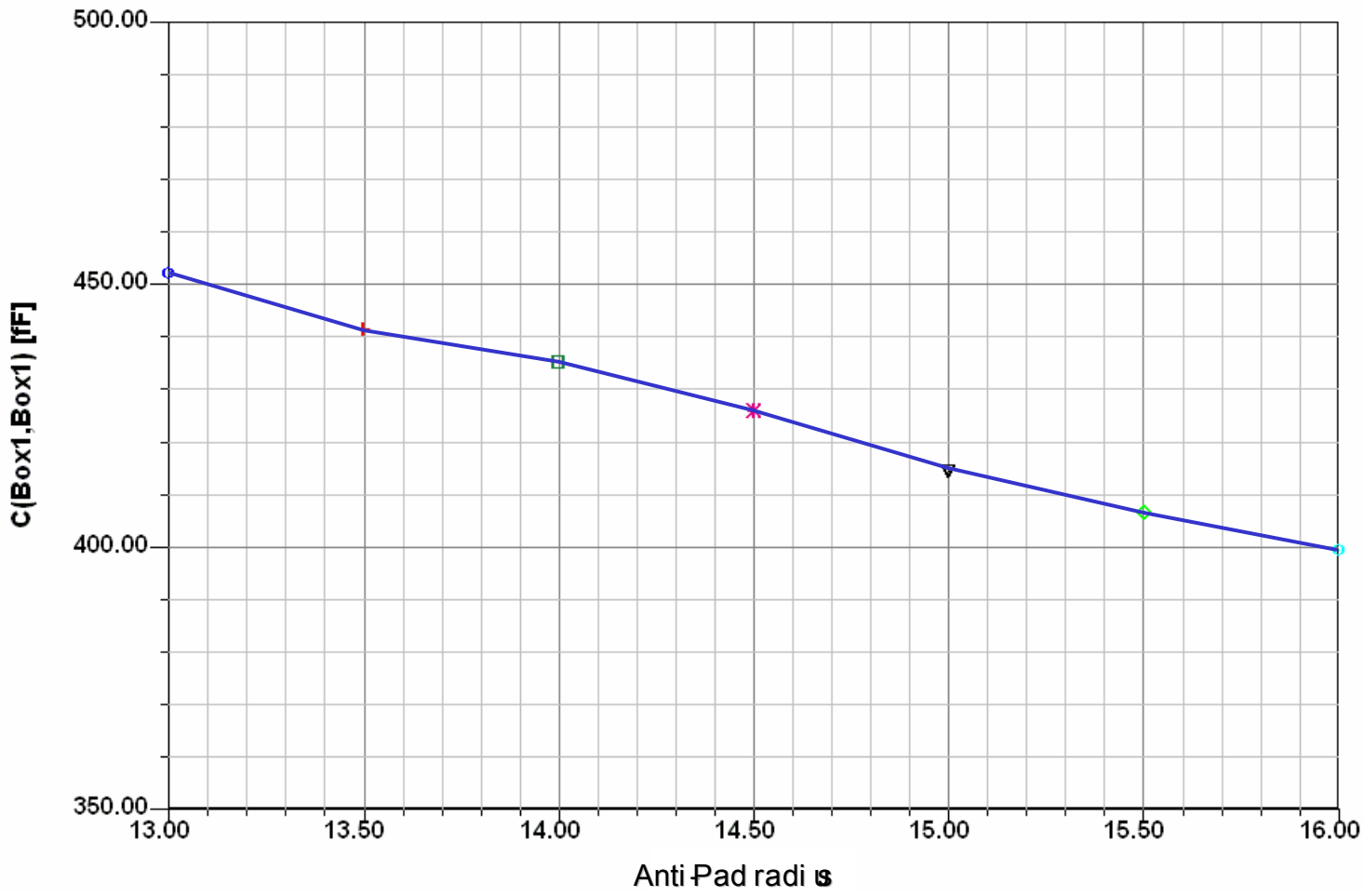



Increasing distance from Source

# RLC Models: PTH Via & Pad

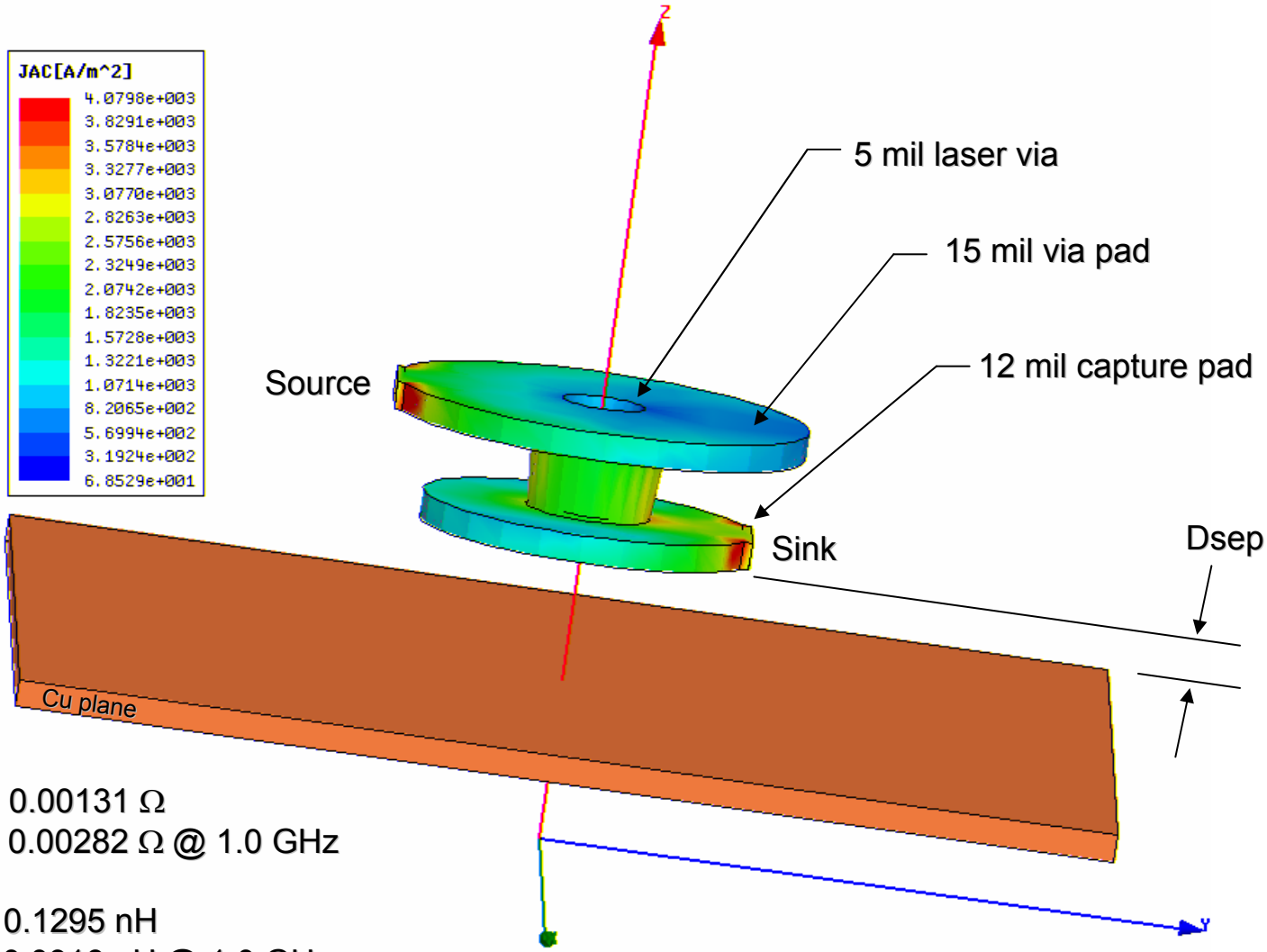
Enabling Technologies

Capacitance: 10 mil via 20 mil pad
Anti-Pad sweep: Start radius 13 mil, Stop radius 16 mil



# RLC Models: 0.8 mm BGA Pad & μVia

Enabling Technologies

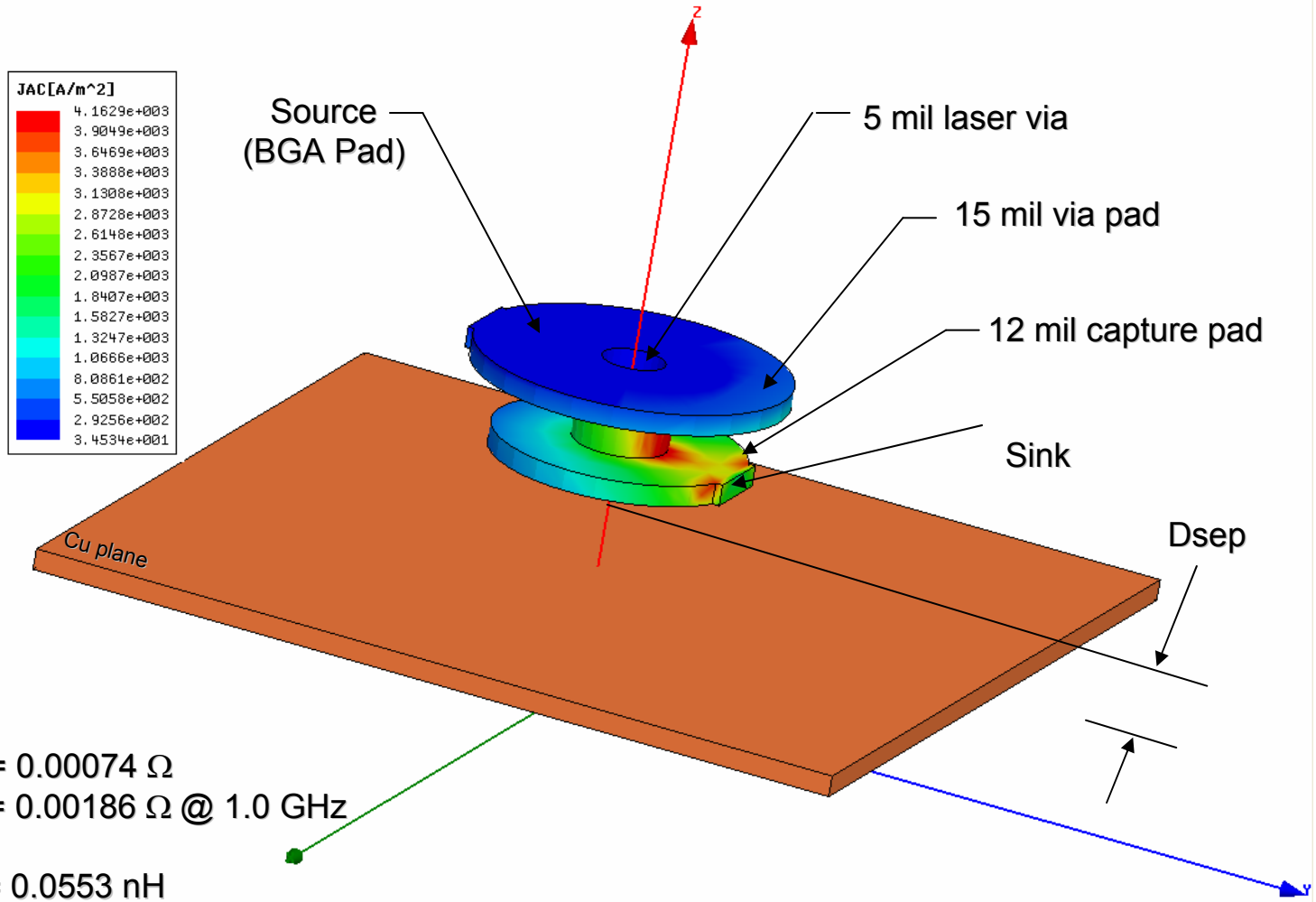



$R_{DC}$ = 0.00131 Ω
$R_{AC}$ = 0.00282 Ω @ 1.0 GHz

$L_{DC}$ = 0.1295 nH
$L_{AC}$ = 0.0916 nH @ 1.0 GHz

# RLC Models: 0.8 mm BGA Pad & μVia





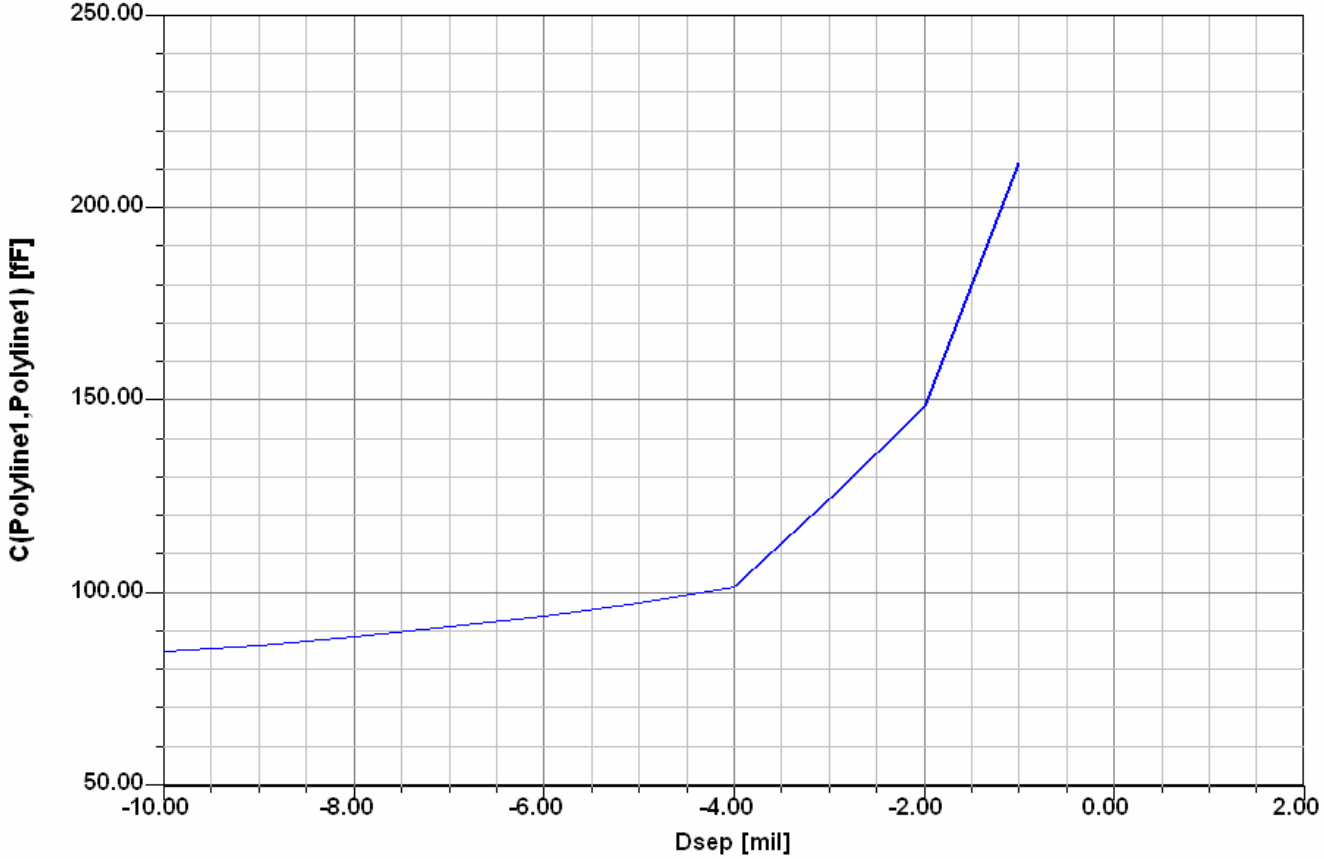

$R_{DC}$ = 0.00074 Ω
$R_{AC}$ = 0.00186 Ω @ 1.0 GHz

$L_{DC}$ = 0.0553 nH
$L_{AC}$ = 0.0337 nH @ 1.0 GHz

# RLC Models: 0.8 mm BGA Pad & μVia

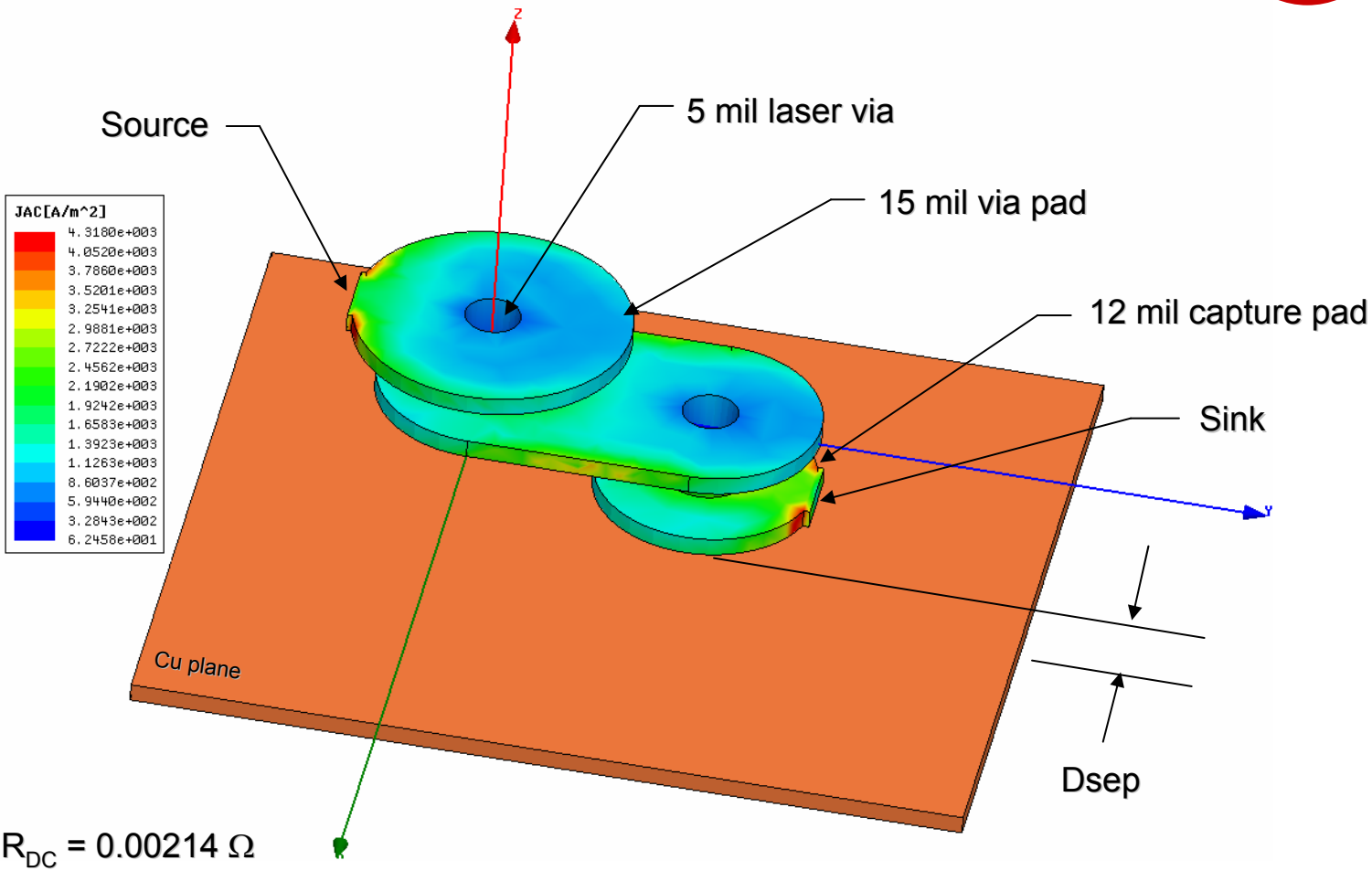
Enabling Technologies

Capacitance: Microvia with respect to plane



# RLC Models: 0.8 mm BGA Pad & μVia



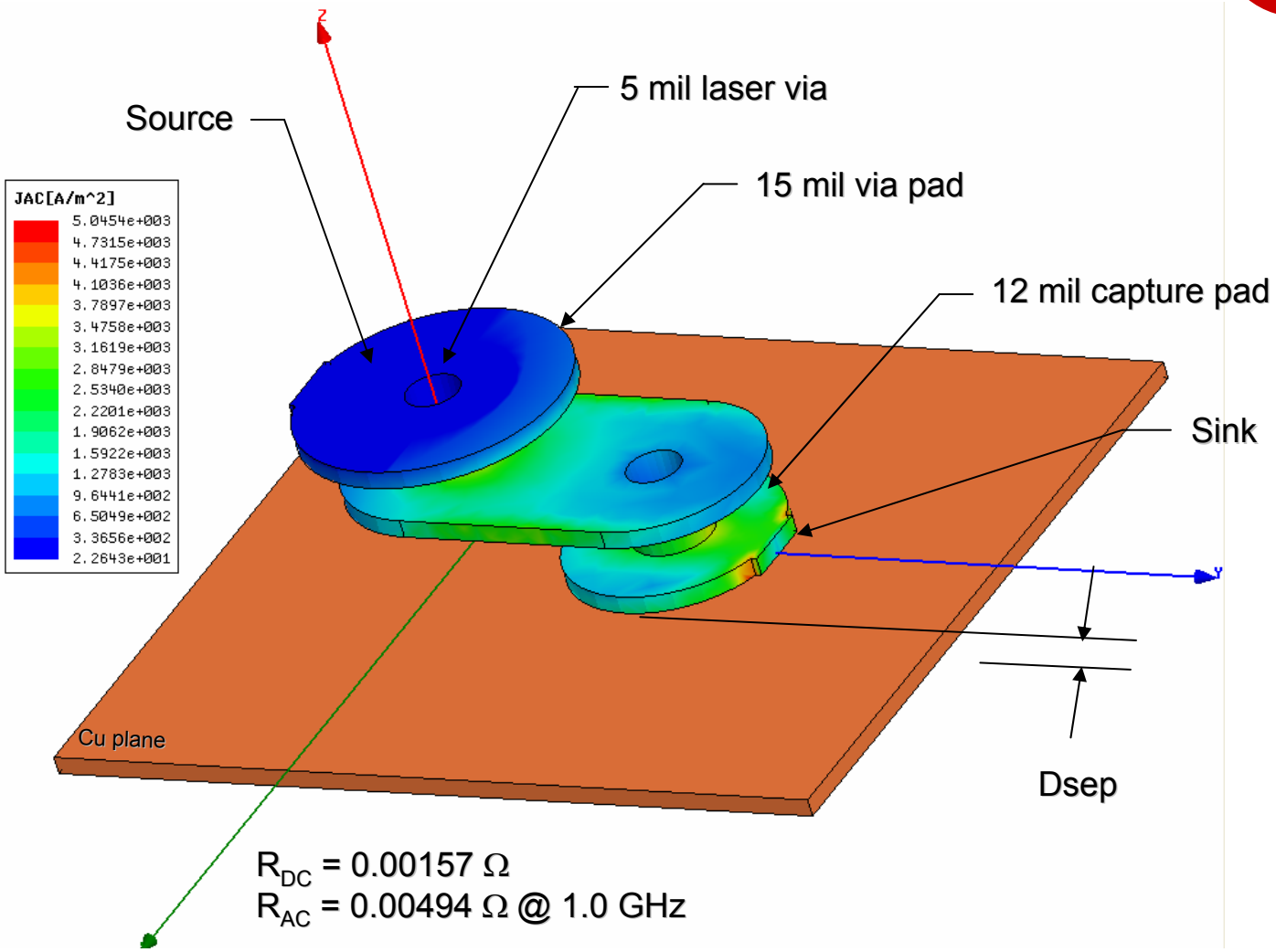



$R_{DC}$ = 0.00214 Ω
$R_{AC}$ = 0.00692 Ω @ 1.0 GHz

$L_{DC}$ = 0.308 nH
$L_{AC}$ = 0.238 nH @ 1.0 GHz

# RLC Models: 0.8 mm BGA Pad & μVia





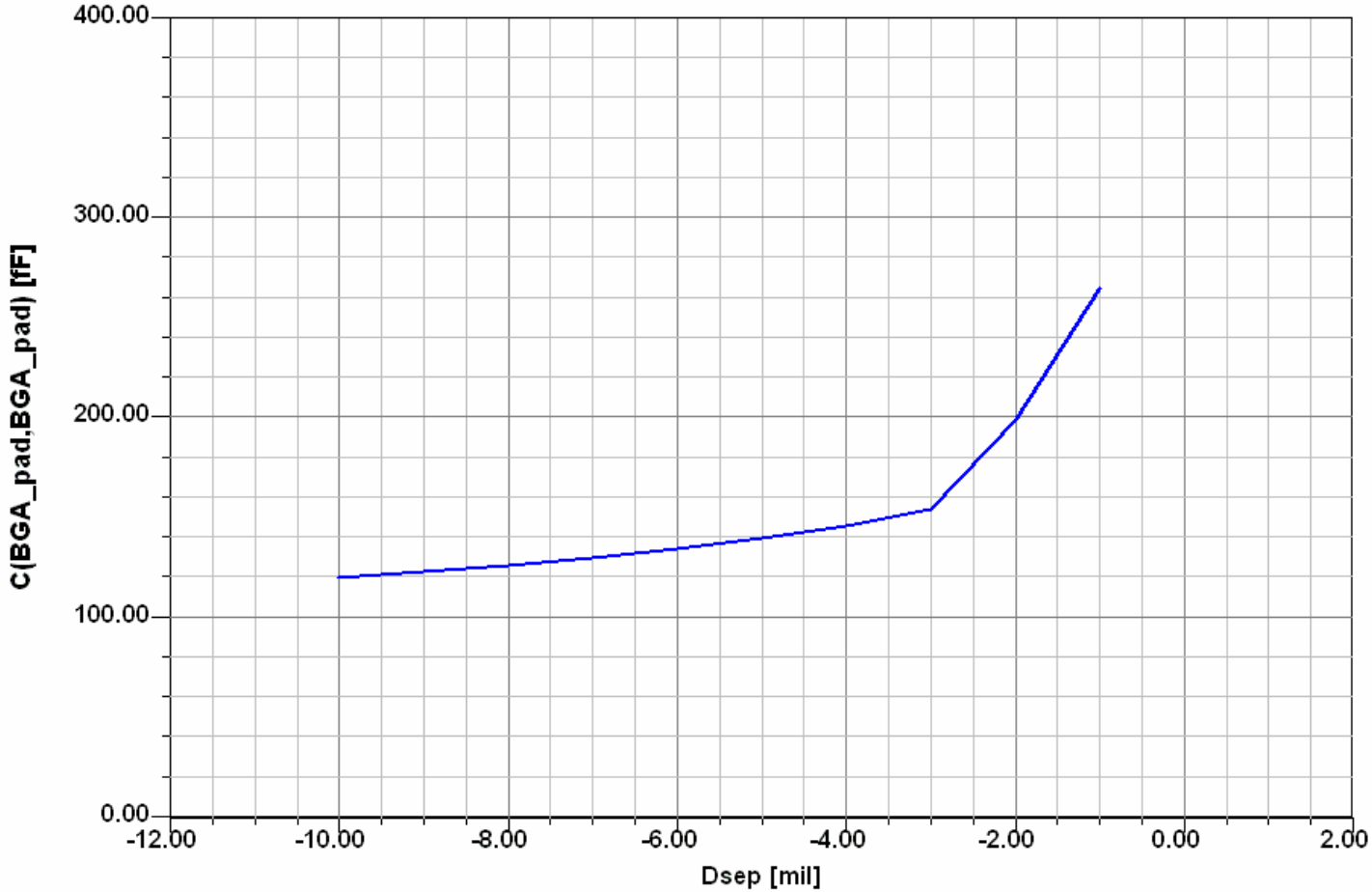

$R_{DC}$ = 0.00157 Ω
$R_{AC}$ = 0.00494 Ω @ 1.0 GHz

$L_{DC}$ = 0.205 nH
$L_{AC}$ = 0.139 nH @ 1.0 GHz

# RLC Models: 0.8 mm BGA Pad & μVia

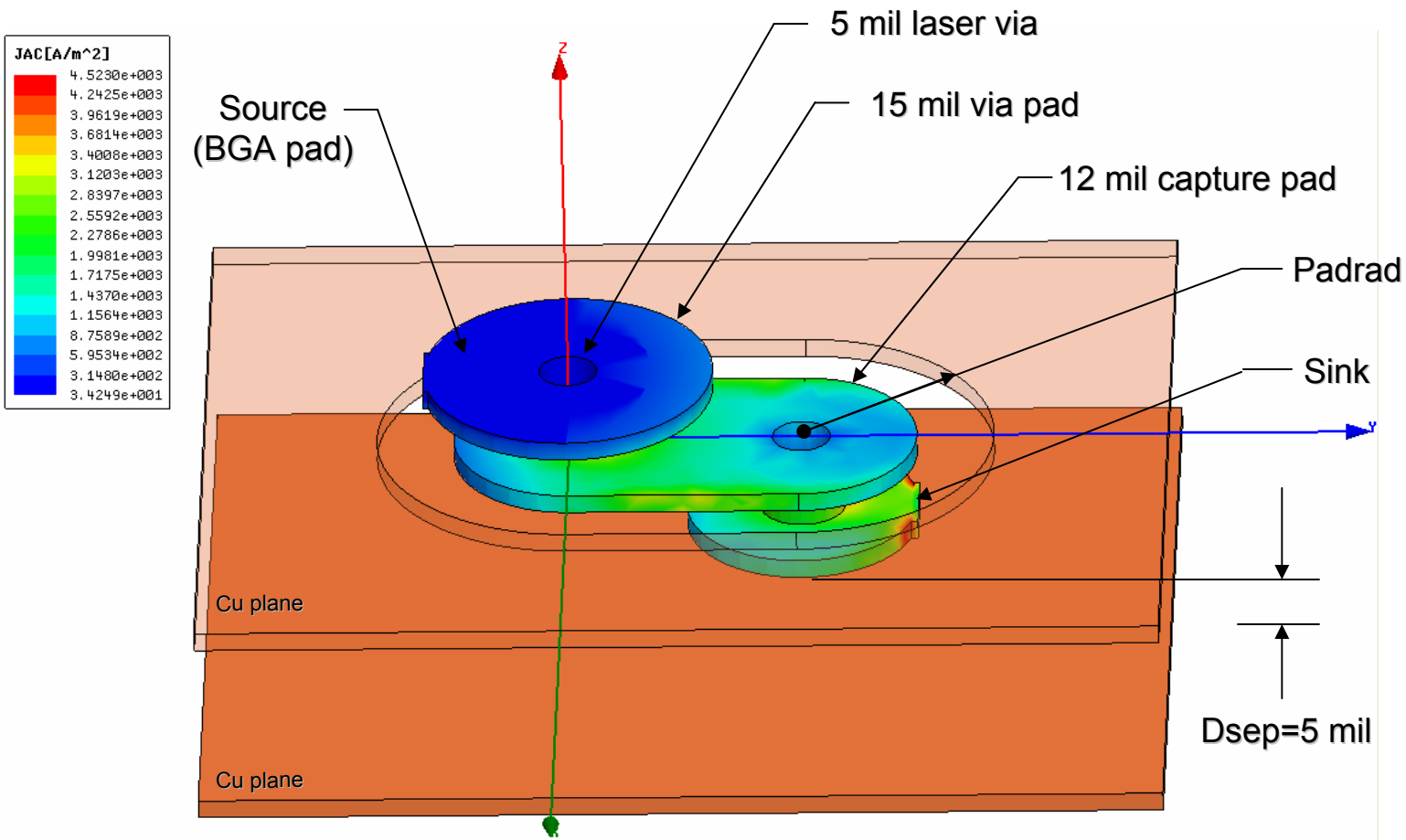
Enabling Technologies

Capacitance: “Stair-Case” Via with respect to plane below



# RLC Models: 0.8 mm BGA Pad & μVia





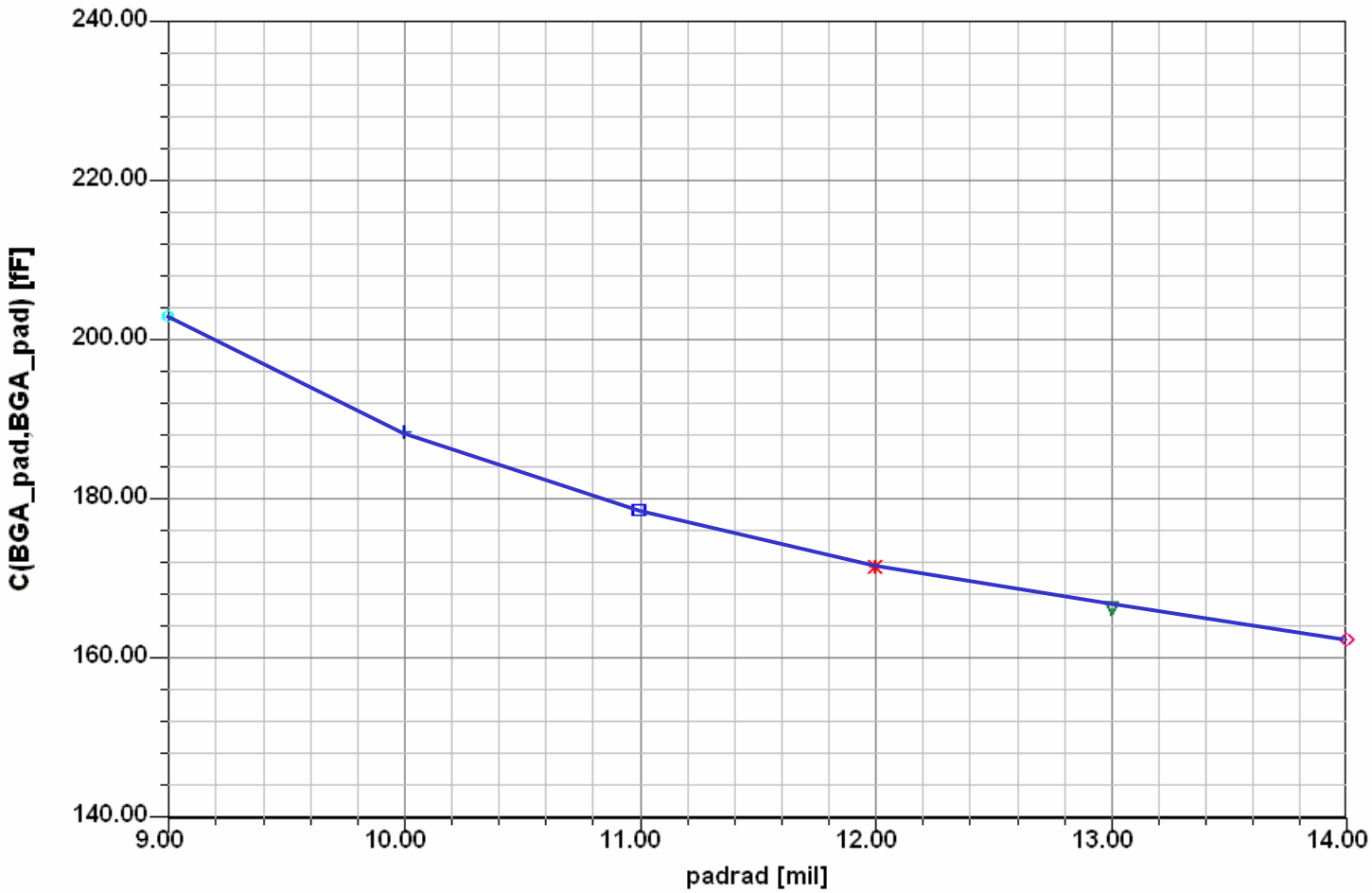

$R_{DC}$ = 0.00158 Ω
$R_{AC}$ = 0.00476 Ω @ 1.0 GHz

$L_{DC}$ = 0.205 nH
$L_{AC}$ = 0.140 nH @ 1.0 GHz

# RLC Models: 0.8 mm BGA Pad & μVia

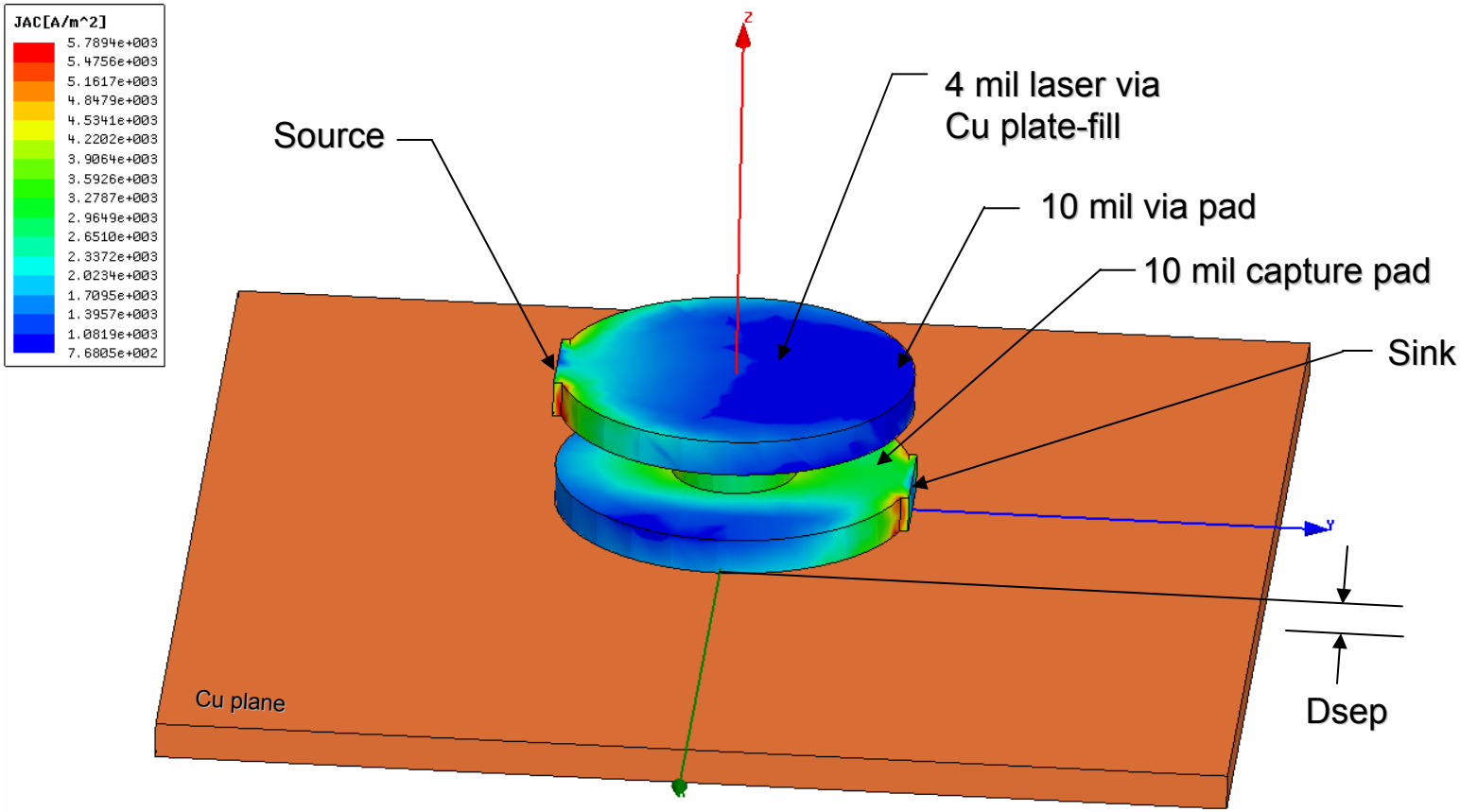


Capacitance: "Stair-Case" Via with respect to adjacent plane



# RLC Models: SMV Pad & μVia





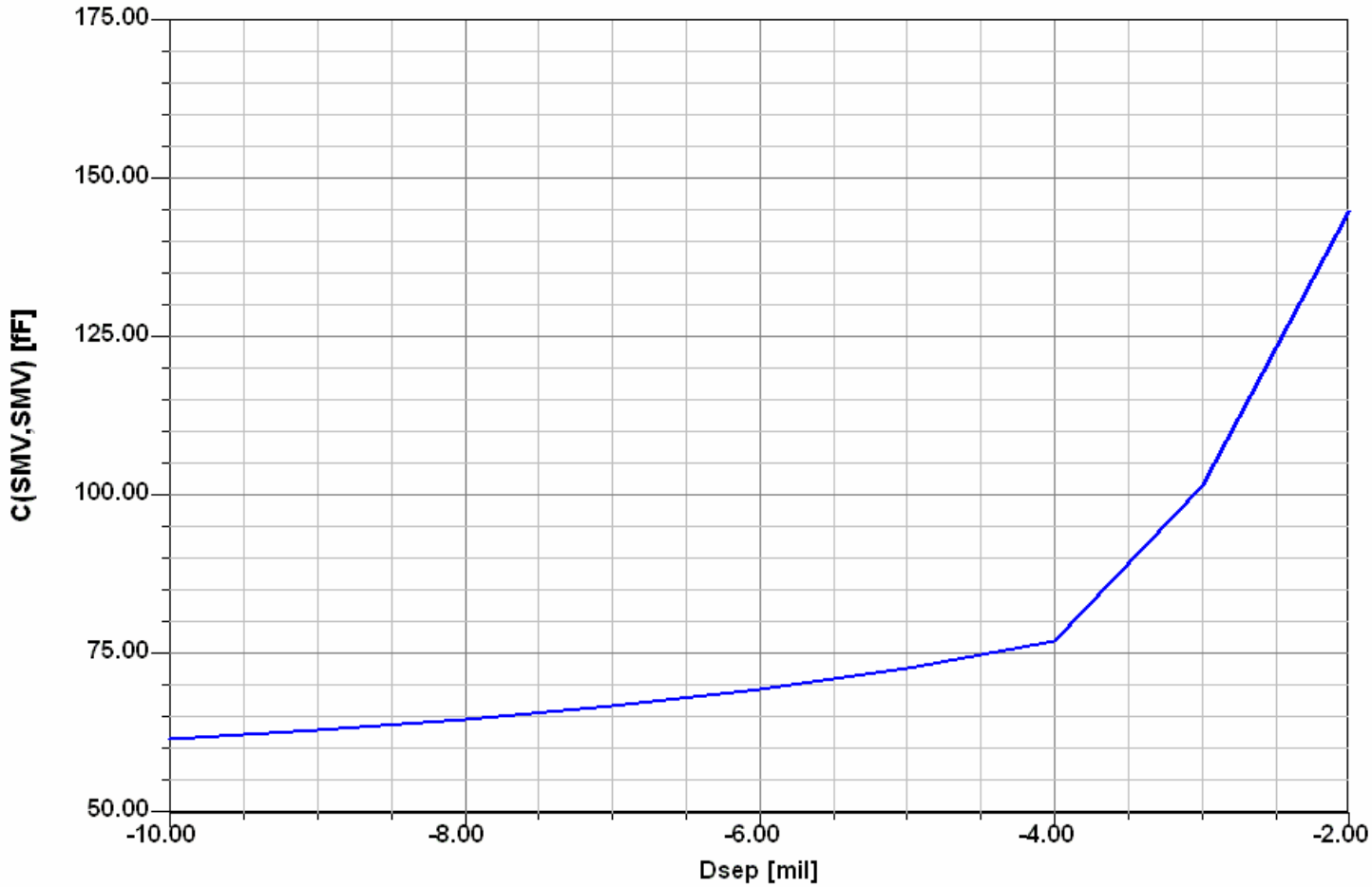

$R_{DC}$ = 0.00125 Ω
$R_{AC}$ = 0.00295 Ω @ 1.0 GHz

$L_{DC}$ = 0.0957 nH
$L_{AC}$ = 0.0550 nH @ 1.0 GHz

# RLC Models: SMV Pad & μVia

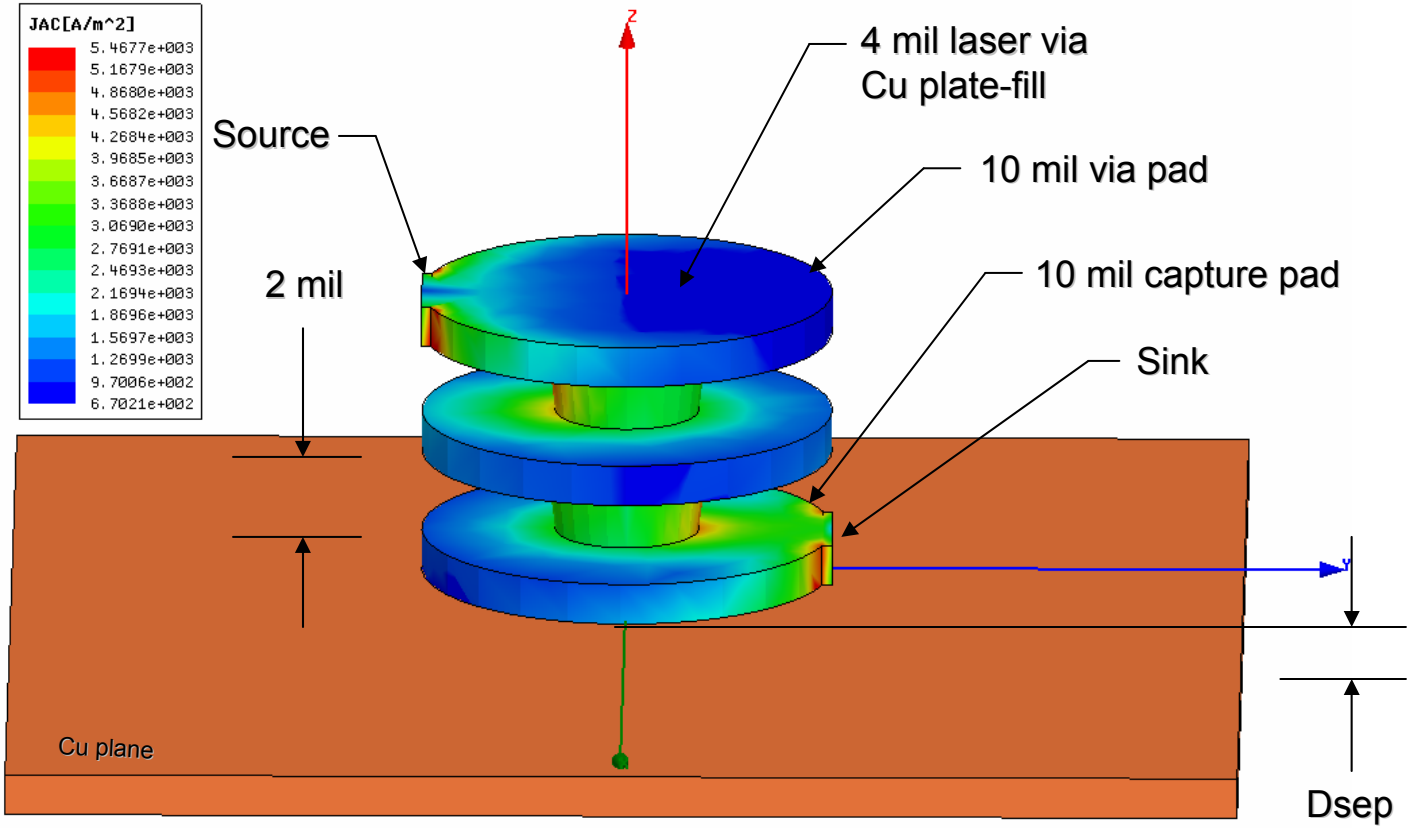


Capacitance: SMV Via with respect to plane below



# RLC Models: SMV_2 Pad & μVia



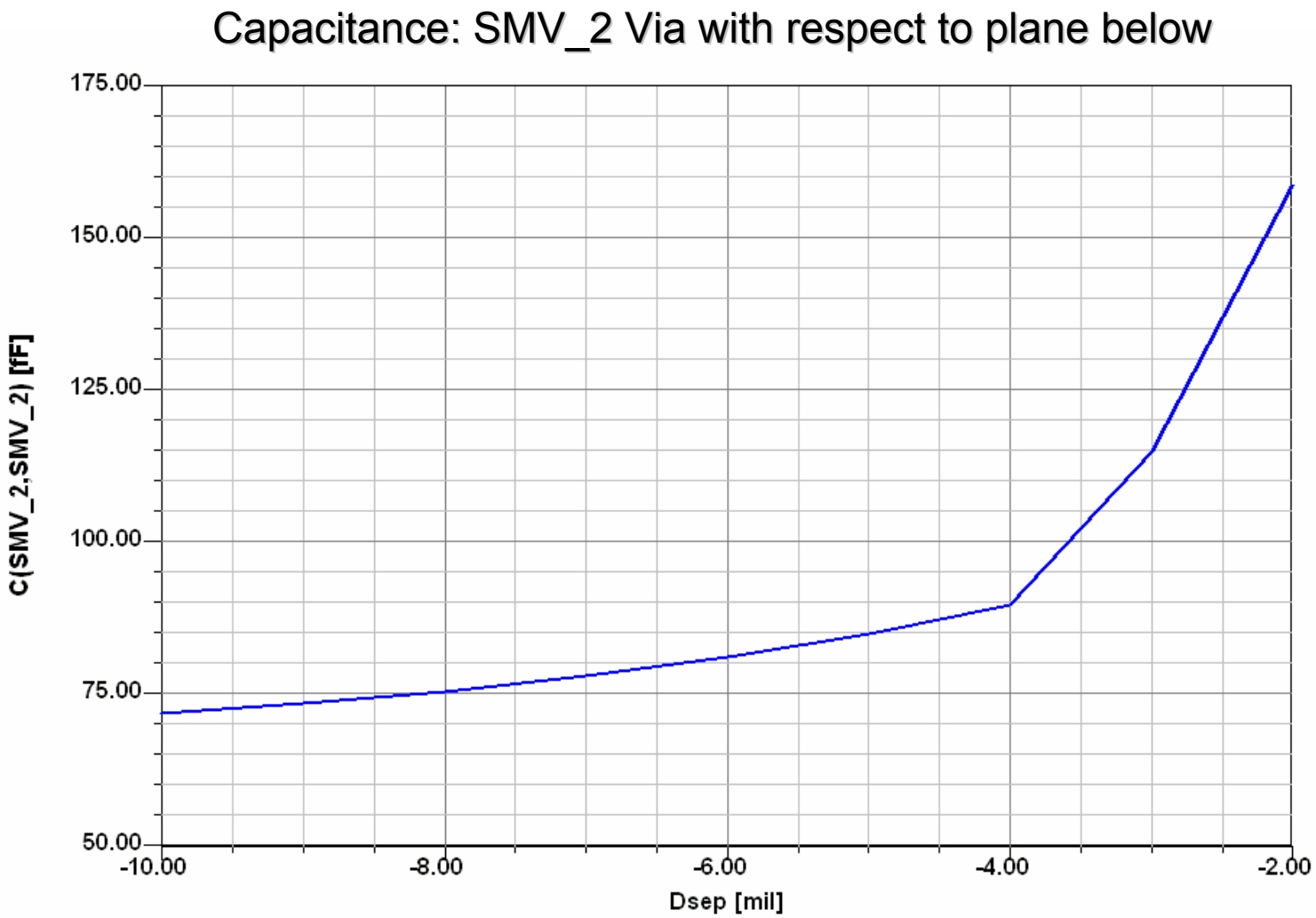



$R_{DC}$ = 0.00148 Ω
$R_{AC}$ = 0.00389 Ω @ 1.0 GHz

$L_{DC}$ = 0.119 nH
$L_{AC}$ = 0.0695 nH @ 1.0 GHz

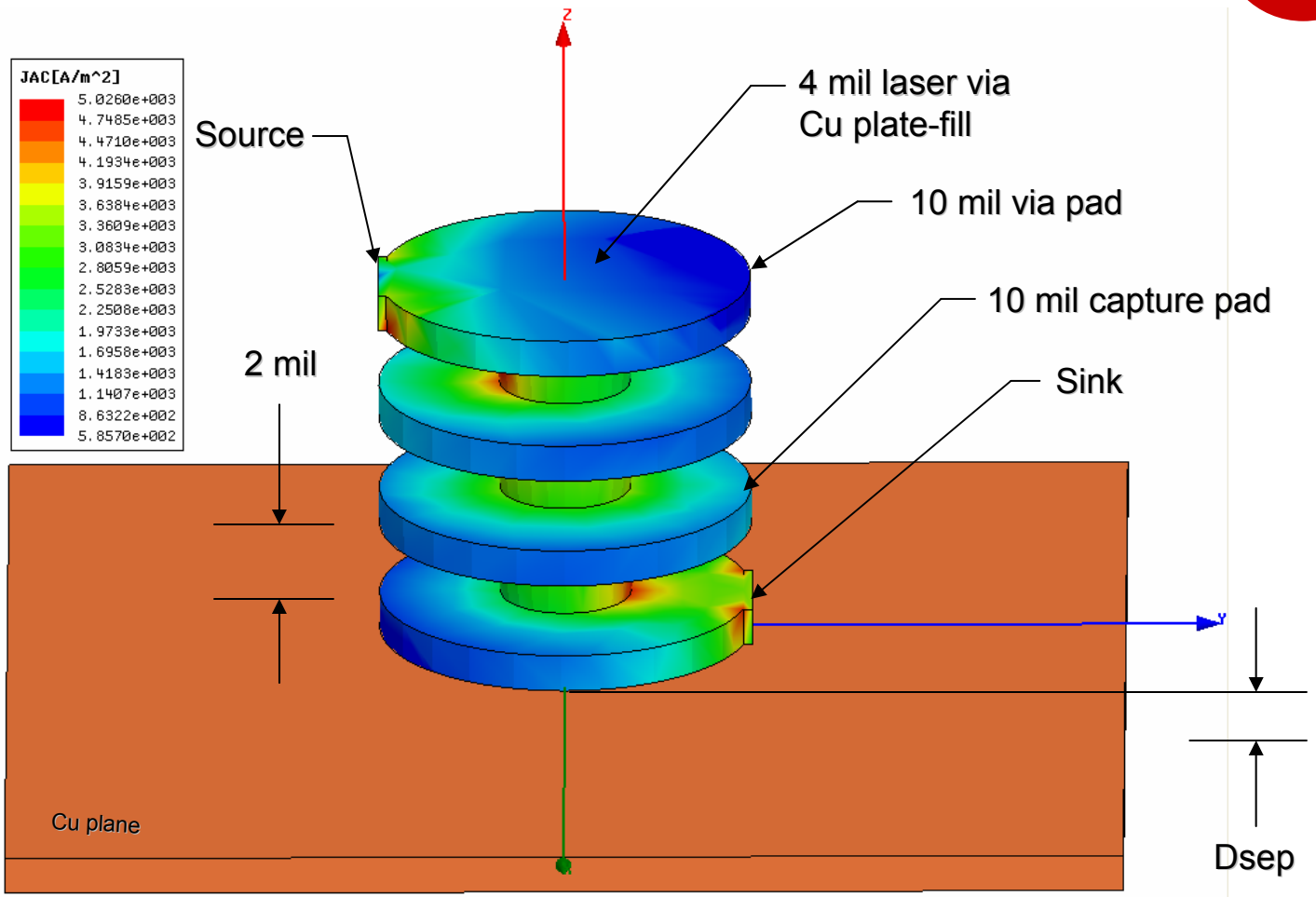
# RLC Models: SMV Pad & μVia





# RLC Models: SMV_3 Pad & μVia





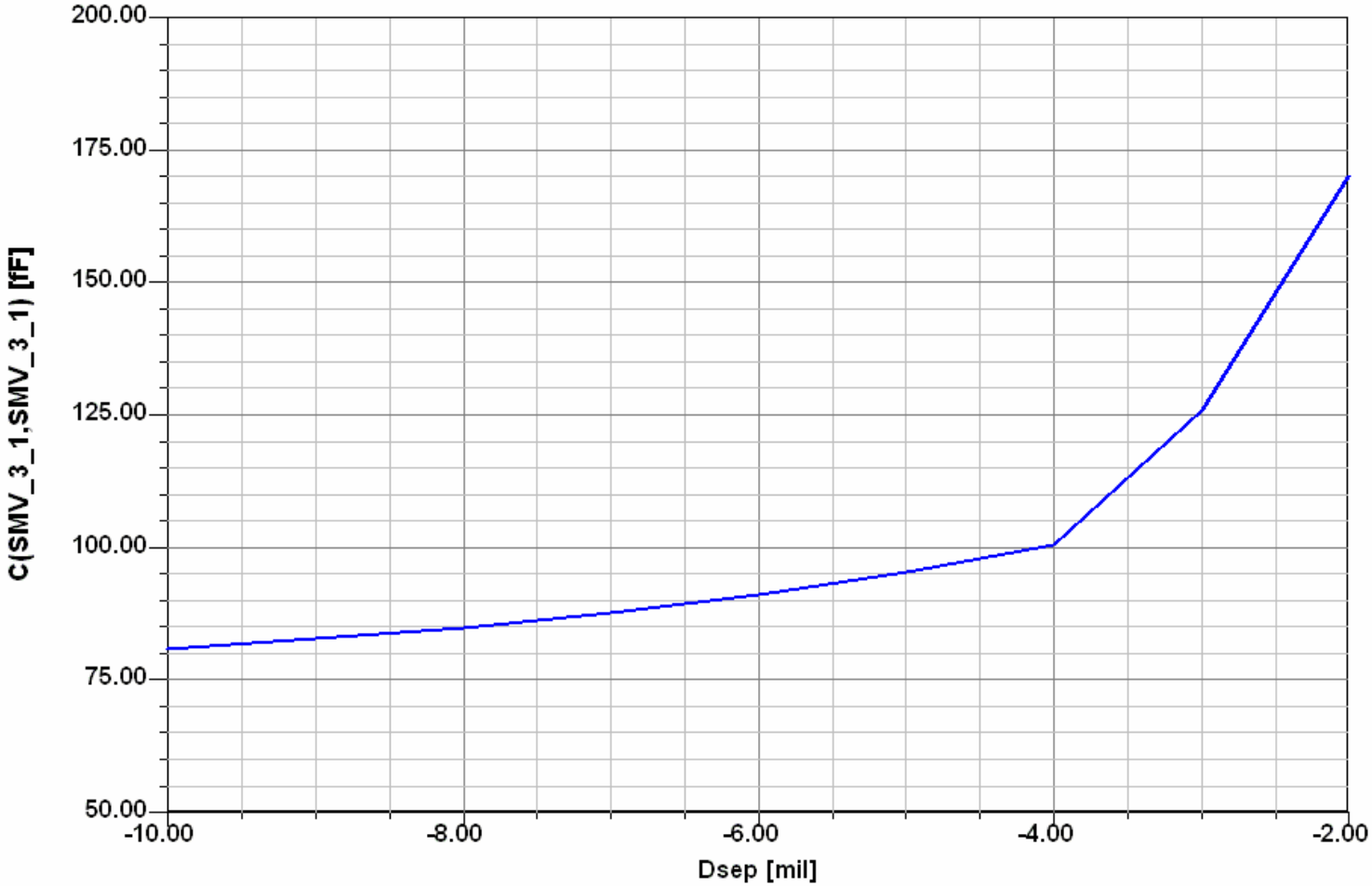

$R_{DC}$ = 0.00161 Ω
$R_{AC}$ = 0.0153 Ω @ 1.0 GHz

$L_{DC}$ = 0.150 nH
$L_{AC}$ = 0.0947 nH @ 1.0 GHz

# RLC Models: SMV Pad & μVia

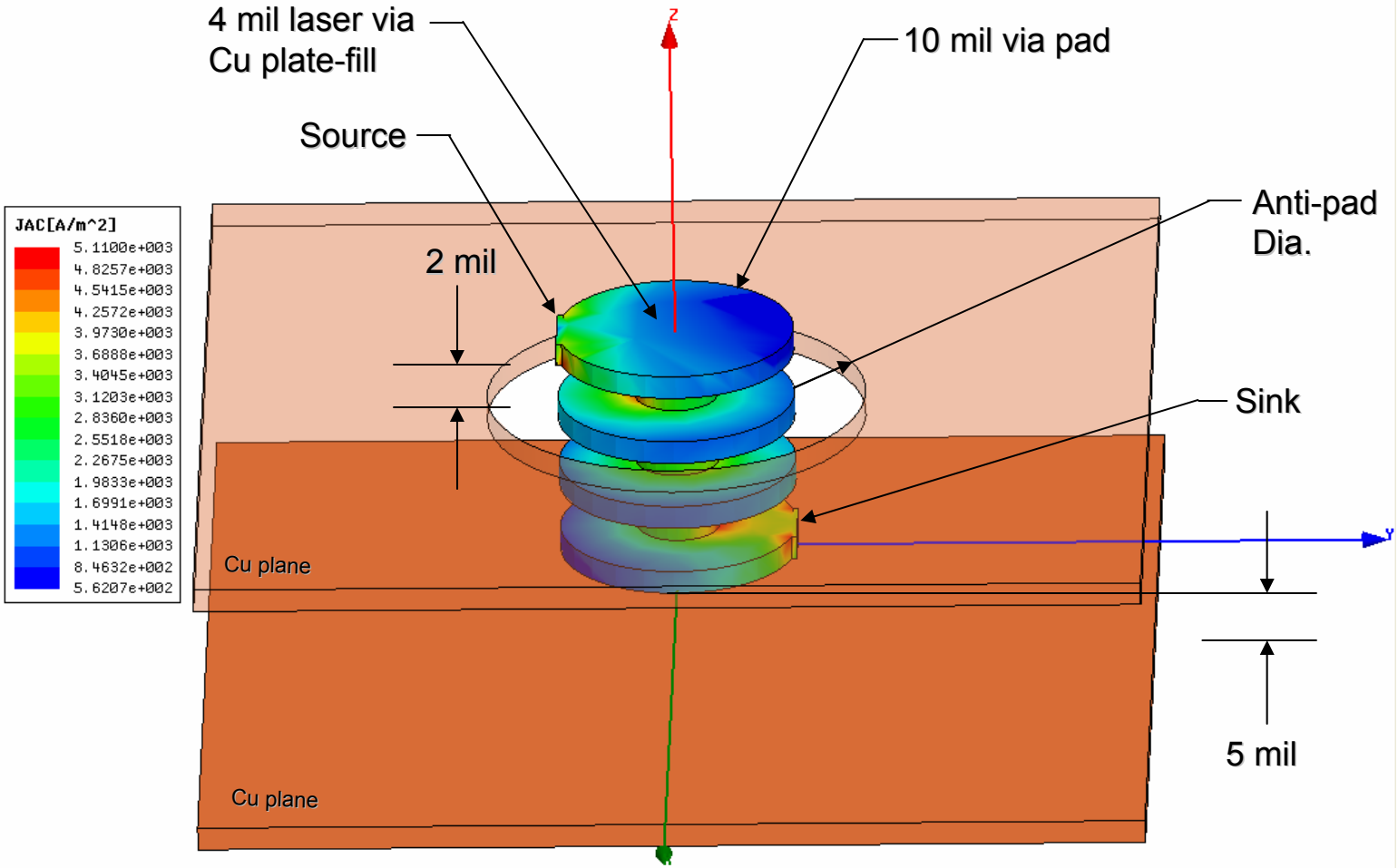


Capacitance: SMV_3 Via with respect to plane below



# RLC Models: SMV_3 Pad & μVia



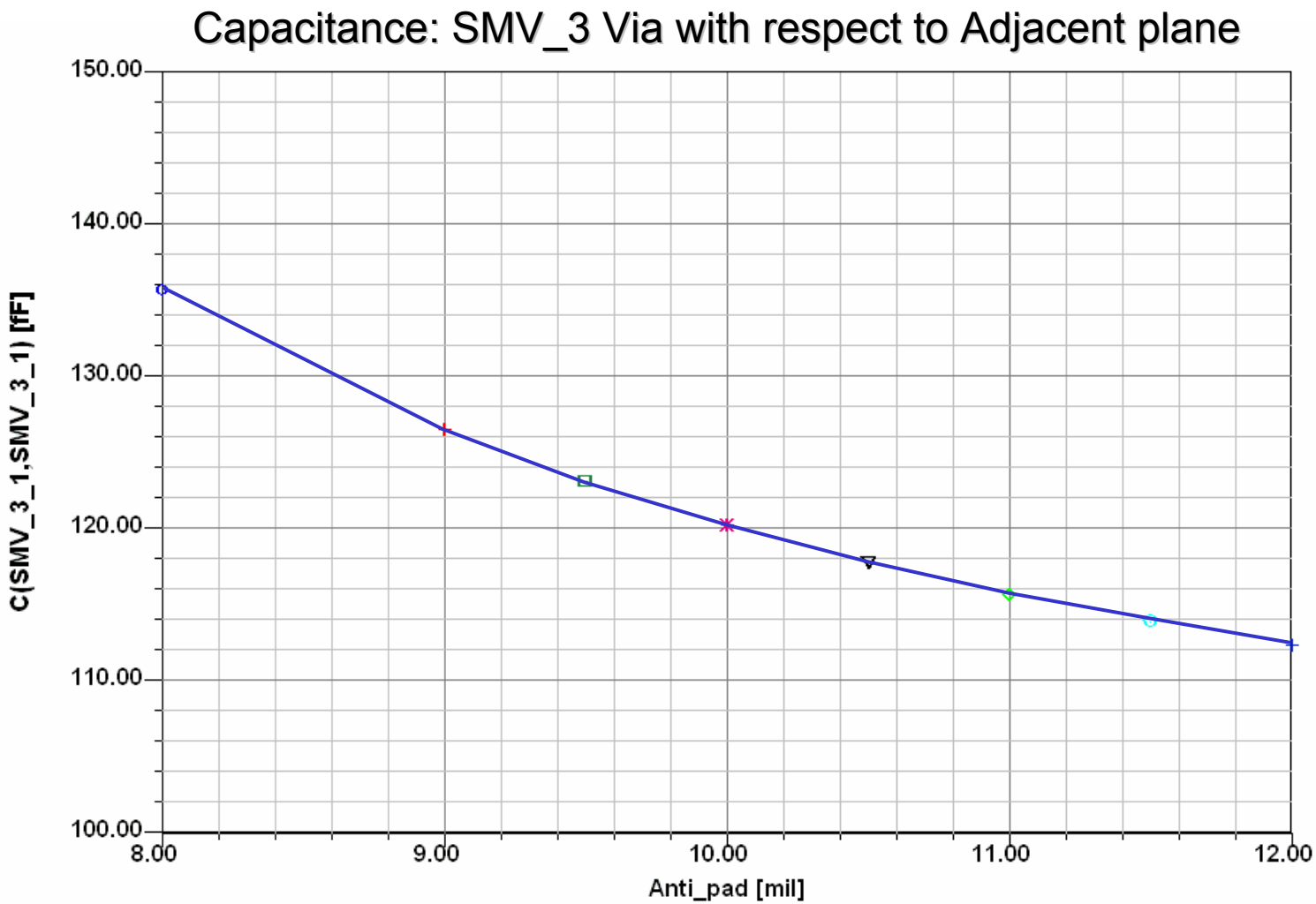



$R_{DC}$ = 0.00161 Ω
$R_{AC}$ = 0.0156 Ω @ 1.0 GHz

$L_{DC}$ = 0.150 nH
$L_{AC}$ = 0.0907 nH @ 1.0 GHz

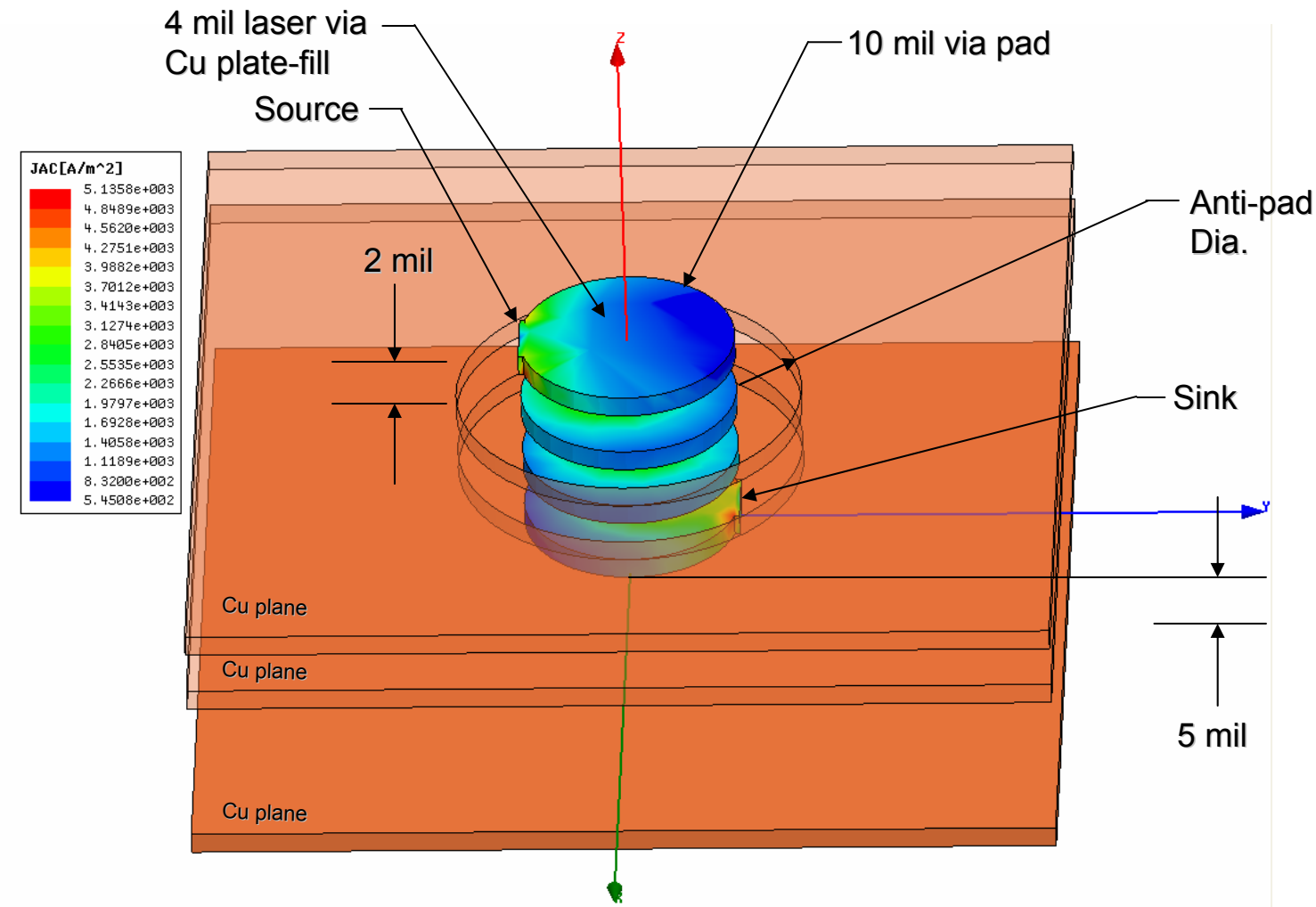
# RLC Models: SMV Pad & μVia

Enabling Technologies



# RLC Models: SMV_3 Pad & μVia



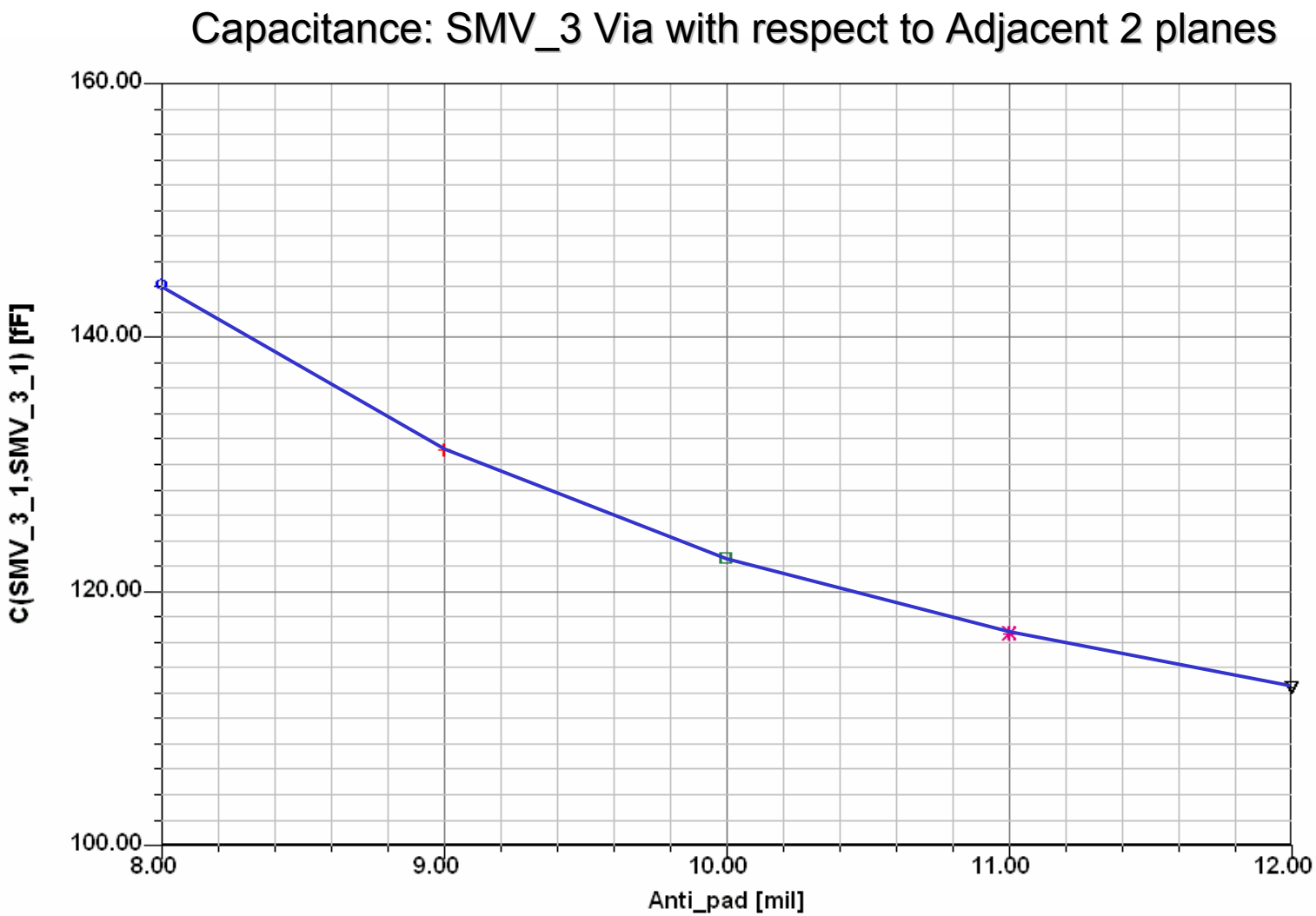



$R_{DC}$ = 0.00161 Ω
$R_{AC}$ = 0.0160 Ω @ 1.0 GHz

$L_{DC}$ = 0.150 nH
$L_{AC}$ = 0.0882 nH @ 1.0 GHz

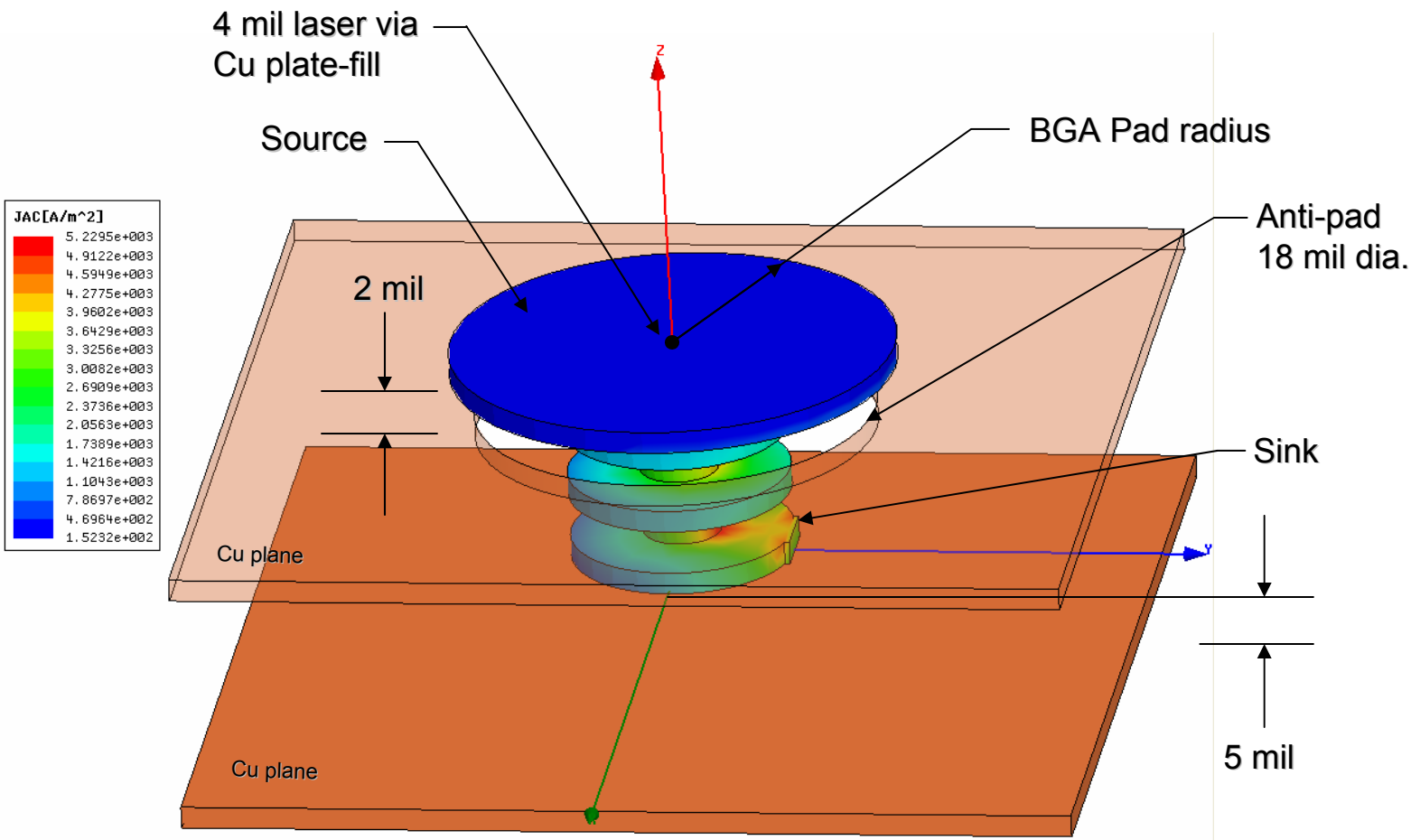
# RLC Models: SMV Pad & μVia

Enabling Technologies



# RLC Models: SMV_3 Pad & μVia

Enabling Technologies

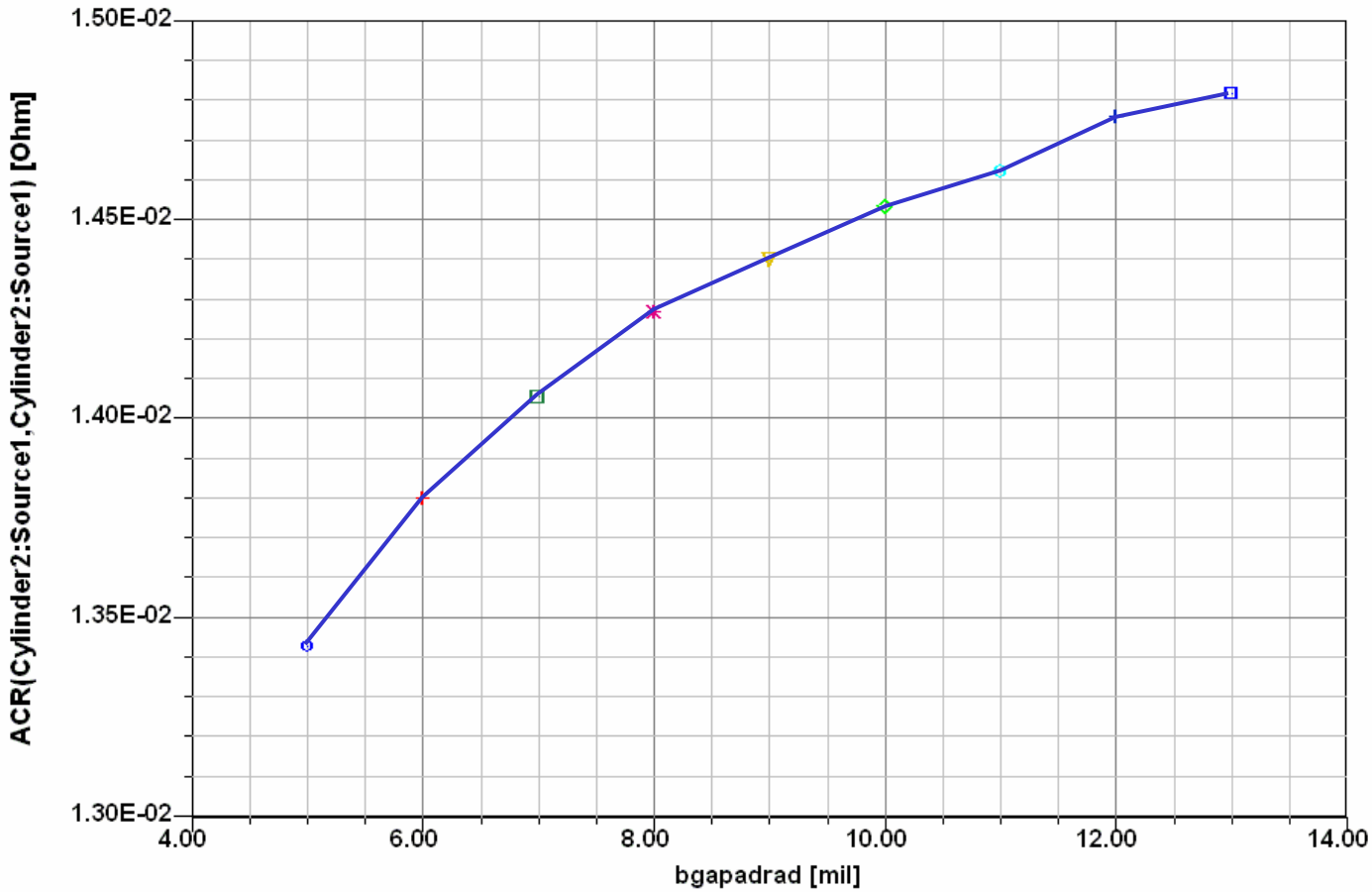



BGA pad diameter sweep: Start 10 mil stop 26 mil

# RLC Models: SMV Pad & μVia



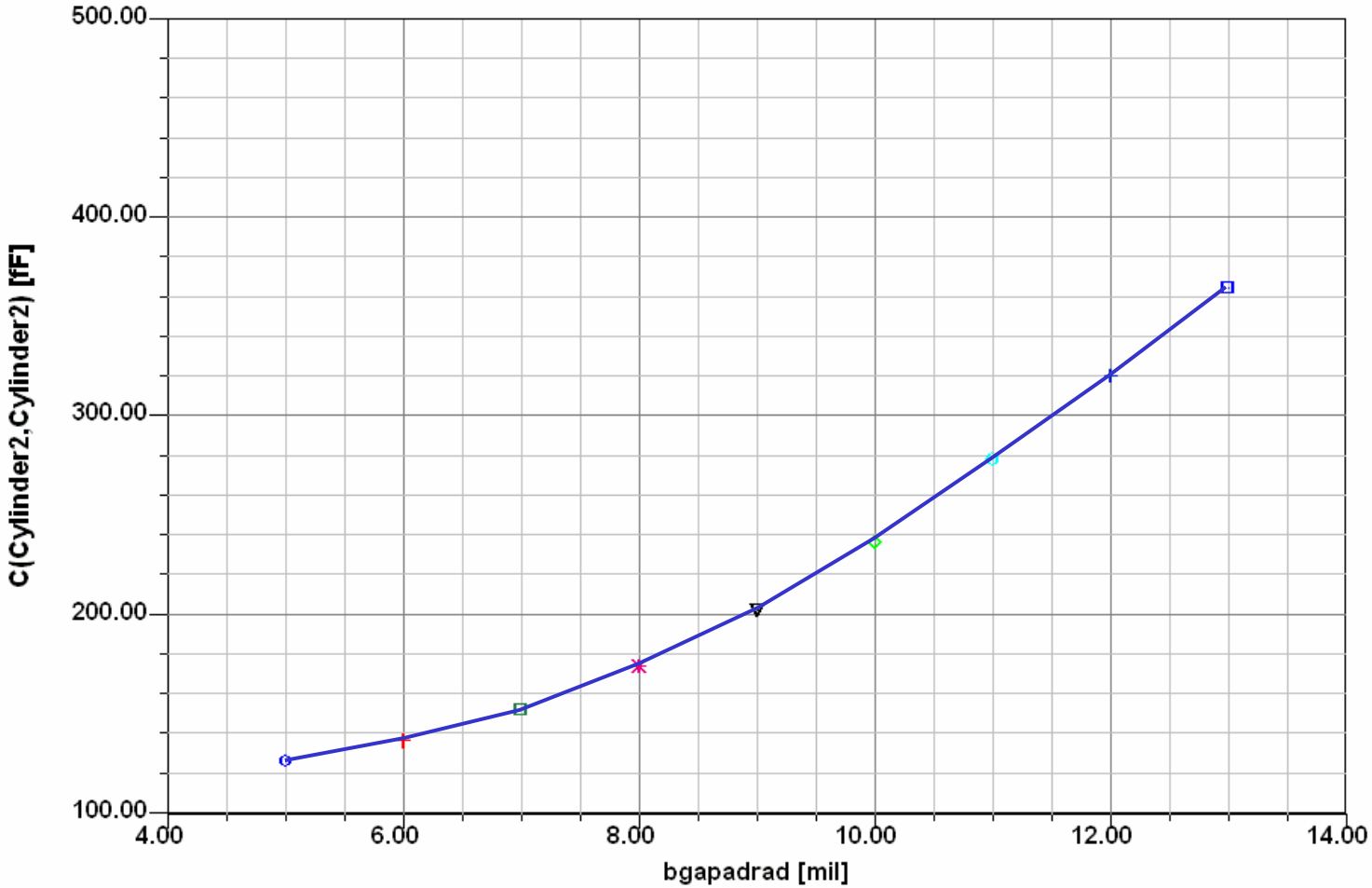
Resistance: SMV_3 Via BGA pad radius sweep: 5 mil start, 13 mil finish



# RLC Models: SMV Pad & μVia



Capacitance: SMV_3 Via with respect to Adjacent plane
BGA pad radius sweep: 5 mil start, 13 mil stop



# RLC Models: SMV Pad & μVia

Enabling Technologies

Inductance: SMV_3 Via BGA pad radius sweep: 5 mil start, 13 mil finish