Advanced PWB Substrates
Enabling Technologies

By

Tom Buck

Dynamic Details Inc.
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Enabling Technologies

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Overview

Technology Drivers
Advanced Materials
Characterized FR-4
Hybrid Constructions
Laser Direct Imaging
High Aspect Ratio Copper Plating
Laser Drilling
Planar Via Technologies

Driving Factors for Advanced PWB Technology

- Advanced Materials
- Characterized FR-4
- Hybrid Constructions
- Laser Direct Imaging
- High Aspect Ratio Copper Plating
- Laser Drilling
- Planar Via Technologies
Overview

Technology Drivers

- Advanced Materials
- Characterized FR-4
- Hybrid Constructions
- Laser Direct Imaging
- High Aspect Ratio
- Copper Plating
- Laser Drilling
- Planar Via
- Technologies
Enabling Technologies

Advanced Printed Circuit Technologies

Chip scale packaging and ever increasing signal speeds are testing the limits of conventional PWB fabrication technologies. Bridging the gap to push forward will require an array of enabling technologies!

- Enabling technologies for advanced PWB’s
  - Advanced low loss laminate systems
    - Mixed dielectric structures
  - Laser Direct Imaging (LDI)
  - High aspect ratio Cu plating (Pulse Plating)
  - Laser drilling
    - Planar Cu filled Microvia’s
    - Stacked Microvia’s
  - Advanced PWB structures
High Density Interconnect Markets

- 56% Cellular/Wireless
- 18% Telecom
- 10% Silicon Packaging
- 10% High End Computer
- 3% Industrial
- 2% Personal Computer
- 1% Medical

Enabling Technologies
Enabling Technologies

Trends in electrical performance and density

Portable products.

Significant density increases due to miniaturization. More pitch reduction than I/O increases. RF electrical requirements are slowly becoming more complex but still limited to small portion of PCB design.

Increasing electrical performance requirements.
T-Buck Dynamic Details Inc. 2003

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Increasing Density

Trends in electrical performance and density

Network/Telecom/High-End Computing.

Significant density increases with rapidly decreasing BGA pitch and increasing I/O driven by a rapid increase in digital speed and a constant multiplying of functionality. Density and speed requirements can be in conflict.

- 1998
- 2004

BGA Pitch

- .5 mm
- .8 mm
- 1.0 mm

- .5 mm SMT
- 1.27 mm BGA

- 100 I/O to 1000 I/O
- 100 I/O to 1500 I/O
- 100 I/O to 2500 I/O

<100 MHz Digital  Rf/wireless  < 1 GHz Digital  2 to 10 GHz Digital

Increasing electrical performance requirements.
Performance Driven Board Design
- Controlled impedance required
- Differential signaling required
  - Edge Coupled Lined
  - Broad Side Coupled
- Solid “AC Return Path”
- Low Attenuation
  - Low loss dielectric
  - Mixed dielectrics
- Higher layer counts required
  - Board thickness?

High Density Connectors
- Controlled Impedance
- Differential Signaling
- Minimize Crosstalk
- High Signal to Ground Ratio

Design Challenge
High Data Rates
- 0.6 Gbit/s
- 1.2 Gbit/s
- 2.5 Gbit/s
- 3.125 Gbit/s
- 10 Gbit/s

Materials:
- FR-4 Epoxy Glass
- Low Loss Epoxies
- RF Materials/Mixed
The Electrical Path is Now A 3D Problem!

High Speed Electrical Path

Circuit Card

Backplane
Impact Of Current Trends On PWB Technology

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- Increased line width to reduce copper loss
- Minimum length routing
- Matched length routing
- Well characterized FR-4 and or low loss dielectrics materials
- Differential signaling between adjacent pins
- Via parameters must be characterized

Conflicting Design Requirements

- BGA escape driving up layer count
- Line widths driven down to 50 mm to 75 mm to allow escape
- Increasing layer counts driving up substrate thickness & Via length
- Smaller via diameters required for escape
- Dramatic increase in Cu plating aspect ratio
- Solder Mask registration becoming an issue with chip scale geometries
Factors Driving Circuit Density & Cost

- Factors that will determine the break point between Conventional through hole and advanced structures:
  - Large scale use of 1.0mm BGA packages
  - Minimum component pitch (Chip scale < 0.8 mm)
  - Localized density
    - Single device with extremely high I/O (escape limited)
    - Local use of Chip Scale components
  - High density double sided designs
  - Surface Power and ground
  - Minimum drilled hole and line/space rules
  - Electrical constraints
    - Controlled length for timing
    - Line width to minimize copper loss
- The bottom line; via density is driving layer count!
MLB Layer Count vs Component Pin Density

Number of Layers vs Pins Per Square Inch

- **Total Layers**
- **Signal Layers**

Start of Exponential layer growth
1.0 mm BGA Signal Layer (42 x 42 array)

5 mil line and 5 mil space yields a channel density of 100 in./in.² outside the array

Channel density within array 25 in.in.²

Global X,Y routing efficiency greatly reduced by large arrays

Solution:
Minimize through holes
2577 I/O 1.0 mm Ceramic Column Grid Array (CCGA) Approx. package size 52mm x 52 mm (2.04” x 2.04”)

130 I/O 0.5 mm BGA Approx. package size 7.5 mm x 7.5mm (0.3” x 0.3”)

Solder Column

Packaging Trends
Enabling Technologies

Dynamic Details, Inc.
Increasing I/O Density Decreasing BGA Pitch

1.27 mm BGA package
Localized via density 62/cm² (400/in.²)

6.45 x Increase in via density

0.50 mm BGA package
Localized via density 400/cm² (2580/in.²)
### Circuit Density vs BGA Pitch (Mechanical Drill)

**Decreasing Channel Density**

<table>
<thead>
<tr>
<th>Drill diam.</th>
<th>Pad diam.</th>
<th>Line width</th>
<th>Hole density</th>
<th>Space</th>
</tr>
</thead>
<tbody>
<tr>
<td>12 mils</td>
<td>25 mils</td>
<td>5 mils</td>
<td>625/in.</td>
<td>50 in./in.^2</td>
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<tr>
<td>10 mils</td>
<td>20 mils</td>
<td>3.5 mils</td>
<td>1008/in.</td>
<td>31 in./in.^2</td>
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<tr>
<td>8 mils</td>
<td>20 mils</td>
<td>3.5 mils</td>
<td>2580/in.</td>
<td>Escape Only</td>
</tr>
</tbody>
</table>

**Technology Shift**

| 0.8 mm |
| 12 mils |
| 25 mils |
| 5 mils  |
| 400/in. |

**Increasing $**

| 0.5 mm |
| 12 mils |
| 25 mils |
| 5 mils  |
| 400/in. |

- **Drill Dia.:** 6 mils
- **Pad Dia.:** N/A
- **Line Width:** 20 mils
- **Space:** 3.5 mils
- **Hole Density:** 50 in./in.^2
- **Channel:** Escape Only!
PWB Technology Requirements

What’s Needed?

- Well characterized “FR-4” materials
- Advanced low loss dielectric materials
- Blind and Buried via’s 125 mm or less
- Copper Geometry 50 mm line & Space
- High aspect ratio copper plating 16:1 or higher

Enabling Technologies
Overview

Technology Drivers

Advanced Materials
Characterized FR-4
Hybrid Constructions
Laser Direct Imaging
High Aspect Ratio
Copper Plating
Laser Drilling
Planar Via
Technologies
## Advanced Low Loss Dielectric Laminates

<table>
<thead>
<tr>
<th>Material</th>
<th>Composition</th>
<th>Tg</th>
<th>Dielectric Constant 1 MHz 1 GHz</th>
<th>Dielectric Constant 1 MHz 2.5 GHz</th>
<th>Dielectric Constant 2.5 GHz 10 GHz</th>
<th>Dielectric Constant 2.5 GHz 10 GHz</th>
<th>Loss Tangent 1 MHz 1 GHz</th>
<th>Loss Tangent 1 MHz 2.5 GHz</th>
<th>Loss Tangent 2.5 GHz 10 GHz</th>
<th>Loss Tangent 2.5 GHz 10 GHz</th>
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<tbody>
<tr>
<td><strong>Generic FR-4 Laminates Families</strong></td>
<td></td>
<td></td>
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<tr>
<td>Tetafunctional (FR-4)</td>
<td>Epoxy/Woven: E-glass</td>
<td>135 C</td>
<td>4.7</td>
<td>4.25</td>
<td>0.025</td>
<td>0.016</td>
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<tr>
<td>Multifunctional (FR-4)</td>
<td>Epoxy/Woven: E-glass</td>
<td>150 C</td>
<td>4.6</td>
<td>4.07</td>
<td>0.025</td>
<td>0.014</td>
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<tr>
<td>High Grade Multifunctional</td>
<td>Epoxy/Woven: E-glass</td>
<td>175 C</td>
<td>4.4</td>
<td>3.9</td>
<td>0.023</td>
<td>0.012</td>
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<tr>
<td><strong>Special Purpose FR-4 Laminates</strong></td>
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<tr>
<td>Low CTE FR-4 (N4000-7)</td>
<td>Epoxy/Woven: E-Glass</td>
<td>155 C</td>
<td>4.5</td>
<td>3.9</td>
<td>0.018</td>
<td>0.017</td>
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<tr>
<td>CAF Resistant FR-4 (N4000-12)</td>
<td>Epoxy/Woven: E-Glass</td>
<td>190 C</td>
<td>3.7</td>
<td>3.6</td>
<td>0.010</td>
<td>0.008</td>
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<tr>
<td>CAF Resistant FR-4 (IS410)</td>
<td>Epoxy/Woven: E-Glass</td>
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<td>3.9</td>
<td>0.023</td>
<td>0.023</td>
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<tr>
<td><strong>(Lead Free Compatible)</strong></td>
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</table>
### Advanced Low Loss Dielectric Laminates

<table>
<thead>
<tr>
<th>Material</th>
<th>Composition</th>
<th>Tg</th>
<th>Dielectric Constant</th>
<th>Loss Tangent</th>
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<tbody>
<tr>
<td></td>
<td></td>
<td></td>
<td>1 MHz</td>
<td>1 GHz</td>
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<tr>
<td>Nelco (N7000-1)</td>
<td>Polyimide/Woven:E-glass</td>
<td>260 C</td>
<td>4.3</td>
<td>3.7</td>
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<tr>
<td>Isola (P95)</td>
<td>Polyimide/Woven:E-glass</td>
<td>260 C</td>
<td>4.4</td>
<td>4.2</td>
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<tr>
<td>Arlon (85N)</td>
<td>Polyimide/Woven:E-glass</td>
<td>260 C</td>
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<tr>
<td>Nelco (N4500-6T)</td>
<td>Epoxy/NonWoven:Aramid</td>
<td>180 C</td>
<td>3.9</td>
<td>3.5</td>
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<td>Nelco (N8000)</td>
<td>Cyanate Ester/Woven:E-glass</td>
<td>240 C</td>
<td>3.8</td>
<td>3.5</td>
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<tr>
<td>ISOLA (G200)</td>
<td>BT/Woven:E-glass</td>
<td>185 C</td>
<td>4.1</td>
<td>3.9</td>
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<tr>
<td>Nelco (N5000)</td>
<td>BT/Woven:E-glass</td>
<td>185 C</td>
<td>4.1</td>
<td>3.8</td>
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<td>Nelco (N5000-32)</td>
<td>Black BT/Woven:E-glass</td>
<td>205 C</td>
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<tr>
<td>MGC (832) Black</td>
<td>Black BT/Woven:E-glass</td>
<td>205 C</td>
<td>4.1</td>
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<td>Mitsui Chemical (BN300)</td>
<td>Black BT/Woven:E-glass</td>
<td>300 C</td>
<td>4.0</td>
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# Advanced Low Loss Dielectric Laminates

<table>
<thead>
<tr>
<th>Material</th>
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<th>10 GHz</th>
<th>1 MHz</th>
<th>10 GHz</th>
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<tr>
<td>GE GETEK</td>
<td>Epoxy-PPO/Woven:E-glass</td>
<td>180 C</td>
<td>3.9</td>
<td>0.012</td>
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<tr>
<td>Nelco N4000-13</td>
<td>Epoxy/Woven:E-glass</td>
<td>200 C</td>
<td>3.9</td>
<td>0.009</td>
<td>0.010</td>
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<tr>
<td>Nelco N4000-13 SI</td>
<td>Epoxy/Woven:Glass *</td>
<td>200 C</td>
<td>3.6</td>
<td>0.008</td>
<td>0.007</td>
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<td>Isola FR-408</td>
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<tr>
<td>Isola IS620</td>
<td>Epoxy/Woven E-Glass</td>
<td>210 C</td>
<td>3.58</td>
<td>0.0086</td>
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<tr>
<td><strong>High Frequency Laminates</strong></td>
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<tr>
<td>Rogers 4003</td>
<td>Hydrocarbon/Ceramic/Woven:Glass</td>
<td>280 C</td>
<td>3.38</td>
<td>0.0027</td>
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<tr>
<td>Rogers 4350</td>
<td>Hydrocarbon/Ceramic/Woven:Glass</td>
<td>280 C</td>
<td>3.48</td>
<td>0.0040</td>
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<tr>
<td>Rogers 4403 (Prepreg)</td>
<td>4000 Series Resin/1080 style Glass</td>
<td>280 C</td>
<td>3.2</td>
<td>0.005</td>
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<tr>
<td>Arlon 25N)</td>
<td>Ceramic Filled PTFE/Woven:Glass</td>
<td>3.5</td>
<td>0.0024</td>
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<tr>
<td>Arlon 25FR</td>
<td>Ceramic Filled PTFE/Woven:Glass</td>
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<td>0.003</td>
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### Advanced Low Loss Dielectric Laminates

<table>
<thead>
<tr>
<th>Material</th>
<th>Composition</th>
<th>Tg</th>
<th>Dielectric Constant</th>
<th>Loss Tangent</th>
</tr>
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<tbody>
<tr>
<td><strong>High Frequency Laminates</strong></td>
<td></td>
<td>10 GHz</td>
<td>10 GHz</td>
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</tr>
<tr>
<td>Isola GIGAVER</td>
<td>APPE/Woven Glass</td>
<td>210 C</td>
<td>3.52</td>
<td>0.0114</td>
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<tr>
<td>Taconics TLE-95</td>
<td>PTFE/Woven:Glass</td>
<td>2.95</td>
<td>0.0028</td>
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<tr>
<td>Taconics TLX</td>
<td>PTFE/Woven:E-glass</td>
<td>2.50</td>
<td>0.0019</td>
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<td>Taconics HT 1.5</td>
<td>Bonding Film</td>
<td>2.35</td>
<td>0.0025</td>
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<tr>
<td>W.L.Gore Speed Board N</td>
<td>Expanded PTFE/Epoxy Resin</td>
<td>2.73</td>
<td>0.0192</td>
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<tr>
<td>W.L.Gore Speed Board C</td>
<td>Expanded PTFE/Cyanate Ester</td>
<td>2.56</td>
<td>0.0038</td>
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## Advanced Low Loss Dielectric Laminates

<table>
<thead>
<tr>
<th>Material</th>
<th>Composition</th>
<th>Dielectric Constant</th>
<th>Loss Tangent</th>
</tr>
</thead>
<tbody>
<tr>
<td><strong>Microwave Laminates</strong></td>
<td></td>
<td>10 GHz</td>
<td>10 GHz</td>
</tr>
<tr>
<td>Rogers RO3003</td>
<td>PTFE/Ceramic</td>
<td>3.00</td>
<td>0.0013</td>
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<td>Rogers RO3006</td>
<td>PTFE/Ceramic</td>
<td>6.15</td>
<td>0.0025</td>
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<tr>
<td>Rogers RO3010</td>
<td>PTFE/Ceramic</td>
<td>10.2</td>
<td>0.0035</td>
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<tr>
<td>Rogers RT/duroid 5870</td>
<td>PTFE/Glass Microfiber</td>
<td>2.33</td>
<td>0.0012</td>
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<tr>
<td>Rogers RT/duroid 5880</td>
<td>PTFE/Glass Microfiber</td>
<td>2.20</td>
<td>0.0009</td>
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<tr>
<td>Rogers TMM 3</td>
<td>Hydrocarbon/Ceramic</td>
<td>3.27</td>
<td>0.0020</td>
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<td>Rogers TMM 4</td>
<td>Hydrocarbon/Ceramic</td>
<td>4.50</td>
<td>0.0020</td>
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<td>Rogers TMM 6</td>
<td>Hydrocarbon/Ceramic</td>
<td>6.00</td>
<td>0.0023</td>
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<td>Rogers TMM 10</td>
<td>Hydrocarbon/Ceramic</td>
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<td>Rogers 3001 (Bonding Film)</td>
<td>Thermoplastic</td>
<td>2.28</td>
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## Advanced Low Loss Dielectric Laminates

<table>
<thead>
<tr>
<th>Material</th>
<th>Composition</th>
<th>Tg</th>
<th>Dielectric Constant</th>
<th>Loss Tangent</th>
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<tbody>
<tr>
<td><strong>Special Purpose Micro-Via Dielectric Material</strong></td>
<td></td>
<td></td>
<td><strong>1 MHz</strong></td>
<td><strong>1 GHz</strong></td>
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<tr>
<td>Nelco 4500-6T</td>
<td>Epoxy/Resin Coated Foil</td>
<td>180°C</td>
<td>3.9</td>
<td>3.5</td>
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<td>Polyclad PCL-CF-400</td>
<td>Epoxy/Resin Coated Foil</td>
<td>165°C</td>
<td>3.5</td>
<td>3.3</td>
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<tr>
<td>Thermont</td>
<td>Random Aramid Fiber</td>
<td>180°C</td>
<td>3.9</td>
<td>3.5</td>
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<td>Nelco 1080 LD Prepreg</td>
<td>Uniform Weave 1080 (N4000-6 Resin)</td>
<td>175°C</td>
<td>4.4</td>
<td>3.9</td>
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<tr>
<td>Nelco 106 LD Prepreg</td>
<td>Uniform Weave 106 (N4000-6 Resin)</td>
<td>175°C</td>
<td>4.4</td>
<td>3.9</td>
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<tr>
<td>Gore Microlam® 610</td>
<td>Expanded PTFE/Resin</td>
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<td>Gore Microlam® 630</td>
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</table>
“Green” Materials

UK Directive

Definition of RoHS: The Restriction of Hazardous Substances in Electrical and Electronic Equipment (RoHS)

Who does it affect?

• Manufacturers, sellers, distributors and recyclers of electrical and electronic equipment containing lead, mercury, cadmium, hexavalent chromium, polybrominated biphenyls or polybrominated diphenyl ethers.

• From 1 July 2006 new electrical and electronic equipment will not contain lead, mercury, cadmium, hexavalent chromium, polybrominated biphenyls or polybrominated diphenyl ethers.
**Definition of RoHS Compliance for Materials**

<table>
<thead>
<tr>
<th>Material</th>
<th>Allowable Amount by weight</th>
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</thead>
<tbody>
<tr>
<td>Lead (Pb)</td>
<td>0.1% by weight</td>
</tr>
<tr>
<td>Cadmium (cd)</td>
<td>&lt;0.01% by weight</td>
</tr>
<tr>
<td>Mercury (Hg)</td>
<td>0.1% by weight</td>
</tr>
<tr>
<td>Hexavalent Chromium (Hex-Cr)</td>
<td>&lt;0.1% by weight</td>
</tr>
<tr>
<td>Polybrominated Biphenyls</td>
<td>0.1% by weight</td>
</tr>
<tr>
<td>(PBB – fire retardant)</td>
<td></td>
</tr>
<tr>
<td>Polybrominated Diphenyl Ethers</td>
<td>0.1% by weight</td>
</tr>
<tr>
<td>(PBDE- fire retardant)</td>
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### “Green” Materials

<table>
<thead>
<tr>
<th>Material</th>
<th>Resin System</th>
<th>(DSC) Tg</th>
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*Mitsubishi Gas Chemical
"Lead Free” Materials

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**Lead-Free Assembly**  Passes 6x @ 288 degrees C  
**Robust Thermal Stability**
Dynamic Details, Inc.

“Lead Free” Solder Profile

Enabling Technologies

Solder Re-Flow Profile

- Higher temperature & dwell time exceed current FR-4 process limits
- Materials with higher Tg, Low Z axis CTE and improved T-288 resistance will be required
Enabling Technologies

Overview

Technology Drivers

Advanced Materials

Characterized FR-4

Hybrid Constructions

Laser Direct Imaging

High Aspect Ratio

Copper Plating

Laser Drilling

Planar Via Technologies

Dynamic Details, Inc.
Factors that influence dielectric constant and loss tangent:

- Signal frequency
- Temperature
- Moisture content
- Glass composition
- Ratio of epoxy resin to glass in the construction
Dielectric Properties of “FR-4” Laminate

Dielectric constant with respect to frequency

Signal frequency in MHz

Epoxy resin content

- 40%
- 50%

Source: D. Heywood, “Controlled Impedance PCB’s from FR4 Material”, Isola Werke UK LTD report
Dielectric Properties of “FR-4” Laminate

Dielectric Constant with respect temperature @ 1 MHz

Source: D. Heywood, “Controlled Impedance PCB’s from FR4 Material”, Isola Werke UK LTD report
Dynamic Details, Inc.

Dielectric Properties of “FR-4” Laminate

Dissipation Factor with respect to temperature @ 1.0 GHz

Data Source: Park-Nelco
Dielectric Properties of “FR-4” Laminate

Dielectric constant with respect to frequency & moisture content

FR-406
44.6 % epoxy resin

Data Source: Isola
Dielectric Constant of “FR-4” Laminate

Considerations:

- Standard “FR4” epoxy-glass laminates can maintain a dielectric constant tolerance of less than +/- 0.2 based on a specific laminate construction and resin content.

- Standard tolerance on prepreg resin content is +/- 1.5% as supplied by vendors, +/- 1.0% can be attained for critical applications (special order).

- Resin content in prepreg varies for each style of prepreg.

- Prepreg resin content is reduced in high pressure lamination due to flow in the melt phase.
Epoxy-Glass Laminate Construction

- Dielectric constant of the composite laminate is a function of the resin/glass ratio
- Composite laminates can have many different resin/glass constructions

PWB Cross-Section

Copper Foil

Woven glass fabric
High dielectric constant \((e_r \approx 6)\)

Epoxy resin
Low dielectric constant \((e_r \approx 3.5)\)

Photo Courtesy of Park Nelco
### Epoxy-Glass Laminate Construction

Standard glass fabrics used in the construction of Prepreg & Laminate

<table>
<thead>
<tr>
<th>Glass</th>
<th>Count Warp</th>
<th>Count</th>
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Enabling Technologies

Dynamic Details, Inc.

Epoxy-Glass Laminate Construction

Glass Style: 106
Plain Weave
Count: 56x56 (ends/in)
Thickness: 0.0015”

Glass Style: 1080
Plain Weave
Count: 60x47 (ends/in)
Thickness: 0.0025”

NOTE:
The plain weave yarn consists of yarns interlaced in an alternating fashion one over and one under every yarn.

Source: Isola
Epoxy-Glass Laminate Construction

Glass Style: 2113
Plain Weave
Count: 60x56 (ends/in)
Thickness: 0.0029”

Glass Style: 2116
Plain Weave
Count: 60x58 (ends/in)
Thickness: 0.0038”

Source: Isola
Dynamic Details, Inc.

Enabling Technologies

Epoxy-Glass Laminate Construction

Glass Style: 1652
Plain Weave
Count: 52x52 (ends/in)
Thickness: 0.004”

Glass Style: 7628
Plain Weave
Count: 44x32 (ends/in)
Thickness: 0.0068 (in)

Source: Isola
## Dielectric properties based on construction & frequency (N4000-6)

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<th>Tolerance</th>
<th>Construction</th>
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<th>1GHz Tol.</th>
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Data Source: Park Nelco
## Epoxy Glass Laminate Properties N4000-13

### Dielectric properties based on construction & frequency (N4000-13)

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**Dielectric properties based on construction & frequency (N4000-13)**

Data Source: Park Nelco

To m Buck 1-2004
**Epoxy Glass Laminate Properties N4000-13 SI**

**Low loss epoxy resin system & low loss/dielectric constant SI glass**

<table>
<thead>
<tr>
<th>Thickness</th>
<th>Tolerance</th>
<th>Construction</th>
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Data Source: Park Nelco
### Controlled Material Stack-up

#### Impedance Requirements:

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<th>L.#</th>
<th>Impedance Type</th>
<th>Orig Line</th>
<th>Fin. Line</th>
<th>Ref Pln</th>
<th>2nd Ref Pln</th>
<th>Z ohms +/- Diff Line Centers</th>
<th>Coplanar Spacing</th>
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<td>6</td>
<td>100.0 +/- 10% 00800</td>
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#### Lamination Stackup:

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<th>Thickness and Tolerances: Cu: Laminates/PrePreg:</th>
<th>Base Material Reqmts: Type: Description:</th>
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<th>X</th>
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Enabling Technologies

Overview

Technology Drivers

Advanced Materials
Characterized FR-4

Hybrid Constructions

Laser Direct Imaging
High Aspect Ratio Copper Plating

Laser Drilling
Planar Via Technologies
Dynamic Details, Inc.

Advanced Low Loss Dielectric Laminates

Relative Laminate Cost Per Square Foot vs Loss Tangent

- Radar Collision Avoidance
- Satellite Communications
- Cellular & PCS Base Station LPAs
- Wireless Cable TV
- Mmwave

Satellite earth terminals
High Speed Digital Backplanes
VSAT

RT/duriod 6000's
RT/duriod 5880 (type GR)

GX/ WGT
Comm PTFE
Ceramic

Thermosets
Comm WGT PTFE

Cellular Handsets
Base Station/WLL Antennas
Personal Communication Systems
Wireless PBS and LAN Pagers

Cyanate Ester
Polyester
BT-Epoxy
PPO/Epoxy
FR4

Based on 0.020” Laminate

Source: Rogers
Mixed dielectric constructions reduce cost by only using more expensive low loss materials where needed.

- FR-4 Epoxy-Glass Sub-Cores provide structural support when using PTFE based laminates.

Typical mixed dielectric construction with low loss cap layer.
Mixed Dielectric Circuit Constructions

Mixed Dielectric: Rogers 4350/FR-4

Cross-Section

Roger 4350
FR-4
Dynamic Details, Inc.

Mixed Dielectric Circuit Constructions

Enabling Technologies

Mixed Dielectric:
Rogers 4350/Rogers TMM 6

Cross-Section

Roger 4350
0.040” Thick

Rogers TMM 6
0.200” Thick
Conduction Cooled Circuit Constructions

PWB Thermal Path Considerations:

- Conduction cooling allows heat to be removed through the PWB
- Conduction cooling with integral core constructions provide thermal paths in one or more of the following ways:
  - Provide heat spreading through the core using the PWB as a radiating surface
  - Using thermal via’s a conducting path can be established from components to the core
  - Heat can be conducted to the edge of the card and be removed by exposing the core and connecting to an external heat sink
  - Thermal vias can be used to establish a thermal connection from the core to surface edge rails and connect to an external heat sink
Copper core constructions:

- Copper conductivity 385 W/m*K
- Copper core CTE 17 ppm/C
- Epoxy laminate conductivity 0.3 W/m*K
Copper core constructions:

- Copper conductivity 385 W/m*K
- Copper core CTE 17 ppm/C
- Epoxy laminate conductivity 0.3 W/m*K
Conduction Cooled Circuit Constructions

Copper core constructions:
- Copper conductivity 385 W/m*K
- Copper core CTE 17 ppm/C
- Epoxy laminate conductivity 0.3 W/m*K
## Conduction Cooled Circuit Constructions

### Diagram Specifications:
- **Layer 1:** 50 ohms
- **Layer 2:** 50 ohms
- **Layer 3:** 50 ohms
- **Layer 4:** 50 ohms
- **Layer 5:** 50 ohms
- **Layer 6:** 50 ohms
- **Layer 7:** 50 ohms
- **Layer 8:** 50 ohms
- **Layer 9:** 50 ohms
- **Layer 10:** 50 ohms
- **Layer 11:** 50 ohms
- **Layer 12:** 50 ohms
- **Layer 13:** 50 ohms
- **Layer 14:** 50 ohms
- **Layer 15:** 50 ohms
- **Layer 16:** 50 ohms
- **Layer 17:** 50 ohms
- **Layer 18:** 50 ohms
- **Layer 19:** 50 ohms
- **Layer 20:** 50 ohms

### Copper Core Specifications:
- Core clearance drill
- Dielectric filler
- Isolated signal via
- Thermal Via

### Copper Core Details:
- 0.032 thickness

### Conduction Cooldown Technology:
- Enabling Technologies
### Thermal Mechanical Properties of Core Materials

<table>
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<tr>
<th>Raw Material</th>
<th>Thermal Conductivity (W/m*K)</th>
<th>CTE (ppm/C)</th>
<th>Density (g/cm³)</th>
<th>Tensile Modulus (msi)</th>
<th>Dielectric Constant (εr)</th>
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Stable values represent data of raw fibers.

Data Source: Thermal Works
Low CTE High Conductivity StablCor™ Laminate

Standard weave pitch based carbon fiber fabric

- High thermal conductivity
- Negative coefficient of thermal expansion
- Extremely high modulus of elasticity

Design Considerations:
- Carbon fiber fabric is electrically conductive
- Both copper planes must be treated as the same potential
- Split planes are made by mechanically routing resulting in loss of thermal path
- Laminate must be pre-drilled to provide electrical clearance
- Optimum designs, dielectric thickness should not exceed 0.015” from the top of core
- CTE will be based on volume metric ratio of StableCor and Copper/Dielectric materials
StablCor Constructions:
• StablCor conductivity 10-1000 W/m*K
• StablCor CTE –1.15 ppm/C
• Epoxy laminate conductivity 0.3 W/m*K
Low CTE Conduction Cooled Circuit Constructions

StablCor Constructions:
- StablCor conductivity 10-1000 W/m*K
- StablCor CTE –1.15 ppm/C
- Epoxy laminate conductivity 0.3 W/m*K
Dynamic Details, Inc.

Low CTE Conduction Cooled Circuit Constructions

Enabling Technologies

* > 124.9°F

* < 68.0°F

Standard FR-4 1 Gbit memory

StablCor 1 Gbit memory

Graphic Source: Thermal Works
Low CTE Conduction Cooled Circuit Constructions

StablCor Constructions:
- StablCor conductivity 10-1000 W/m*K
- StablCor CTE –1.15 ppm/C
- Epoxy laminate conductivity 0.3 W/m*K
Overview

Technology Drivers

Advanced Materials
Characterized FR-4
Hybrid Constructions

Laser Direct Imaging

High Aspect Ratio
Copper Plating
Laser Drilling
Planar Via
Technologies
Conventional Photo Printing Process

Laser plot Mylar photo tools

Expose circuit image using Mylar photo tools
Conventional Photo Printing Process

Engineering Considerations
- Alignment of upper and lower tools
- Alignment of tools to substrate
- Scaling of photo tools
- Geometric compensation
- Temperature stability of tools while photo printing
The minimum photo tool opening is limited by the ability to fully remove un-exposed resist in the narrow gap between traces.
Enabling Technologies

Dynamic Details, Inc.

Laser Direct Imaging (LDI)

Elimination of Photo Tools

- No Film/Artwork Movement
- Quick Turn Made Easy
  - Run product as soon as Engineering releases data to the floor
- Reduction in Defect Count.
  - Direct Write = No Film related defects
  - No issues related to loss of vacuum

Orbotech DP-100

Scanning Optics
Laser Direct Imaging (LDI)

- Improved Resolution
  - System Resolution 4000 dpi
  - System Capability: 50µm/50µm (.002”/.002”) Line & Space

- Improved Registration
  - CCD Camera System & Target Fiducials
    - Through Holes Drilled
    - 24 Hole Pattern of Laser Drilled Microvia
      - System capability
        - Positional Accuracy +/-25µm

- LDI Solder Mask
  - Beta testing is in progress on Taiyo LDI SM
Using CCD Cameras and Mechanical or Laser Drilled Fiducials it is possible to get perfect registration every time.
Using Laser Imaging it is possible to achieve finer resolution without the impact to yield that is experienced in contact printing using Photo Tools.

Laser Direct Imaging (LDI)

Improved Image Quality with LDI

Printing Defects Using a Photo Tool

1.5 mil Track and Gap in Manufacture
Dynamic Details, Inc.

Laser Direct Imaging (LDI)

Enabling Technologies

Vertical

Horizontal

50µm/50µm (.002"/.002")

Shipley LD 730 Photo Resist
Using the DP-100 Registration Features and Data Scaling Option it is possible to register a 4 mil pad to a 2 mil via without ‘Break Out’ in production using a 20 x 16” manufacturing panel.
Dynamic Details, Inc.
Laser Direct Imaging (LDI)

Precise Inner Layer Registration

24 Layer PCB Cross-Section
Dynamic Details, Inc.

Laser Direct Imaging (LDI) Solder Mask

- Laser Direct Imaged Solder Mask
  - Adaptively tooled
  - Improved Registration +/- 0.001” vs +/- 0.003”

Standard LPI Solder Mask
+/- 0.003”

Laser Defined Solder Mask
+/- 0.001”
Enabling Technologies

Overview

Technology Drivers
- Advanced Materials
- Characterized FR-4
- Hybrid Constructions
- Laser Direct Imaging

Advanced Materials
- Characterized FR-4

Hybrid Constructions
- High Aspect Ratio Copper Plating
- Laser Drilling
- Planar Via Technologies
High Aspect Ratio Pulse Plating

- **Equipment**: Complex Waveform (WST) Pulse
- **Process**: Mixed Frequency WST
  - Max effect on mixed feature on boards
  - Wide operating window
- **Chemistry**: MACuSPEC from MacDermid
## Typical Plating Capabilities

<table>
<thead>
<tr>
<th>Description</th>
<th>Aspect ratio</th>
<th>Via/Hole Diameter</th>
<th>Dielectric/Board Thickness</th>
</tr>
</thead>
<tbody>
<tr>
<td>Microvia</td>
<td>0.5:1</td>
<td>100 µm (.004”)</td>
<td>50 µm (.002”)</td>
</tr>
<tr>
<td>PTH</td>
<td>8:1</td>
<td>200 µm (.008”)</td>
<td>1.75 mm (.062”)</td>
</tr>
<tr>
<td>PTH</td>
<td>10:1</td>
<td>337.5 µm (.0135”)</td>
<td>3.4 mm (.135”)</td>
</tr>
</tbody>
</table>
### Pulse Plating Capabilities

<table>
<thead>
<tr>
<th>Description</th>
<th>Aspect ratio</th>
<th>Via/Hole Diameter</th>
<th>Dielectric/Board Thickness</th>
</tr>
</thead>
<tbody>
<tr>
<td>Microvia</td>
<td>0.6:1 1:1(^2)</td>
<td>100 µm (.004”)</td>
<td>100 µm (.004”)</td>
</tr>
<tr>
<td>PTH</td>
<td>11:1 14:1</td>
<td>200 µm (.008”)</td>
<td>2.8 mm (.112”)</td>
</tr>
<tr>
<td>PTH</td>
<td>14:1 16:1</td>
<td>337.5 µm (.0135”)</td>
<td>5.4 mm (.216”)</td>
</tr>
</tbody>
</table>

**Notes:**

1. Capabilities have been proven! Consult DDI engineering.
2. Requires special process and may not work on all applications.
High Aspect Ratio Pulse Plating

Aspect Ratio = 14:1
Thickness 2.8mm (.112”)
Drill dia. 200 µm (.008”)

Controlled depth mechanical drilling
Dynamic Details, Inc.

High Aspect Ratio Pulse Plating

Aspect Ratio = 16:1  Thickness = 5.4mm (.216”)  Drill dia. = 337.5 µm (.0135”)

36 Layer MLB
Dynamic Details, Inc.

High Aspect Ratio Pulse Plating

Laser drilled microvia's Aspect Ratio 0.5:1
Enabling Technologies

Overview

Technology Drivers
Advanced Materials
Characterized FR-4
Hybrid Constructions
Laser Direct Imaging
High Aspect Ratio
Copper Plating
Laser Drilling
Planar Via Technologies
Laser Drilling Technology & Microvias

What is considered a Microvia?

- Generally microvia’s are considered to be blind holes that terminate to a lower layer without the need to generate a sub-lamination.
- Hole diameters range from 3 to 8 mils and are typically in the 4 to 6 mil range.
- Hole depth is limited by copper plating aspect ratio, typically 0.5: to 0.6:1 however higher aspect ratios have been achieved.
- Most common method for hole formation is laser drilling with YAG lasers.
- Microvia’s terminate to the underlying pad without penetrating the copper.
Common High Density Via Structures

- 1:3 \( \mu \)Via
- 1:2 \( \mu \)Via
- 1:3 Stacked plate fill \( \mu \)Via
- Through hole
- 1:2 Plate fill \( \mu \)Via
- HDI Dielectric
- 2-4-2 HDI Substrate

2 Layer HDI buildup

4 Layer MLB core

1:2 \( \rightarrow \) 2:3 Staircase \( \mu \)Via

Buried via
Conventional MLB vs HDI

0.8 mm μBGA

Conventional MLB Substrate

Laser drilled via in pad
(Solder mask defined attachment pad layer # 1)

Solder mask defined pad

Laser drilling technology

0.8 mm

HDI Substrate

Signal routing on layer # 2

Mechanical drilled via’s offset from attachment pad
Microvias in SMT Pads

- Laser Drilled Microvias
- Via location does not impact assembly due to its extremely small volume

0.5 mm
Common Laser Drilling Techniques

- **ND:YAG (Ultra-Violet)**
  Capable of drilling copper, all re-enforcing materials and all laminate resin systems. 25 to 50 micron beam forms holes by spiraling of trepaning the beam.

- **CO₂ (Infrared)**
  Capable of drilling most re-enforcing materials and laminate resin systems. Not effective for drilling copper (copper is reflective in the infrared spectrum). Forms holes by pulsing a larger high energy beam.

- **Combination ND:YAG CO₂ forms**
  Holes by removing copper with the ND:YAG laser and the dielectric and re-enforcing material with the CO₂ laser.
Laser Drilling Technology

Typical laser drilled Microvia geometry

Laser drilled Microvia
Layer 1 to 2

Laser drilled Microvia
Layer 1 to 3

Note: Typical aspect ratio on laser drilled holes is 0.5:1 to 0.7:1 max
Factors Impacting Laser Drilling Time & Cost

- Copper foil thickness
- Dielectric thickness
- Hole diameter
- Dielectric composition
  - Non-reinforced resin (RCC)
  - Non-woven reinforcement (Thermont ®)
  - Woven (106, 1080 glass)
- System Optimization = increases velocity and power
Typical ND:YAG Laser Drilling Speeds

<table>
<thead>
<tr>
<th>Cu Thick.</th>
<th>Via Dia.</th>
<th>Drilling Speed Holes/sec.</th>
</tr>
</thead>
<tbody>
<tr>
<td>9 µm</td>
<td>100 µm</td>
<td>76</td>
</tr>
<tr>
<td>9 µm</td>
<td>150 µm</td>
<td>47</td>
</tr>
<tr>
<td>9 µm</td>
<td>200 µm</td>
<td>30</td>
</tr>
</tbody>
</table>
Routing Channel Density vs. Via Structure

Standard through hole technology:
- Channel density limited by via density,
  geometry and pitch

Blind & Buried via’s:
- Channel density enhanced
- Still geometry limited
- Limited Z axis connectivity

Microvias:
- Channel density enhanced
  through smaller geometry
  Limited Z axis connectivity

SMV:
- Channel density enhanced
  through smaller geometry
  Unlimited Z axis connectivity

Once you leave through hole designs
the goal is to find the via combination
that maximizes routing channel density
at the lowest cost
Routing Channel Density vs. Via Structure

- Increased channel density on lower sub lamination
- Standard PTH geometry apply, reduced aspect ratio on sub drill
- Anti-pad diameter must account for tolerance buildup in multiple laminating cycles
- Increased channel density on sub lamination
- Standard PTH geometry apply, reduced aspect ratio on sub drill
- Anti-pad diameter must account for tolerance buildup in multiple laminating cycles
- No Z axis connectivity between adjacent sub-laminations
Routing Channel Density vs. Via Structure

- Increased channel density on layer 1 and 2 from reduced geometry
- Increased channel density on layers n-1 to n resulting from a blind hole
- Standard PTH geometry apply to mechanical drilled holes
- Dielectric thickness layer 1:2 limited by plating aspect ratio (0.5:1 to 0.6:1)
Dynamic Details, Inc.
Microvia Through Hole Combo 1.0 mm

- 3 Track routing layer 2
- Ball pad
- 12 mil capture pad
- 2 Track routing layer 1
- Laser drilled hole
- High density Routing layer
- 30 mil anti-pad
- 2 Track routing Between PTH pads
- Plated through hole 10 mil drill, 20 mil pad
Dynamic Details, Inc.

Microvia: 0.8 mm BGA Signal Routing

Microvia in pad used to enhance escape on high density BGA's

1+6+1 HDI Structure

0.8 mm BGA

Enabling Technologies
Dynamic Details, Inc.

Microvia Through Hole Combo 0.8 mm

- Two track routing
  - Layer 2
- Ball pad
- High density
  - Routing layer
- One track routing
  - Layer 1
- 0.8 mm
- 10 mil drill
- 20 mil pad
- 1 mm pitch
- 3 mil max.
- No limit!
Laser Drilling Technology

- Interstitial Microvia
- Two track signal routing on surface
- 1.0 mm BGA
- Microvia in pad
- Thermount Dielectric
Dynamic Details, Inc.
Laser Drilling Technology

Enabling Technologies

39 x 39 1.0 mm BGA

Layer 1 Signal Routing

1.0 mm
Dynamic Details, Inc.

μvia & Buried & PTH 1.0 mm Pitch (Full Offset)

- Ball pad
- Laser drilled hole
- Buried via (2:N-1)
- PTH 10 mil drill 20 mil pad
- 30 mil anti-pad
- 12 mil capture pad
- 3 mil Max

No limit!
μvia & Buried & PTH Via’s 1.0 mm (Min Offset)

- Ball pad
- Laser drilled hole
- Buried via (2:N-1)
- 12 mil capture pad
- 30 mil anti-pad
- One track Route Between Capture pad and buried via
- PTH 10 mil drill, 20 mil pad
Dynamic Details, Inc.

Laser Drilling Technology

Enabling Technologies

0.8 mm BGA

Via in pad

Offset via

Interstitial Microvias Layer 1 to 2
Microvia Through Hole & Buried Combo 0.8 mm

- Buried via
  - 8 mil drill
  - 18 mil pad

- Ball pad

- One track between PTH's

- One track routing
  - Layer 2 on 45 degree

- 0.8 mm

- 10 mil drill
  - 20 mil pad
  - 1 mm pitch

- 3 mil max.
  - No limit!
Microvia Applications For Power and Ground

- Ground Via
- Microvia Ground Connections
- RF Ground Plane
- Analog & RF Side
- Digital Side
Dynamic Details, Inc.

Microvia Through Hole & Buried Combo 0.8 mm

- Buried via
  - 8 mil drill
  - 18 mil pad

- Ball pad
- No Via

- Plane Connection
  - 10 mil drill
  - 20 mil pad
  - 1 mm pitch

- One track routing

- 0.8 mm

- One track between PTH's

- Plane Connection
  - 3 mil max.

- No limit!
Dynamic Details, Inc.
Microvia “Stair Case” & Buried Combo 0.8 mm

Enabling Technologies

- Buried via
  - 10 mil drill
  - 20 mil pad

- Ball pad
  - 10 mil drill
  - 20 mil pad
  - 1 mm pitch

- One track between
  - PTH’s

- One track routing
  - Between “Stair Case”

- 3 mil max.
Enabling Technologies

Microvia “Stair Case” & Buried Combo 0.8 mm

- Buried via: 10 mil drill, 20 mil pad
- Plane Connection: 0.8 mm
- 10 mil drill, 20 mil pad, 1 mm pitch
- Plane Layer two
- “Stair-Case” Connection through a plane layer
- One track between PTH’s
- 3 mil max.
Dynamic Details, Inc.
Laser Drilling Technology

Enabling Technologies

Laser drilled via’s
Mechanically drilled via

0.8 mm BGA

0.8 mm BGA

Tin/Lead Surface Finish
Dynamic Details, Inc.

Using Microvia’s For Power & Ground

Enabling Technologies

Signal Via

Power Via

Layer 1 & 8
“Ground Flood”

Internal escape pad
within power layer

1.0 mm BGA

Copper “Ground Flood”
under LPI Solder mask
Dynamic Details, Inc.

Microvia Geometry (Surface Power And Ground)

- Signal Pad
- Ground Pad
- Power Pad

Layer 1
Layer 2

Microvia layer 1:2

Side View
Enabling Technologies

Dynamic Details, Inc.

Using Microvia’s For Power & Ground

Layer 1: Ground

Layer 2: Power

Layer 3: Signal

Layer 4: Ground

Through holes eliminated by Microvia P&G connections

Antipads for buried PTH Signal connections
Increased Density: Microvia’s Replace PTH P&G

5 channels at 5/5 line/space or
6 channels at 4/4.5 lines/space

Microvia’s used on External power and ground layers eliminate through holes and double the effective pitch.

12 mils
39.37 mils
24 mils
Enabling Technologies

Overview

Technology Drivers

- Advanced Materials
- Characterized FR-4
- Hybrid Constructions
- Laser Direct Imaging
- High Aspect Ratio
- Copper Plating
- Laser Drilling
- Planar Via Technologies
Potential Assembly Issues With Via In Pad:

- Microvias vias in pad from layer 1 to 2 must have minimum volume after plating to prevent and or minimize solder voiding due to trapped volatiles
- Even with minimum microvia volume an optimized solder profile is often necessary
- Microvia diameters for connecting layer 1 to 3 or greater are in all cases too large for via in pad
- Potential joint reliability issue with large ceramic devices with via in pad when no escape pattern is used “Dog Bone” due to large CTE mismatch to the organic substrate
Laser Drilling Technology Via In Pad

Ideal Solder Joint

Chip Scale BGA Package with Microvia in Pad
Laser Drilling Technology Via In Pad

X-Ray of BGA site

Solder void within a solder ball at via in pad location
Laser Drilling Technology Via In Pad

Unacceptable Via In Pad Solder Joints
DDI Planar Via Technologies”

Technology Drivers For Planar Via-In-Pad:

- Eliminate potential solder voiding in Via-In-Pad applications
- Address Via-In-Pad applications for multilayer HDI structures (i.e. 1:3, 1:4 connections) while maintaining low aspect ratio plating
- High capacitance low inductance HDI power structures
- Via-In-Pad capability with RF laminates greater than 0.002” thick
- Effective use of embedded resistors on HDI layers

- Process Technologies
  - PTH Conductive fill and Cu plate
  - PTH Non-Conductive fill and plate
  - Planar Cu fill microvia
  - Planar Cu fill Stacked MicroVia “SMV”
VIA Fill For Plated Through Holes

Via Filling Process

- Mechanical Drilling
- Copper Plating
- Screen via fill Planarize
- Secondary Copper Plate

- Dupont CB100 Conductive via fill (sliver filler)
- Taiyo TR7901 Conductive via fill (silver filler)
- Methode 1210 Conductive via fill (silver filler)
Enabling Technologies

Conductive Via Fill For PTH

Cross-section with conductive via fill (Taiyo TR7901 Silver filled)

Surface view (X,Y) after via filling and before Cu plating

Surface copper foil

Conductive Via fill

Small voiding typ.
Copper plated hole barrel

S rill voiding typ.
Enabling Technologies

Dynamic Details, Inc.

Conductive Via Fill For PTH

Cross-Section

View of surface

Electroplated surface

CB-100 Conductive via fill

Component land pad
DDI Stacked Microvia’s “SMV”

Stacked Microvia’s Attributes:

• Provides a solid copper fill eliminating potential solder voiding
• Improved assembly for Chip Scale components
• Improves routing density for Fine Pitch BGAs (0.65 mm & 0.5 mm)
• Allows routing out on multiple layers with 0.010” Pad diameters
• Maximize copper on plane layers
• Lower inductance when compared to “staircase” and offset via’s
Laser Drilled Via’s: Plated Cu Fill

Laser drilled via’s with Cu plate fill

- 0.004” laser drilled via with Cu plate fill
- 0.008” diameter surface pad

Surface pad
Copper Fill
Layer 2
capture pad
BGA Land pads with planar copper surface & Immersion Nickel Gold

Planar Surface for 0.8 mm BGA
### Microvia Technology with Planar Cu Fill

- **.002” trace & space**
- **Laser Direct Image (LDI)**

#### Layer Specifications

<table>
<thead>
<tr>
<th>Layer</th>
<th>Material</th>
<th>Thickness</th>
<th>Aspect Ratio</th>
<th>Pad Width</th>
</tr>
</thead>
<tbody>
<tr>
<td>Layer 1</td>
<td>FR4</td>
<td>.002</td>
<td>0.4 mm</td>
<td>.008</td>
</tr>
<tr>
<td>Layer 2</td>
<td>FR4</td>
<td>.006</td>
<td>0.5:1</td>
<td>.010</td>
</tr>
<tr>
<td>Layer 3</td>
<td>FR4</td>
<td>.006</td>
<td></td>
<td></td>
</tr>
<tr>
<td>Layer 4</td>
<td>FR4</td>
<td>.006</td>
<td></td>
<td></td>
</tr>
<tr>
<td>Layer 5</td>
<td>FR4</td>
<td>.006</td>
<td></td>
<td></td>
</tr>
<tr>
<td>Layer 6</td>
<td>FR4</td>
<td>.002</td>
<td></td>
<td></td>
</tr>
</tbody>
</table>

**Solder mask clearance for Flip Chip Area**: .001/side

**Solder mask**

**Finish Thickness**: .036 +/- .003

**Material**: N4000-13  
**Tg**: 210°C

**Utilize Laser Direct Image (LDI) Solder mask**

**.004 Laser drill**

**Plate Fill**

**0.5:1 aspect ratio**

**L1 = .008 Pad**

**L2 & 5 = .010 Pad**
SMV Geometry (Offset Buried Via)

1:2 Microvia

Full offset “Dog Bone”

Layer 1
Layer 2
Layer 3
Layer 4

1:3 SMV Connecting layer 1 to the “Dog Bone” on layer 3 and mechanically drilled hole to layer 4

0.5mm

Side View

10 mil Hole

Stripline layer
Applications For Planar Cu filled Via’s

1-8-1: Offset laser drilled via over conductive filled buried via’s

- Layer 2 - 9 = Buried Vias 0.020” pad & 0.010” drill Conductive Via Fill
- Layer 1 - 2 & 9 - 10 Microvias L1 & 10 = 0.010” pad 0.006” laser drill
- Layer 1 - 10 through Vias 0.020” pad & .010” drill

Layer 1 & 2 - 9 & 10 3/8 oz copper if trace and space <0.004”
Dynamic Details, Inc.

SMV Geometry (Minimum Offset)

Enabling Technologies

Layer 1
Layer 2
Layer 3
Layer 4

BGA Land Pad
Anti-Pad

0.5mm

4 mil SMV, 10 mil pad

10 mil hole 20 mil pad

1.0mm
Applications For Planar Cu filled Via’s

1-8-1: Laser drilled via over conductive filled buried via’s

Layer 1 - 2 & 9 – 10
Microvias
L1 & 10 = 0.010” pad
0.006” laser

Layer 2 - 9 = Buried Vias
.020” pad & .010” drill
Conductive Via Fill

Layer 1 - 10 through Vias
.020” pad & .010” drill

3/8 oz copper if trace and space <.004”
SMV Geometry (Conductive Via Fill And Plate)

- **4 mil SMV via**
- **10 mil BGA Pad's**
- **Layer 1**
- **Layer 2**
- **Layer 3**
- **Layer 4**

- **0.5mm**
- **30 mil Anti-pad**
- **10 mil Mechanically drilled hole**
- **20 mil pad with conductive via fill**
Dynamic Details, Inc.

Applications For SMV Technology

2-4-2: Stacked microvia using planar Cu fill

Layer 1 - 2 & 8-7 = Microvias
L1 .010” pad & .004” laser drill

Layer 2 – 3 & 6 - 7 = Microvias
0.010” pad & 0.004” laser drill

Layer 1 - 8 = Through-hole
0.022” pad & 0.012” drill

Layer 3 - 6 = Buried Vias
0.022” pad & 0.010” drill

Buried via holes to be filled with non-conductive epoxy
Layer 4 – 5 buried via 0.016” pad & 0.008” drill
Conductive Fill
Planar & Plate

Stacked Microvias
Laser drilled 0.004”
0.008” pad
Plate – Filled

Finish Thickness = 0.062 +/- 0.005 Material = Nelco N4000-6FC 175°C Tg
SMV Geometry (Multilayer signaling)

- **Ground Connection**
- **BGA Land Pad**
- **Layer 1**
- **Layer 2**
- **Layer 3**
- **Layer 4**
- **Layer 5**
- **Minimal plane voiding**
- **Power Connection**
- **3 mil line**
- **3.6 mil space**
- **Anti-Pad**
- **0.5mm**
+4 Stacked Microvia Construction

Vertical stacked via’s access 5 interconnect layers
Applications For SMV Technology

0.016” pad
0.008” drill

Dual Stripline .00275” trace = 50 ohms
Coated Microstrip 0.0025” trace = 60 ohms
0.004” trace = 50 ohms

Finish Thickness = 0.050 +/- 0.005 Material = High Performance FR4 210°C Tg
Applications For SMV Technology

- Seven layers for fan-out of 0.65 mm, 0.5 mm & 0.4 mm BGAs
- 0.5 mm = .010” diameter pad using a .004” laser drill, 0.003” trace & 0.0033 space
- 0.008” diameter pad using .004” laser drill is also available
- 0.4 mm = .008” diameter pad, .004” laser drill, .0026” trace & space

Capable of creating a 14 Layer stacked configuration
Dynamic Details, Inc.

Applications For SMV Technology

Stacked Microvias
Layer 1 - 2
Layer 2 - 3
Layer 3 - 4
Layer 4 - 5
Layer 5 - 6
Layer 6 - 7
0.010” pad
0.004” laser drill

Buried Vias
Layer 7 - 8
0.016” pad
0.006” drill
Fill with conductive epoxy

Stacked Microvias
Layer 9 - 8
Layer 10 - 9
Layer 11 - 10
Layer 12 - 11
Layer 13 - 12
Layer 14 - 13
0.010” pad
0.004” laser drill

Layer 1 - 14 = Through-hole
0.020” pad & 0.010” drill

Layer 4 - 11 = Buried Vias
Layer 6 – 9 = Buried Vias
0.022” pad & 0.010” drill

Solder mask

Finish Thickness = .062” +/- .006”
Material = High Temperature FR4 175° C Tg
### SMV Design Rules

#### Laser Drilled SMV Layer 1 to 2 & 2 - 3

<table>
<thead>
<tr>
<th>#</th>
<th>Description</th>
<th>Standard SMV</th>
<th>Advanced SMV</th>
</tr>
</thead>
<tbody>
<tr>
<td>A</td>
<td>Minimum Layer 1 copper thickness</td>
<td>1.8</td>
<td>1.8</td>
</tr>
<tr>
<td></td>
<td></td>
<td>20%</td>
<td>10%</td>
</tr>
<tr>
<td>B</td>
<td>Minimum Layer 2 copper thickness</td>
<td>1.6</td>
<td>1.6</td>
</tr>
<tr>
<td></td>
<td></td>
<td>20%</td>
<td>10%</td>
</tr>
<tr>
<td>C</td>
<td>Layer 1 – 2 dielectric thickness</td>
<td>2.0</td>
<td>3.0</td>
</tr>
<tr>
<td></td>
<td></td>
<td>10%</td>
<td>10%</td>
</tr>
<tr>
<td>D</td>
<td>Minimum Layer 2 pad for Layer 1 to 2 Microvia</td>
<td>10</td>
<td>8</td>
</tr>
<tr>
<td></td>
<td></td>
<td>NA</td>
<td>NA</td>
</tr>
<tr>
<td>E</td>
<td>Minimum Layer 1 pad for Layer 1 to 2 Microvia</td>
<td>8</td>
<td>8</td>
</tr>
<tr>
<td></td>
<td></td>
<td>NA</td>
<td>NA</td>
</tr>
<tr>
<td>F</td>
<td>Minimum Layer 1 pad for Stacked Microvia</td>
<td>8</td>
<td>8</td>
</tr>
<tr>
<td></td>
<td></td>
<td>NA</td>
<td>NA</td>
</tr>
<tr>
<td>G</td>
<td>Minimum Layer 2 pad for Stacked Microvia</td>
<td>10</td>
<td>8</td>
</tr>
<tr>
<td></td>
<td></td>
<td>NA</td>
<td>NA</td>
</tr>
<tr>
<td>H</td>
<td>Minimum drill diameter for buried via</td>
<td>10</td>
<td>10</td>
</tr>
<tr>
<td></td>
<td></td>
<td>NA</td>
<td>NA</td>
</tr>
<tr>
<td>I</td>
<td>Minimum Pad diameter for buried via</td>
<td>18</td>
<td>16</td>
</tr>
<tr>
<td></td>
<td></td>
<td>16</td>
<td>NA</td>
</tr>
<tr>
<td>J</td>
<td>Laser drilled Microvia dia. from layer 1 to 2 &amp; 2 -3</td>
<td>4</td>
<td>4</td>
</tr>
<tr>
<td></td>
<td></td>
<td>NA</td>
<td>NA</td>
</tr>
<tr>
<td>K</td>
<td>Aspect ratio</td>
<td>0.5: 1</td>
<td>0.75:1</td>
</tr>
<tr>
<td></td>
<td></td>
<td>NA</td>
<td>NA</td>
</tr>
</tbody>
</table>
Summary & Conclusions

- Increasing device I/O & speed are driving traditional plated through hole technology to the limits of performance both physically and electrically. What’s needed?
  - High performance well characterized dielectric materials
  - Advanced imaging techniques (Laser Direct Imaging)
  - Alternate via structures (Laser drilled, Blind & buried)
  - Filled via technologies
  - Stacked laser drilled via structures
  - High aspect ratio copper plating capability

- Chip scale components are migrating from hand-held devices to large scale electronic systems with increasing I/O’s and they are here today!!!
Design Considerations With Microvias

With aspect ratio’s limited to 0.5 to 0.6 and typical hole diameters of 4 to 6 mils, dielectric thickness are respectively 2 mils to 3 mils max.

Thin dielectric issues include:

- Dielectric layers are generally single ply constructions
- Thickness variations of 20 percent can be expected
- Impedance of 50 ohms and higher are difficult to achieve without using fine lines (i.e. < 5mils)
- Tolerance must be considered when lines are less than 5 mils
- Surface and buried via layers are plated increasing trace thickness and must be accounted for in the impedance model
- Parametric modeling is recommended for critical lines
Properties of interest:

- Capacitance of via structure with respect to:
  - Adjacent return planes
  - Anti-pad geometries
- DC resistance
- AC resistance
- DC inductance
- AC inductance
Enabling Technologies

Dynamic Details, Inc.

RLC Models: PTH Via & Pad

Source

10 mil drill
20 mil pad

Anti-pad

1.0 oz
Cu plane

62 mil via length
εᵣ = 4.0

Capacitive stub length

Sink
Dynamic Details, Inc.

Enabling Technologies

RLC Models: PTH Via & Pad

Inductance: 10 mil via 20 mil pad
Current path sweep: Start Z=2 mil, Stop Z=58 mil

Source set at 60 mils

Increasing distance from Source
RLC Models: PTH Via & Pad

Capacitance: 10 mil via 20 mil pad
Anti-Pad sweep: Start radius 13 mil, Stop radius 16 mil
RLC Models: 0.8 mm BGA Pad & µVia

\[ R_{DC} = 0.00131 \ \Omega \]
\[ R_{AC} = 0.00282 \ \Omega \ @ \ 1.0 \ GHz \]
\[ L_{DC} = 0.1295 \ \text{nH} \]
\[ L_{AC} = 0.0916 \ \text{nH} \ @ \ 1.0 \ GHz \]
Enabling Technologies

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RLC Models: 0.8 mm BGA Pad & μVia

\[
\begin{align*}
R_{DC} &= 0.00074 \, \Omega \\
R_{AC} &= 0.00186 \, \Omega \, @ \, 1.0 \, GHz \\
L_{DC} &= 0.0553 \, nH \\
L_{AC} &= 0.0337 \, nH \, @ \, 1.0 \, GHz
\end{align*}
\]
Capacitance: Microvia with respect to plane

[Graph showing capacitance vs. Dsep (mil)]
RLC Models: 0.8 mm BGA Pad & μVia

- \( R_{DC} = 0.00214 \, \Omega \)
- \( R_{AC} = 0.00692 \, \Omega \) @ 1.0 GHz
- \( L_{DC} = 0.308 \, nH \)
- \( L_{AC} = 0.238 \, nH \) @ 1.0 GHz
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RLC Models: 0.8 mm BGA Pad & µVia

Source

5 mil laser via

15 mil via pad

12 mil capture pad

Sink

Cu plane

\[
\begin{align*}
R_{DC} &= 0.00157 \ \Omega \\
R_{AC} &= 0.00494 \ \Omega \ @ \ 1.0 \ GHz \\
L_{DC} &= 0.205 \ nH \\
L_{AC} &= 0.139 \ nH \ @ \ 1.0 \ GHz
\end{align*}
\]
RLC Models: 0.8 mm BGA Pad & μVia

Capacitance: “Stair-Case” Via with respect to plane below
RLC Models: 0.8 mm BGA Pad & μVia

Source (BGA pad)

Sink

5 mil laser via

15 mil via pad

12 mil capture pad

Padrad

Dsep=5 mil

\[ R_{DC} = 0.00158 \, \Omega \]

\[ R_{AC} = 0.00476 \, \Omega \, @ \, 1.0 \, GHz \]

\[ L_{DC} = 0.205 \, nH \]

\[ L_{AC} = 0.140 \, nH \, @ \, 1.0 \, GHz \]
Capacitance: “Stair-Case” Via with respect to adjacent plane
RLC Models: SMV Pad & μVia

Source

4 mil laser via
Cu plate-fill

10 mil via pad

10 mil capture pad

Sink

Cu plane

Dsep

$R_{DC} = 0.00125 \, \Omega$

$R_{AC} = 0.00295 \, \Omega \, @ \, 1.0 \, \text{GHz}$

$L_{DC} = 0.0957 \, \text{nH}$

$L_{AC} = 0.0550 \, \text{nH} \, @ \, 1.0 \, \text{GHz}$
Capacitance: SMV Via with respect to plane below

\[ C_{SMV,SMV} \text{ [pF]} \]

\[ D_{sep} \text{ [mil]} \]
Dynamic Details, Inc.

RLC Models: SMV_2 Pad & μVia

\[ R_{DC} = 0.00148 \, \Omega \]
\[ R_{AC} = 0.00389 \, \Omega \, @ \, 1.0 \, \text{GHz} \]

\[ L_{DC} = 0.119 \, \text{nH} \]
\[ L_{AC} = 0.0695 \, \text{nH} \, @ \, 1.0 \, \text{GHz} \]
Enabling Technologies

Dynamic Details, Inc.

RLC Models: SMV Pad & µVia

Capacitance: SMV_2 Via with respect to plane below

![Graph showing capacitance change with respect to depth]
Dynamic Details, Inc.

Enabling Technologies

RLC Models: SMV_3 Pad & μVia

Source

4 mil laser via
Cu plate-fill

Sink

10 mil via pad

10 mil capture pad

Cu plane

Dsep

\[ R_{DC} = 0.00161 \, \Omega \]
\[ R_{AC} = 0.0153 \, \Omega \, @ \, 1.0 \, \text{GHz} \]
\[ L_{DC} = 0.150 \, \text{nH} \]
\[ L_{AC} = 0.0947 \, \text{nH} \, @ \, 1.0 \, \text{GHz} \]
Capacitance: SMV_3 Via with respect to plane below

![Graph showing capacitance vs. Dsep (mil)]
Enabling Technologies

Dynamic Details, Inc.

RLC Models: SMV_3 Pad & \( \mu \)Via

- **4 mil laser via**
- **Cu plate-fill**
- **10 mil via pad**
- **2 mil**
- **Anti-pad Dia.**
- **Sink**
- **Cu plane**
- **5 mil**

**Parameters**

- \( R_{DC} = 0.00161 \, \Omega \)
- \( R_{AC} = 0.0156 \, \Omega \) @ 1.0 GHz
- \( L_{DC} = 0.150 \, \text{nH} \)
- \( L_{AC} = 0.0907 \, \text{nH} \) @ 1.0 GHz
Capacitance: SMV_3 Via with respect to Adjacent plane
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Dynamic Details, Inc.

RLC Models: SMV_3 Pad & µVia

4 mil laser via
Cu plate-fill

10 mil via pad

Source

Anti-pad Dia.

Sink

2 mil

5 mil

Cu plane

R_{DC} = 0.00161 \, \Omega
R_{AC} = 0.0160 \, \Omega \text{ @ } 1.0 \text{ GHz}
L_{DC} = 0.150 \, \text{nH}
L_{AC} = 0.0882 \, \text{nH \text{ @ } 1.0 \text{ GHz}}
Capacitance: SMV_3 Via with respect to Adjacent 2 planes
Enabling Technologies

Dynamic Details, Inc.

RLC Models: SMV_3 Pad & µVia

4 mil laser via
Cu plate-fill

Source

BGA Pad radius

Anti-pad
18 mil dia.

Sink

Cu plane

2 mil

BGA pad diameter sweep: Start 10 mil stop 26 mil

5 mil
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RLC Models: SMV Pad & μVia

Resistance: SMV_3 Via BGA pad radius
sweep: 5 mil start, 13 mil finish

![Graph showing the relationship between resistance and BG pad radius](image)
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RLC Models: SMV Pad & μVia

Capacitance: SMV_3 Via with respect to Adjacent plane
BGA pad radius sweep: 5 mil start, 13 mil stop
Inductance: SMV_3 Via BGA pad radius
sweep: 5 mil start, 13 mil finish