Design and Realization of an ALICE SDD End-Ladder Prototype

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Abstract

The paper presents the last version of a rad-hard digital chip together with a full end-ladder card prototype of the data acquisition (DAQ) chain of the ALICE SDD experiment. The chip has been designed and constructed using a rad-hard digital library provided by CERN. The end-ladder card includes all the electronic devices foreseen for the DAQ chain of ALICE SDD experiment. Moreover the card interfaces with the front-end electronics and with the counting room detector data link (DDL). Particularly, the end-ladder card prototype has been designed taking into account the constraints on the dimensions of the final apparatus.

I. INTRODUCTION

The paper explains the design and the construction of a prototype of an end-ladder card for the ALICE SDD experiment. The design is a part of the ALICE ITS [1], [2] experiment, at CERN. In the ALICE ITS, that is a portion of the whole ALICE detector, the end-ladder performs data reduction, compression and packing for a data acquisition chain. Particularly the end-ladder card includes a chip that mainly carries out the above mentioned tasks. Besides the chip's functions the end-ladder card interfaces with the Front End Electronics (FEE) and elaborates and transmits the dataset received from the front-end electronics through an optical channel and to the counting room.
The paper also describes the chip that compresses and packs the dataset. In addition the paper shows in detail the design of the end-ladder prototype card and the relative tests that are going to be carried out in the next future.

II. THE END-LADDER CARD PROTOTYPE

The prototype card includes an actual ALICE SDD prototype unit with all the components foreseen for the final implementation on the experiment, shown on lower box of fig. 1, plus an external larger unit with all the testing equipment required for measurements in lab, shown on top box of fig. 1. The two units are part of the same end-ladder prototype card. So, even though the figure shows two main colored boxes they both refer to the same end-ladder prototype unit. The actual end-ladder board matches the final dimension while the external part of the card provides all the connectors and a receiver mirror unit for an easy-to-use complete system. All the final optical modules are provided and are composed of 3 items: 2-photodiodes and 1-laser single-mode working at a wavelength of 1310nm. The optical components are provided with their own fibers. The whole picture of the card is shown in fig. 2.
Once the front end data set enters the system, a small size digital rad-hard chip performs a bi-dimensional compression [3], [4]. In addition the chips acts as a JTAG switch for the FEE. The incoming dataset is so compressed, packed and serialized via a Gigabit Optical Link serializer (GOL) chip that interfaces, by means of a 800Mb/s optical link [5], with the counting room. The serialized dataset is received into a mirror receiver unit that de-serializes the stream and re-constructs the incoming dataset after the bi-dimensional compression. This mirror unit is included into the external larger board of the end-ladder card prototype as shown in fig. 1 and 2.
The card is able to drive all the final components that will be mounted into the ALICE SDD DAQ chain. In addition most of the ASICs mounted on the board are already in the final version with the final foreseen package. Also the optical modules match the foreseen transmission mode (single) and wavelength (1310nm).
The card allows diffrent working modes since it has been designed with several configuration and testability pins. For example on the card can be run separately 3 different and asynchronous 40MHz clock signals. The first is used for clocking the deserializer chip on the deserializer unit, the second for providing the reference clock, through the optical link, to the GOL serializer, and the third is used by a FPGA-based receiver also implemented on the deserializer unit. Two out of three at a time of these clocks may be grouped to test the relationship among each other in term of signal phase. In fact, an improper signal phasing may cause errors during data transmission. In addition the input dataset may be provided both with LVDS or CMOS signals. So the signals may be originated directly through the actual detector or by means of LVDS to CMOS converters. Also the clock jitter may be tested to realized up to what extent the system is jitter immune. This can be measured selecting the clock jitter with a pattern generator. All these types of tests must be done in the next months and will require a long and accurate processing and analysis phase.

III. CARLOS CHIP

The compressor chip, hereafter named CARLOS, is a VLSI Application Specific Integrated Circuit (ASIC) device that has been designed and developed, within the ALICE collaboration, both in the Physics Department of Bologna University and at CERN. CARLOS is composed of nearly 19k gates, 86 user pads out of the 100 total pads, it is clocked

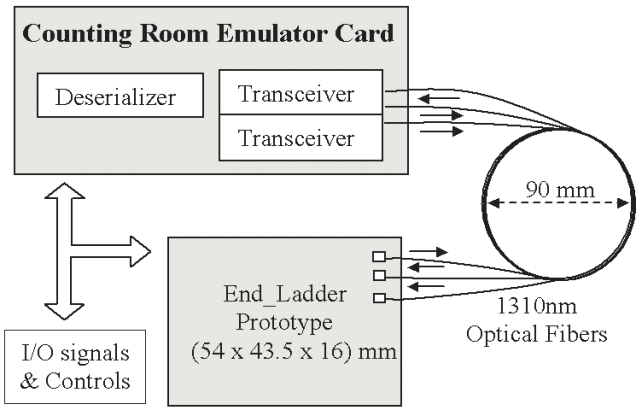

Figure 1 - Sketch of the End-Ladder Card Prototype

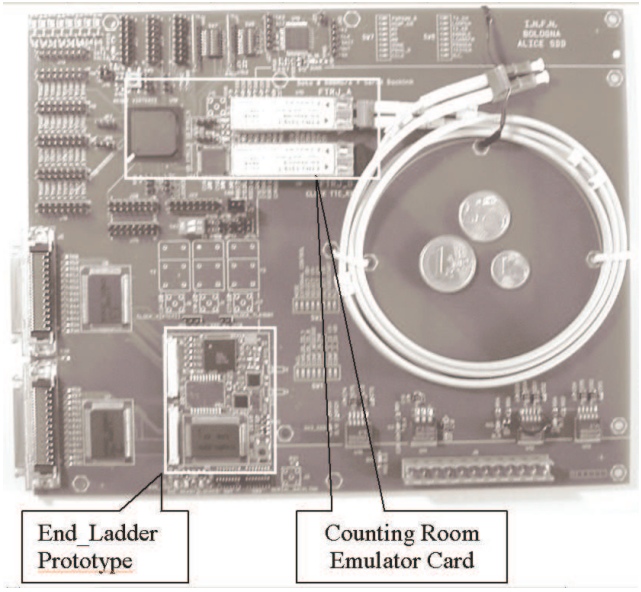

Figure 2 - Picture of End-Ladder Card Prototype

at 40 MHz, it has been designed mostly by means of the VHDL language and implemented in a 0.25µm CMOS 3-metal rad-hard digital library [6], [7], [8]. Apart from the VHDL the chip implements RAMs cells, also designed to be rad-hard, that have been developed full-custom and treated as black-boxes in the context of the chip. The library itself has been developed at CERN to be applied into LHC electronics even though is basically derived from a standard 0.25µm CMOS commercial technology. The whole die area of the chip is 4x4 mm^2. The library and the design techniques guarantee the radiation hardness of the chip under the radiation dose of the experiments that is expected to be some tens of krad. The chip has been already used successfully during a test beams at CERN in August 2003 and 2004. The implementation of the on-line data bi-dimensional compressor has been carried out, apart from digital control logic, by means of previously mentioned full-custom dual-port static RAMs divided into two 256x9-bit words per data channel. Altogether there are 4 RAM macro cells [9]. Also these macro cells have been implemented by means of the rad-hard library. Within the whole DAQ chain the chip works after the data coming from the silicon drift detector have been sampled and digitalized by other dedicated chips. Then the compressed and packed dataset goes to a receiver card that acts as a concentrator for several CARLOS chips. All in all the dataset is serialized into the 800Mb/s optical link and received into a mirror receiver card that de-serializes the stream and re-constructs the incoming dataset as it was generated by CARLOS chip.

So far a prototype of an and-ladder card has been designed and constructed: now is almost finished and the first tests on the full readout chain will start in the next future. Nevertheless, the preliminary tests carried out on a chain composed of different cards connected each other have shown that the full chain works well and for this reason has been designed a full end-ladder prototype card.

IV. Readout Architecture

The requirements for the SDD readout system derive from both the features of the detector and the ALICE experiment in general. A pattern generator provides the input dataset vectors that simulate the real SDD detector [10]. The amount of data generated by the SDD originates from 2 half detectors for each CARLOS chip. Each half detector is composed of 256 anodes and, for each anode, 256 time samples are sampled in order to cover the full drift (time) length. Altogether each detector is able to generate an dataset made of up to 256x256 data words. The dataset from the two half detectors are read by one of the two channels of CARLOS chip. The readout electronics is composed of front-end boards (not shown in the figures) that collect data from the silicon detectors and end-ladder boards that contain CARLOS chips, GOL serializers and optical links. All the boards are inserted in a radiation environment. The whole acquisition system electronics performs analog data acquisition, A/D conversion, buffering, data compression and interfacing to the ALICE data acquisition system. Particularly the data compression and interfacing task is carried out by CARLOS chip. Each chip reads two 8-bit input data, is synchronized with an external trigger device and writes a 16-bit output word at 40MHz. Then the data are serialized and transmitted by means of an optical link at 800Mbit/s.

CARLOS itself contains a JTAG unit: this is a block driven via a JTAG port, which allows CALOS chip to run in two different ways: RUN mode or JATG mode. The mode selection and some dedicated commands such as reset are read by means of a serial back-link channel. For example once in JTAG mode the chip allows all internal registers to be initialized, read, written and so on. For what concerns JTAG, CARLOS also acts as a JTAG switch providing three JTAG ports in output: two for the hybrids of the half detectors and one for the serializer GOL chip. In other words CARLOS receives one input JTAG port and provides in output 3 JTAG ports, thus allowing opening JTAG connection towards different devices.

Figure 3 shows a picture of the final layout of CARLOS. It is a 16 mm^2 squared chip, RAMs included, with 100 pads and now is packaged on a CQFP100 ceramic package for testing purposes only.

V. CARLOS TESTS

CARLOS tests were primarily designed using a Printed Circuit Board (PCB) for test purposes only. A four-layer PCB was built to provide I/O signals with strip-line connectors by inserting the packaged chips on ZIF sockets. These chips were randomly selected from the central lines of the silicon wafer during fabrication and were stressed up to 60 MHz; at higher clock frequencies they begin to fail. Although the CARLOS layout was realized with separated core and periphery power supply pads, the tests were executed at 2.5V for both powers. At the required 40MHz clock frequency, the chips consume power at a level of 200mW.

At first CARLOS was stimulated using the identical test vectors applied during post-layout simulation. The pattern generator provided a 100 k-word test bench including the JTAG configuration and two 50-kword events. Then the dataset red by the logic analyzer were processed using a dedicated SW tool to reconstruct back the original input dataset. In other words this tool performs the CARLOS reverse function. As a second step the tool compares actual input values with reconstructed ones and lists errors in case of mismatch. This software tool automated the CARLOS tests and allowed to draw conclusions on the whole DAQ chain functionality.

Below is reported a quick summary of the tests on 20 packaged chips:

1. 19 chips work properly,
2. 1 chip has only one good channel.

The second test on the 20 chips was the built-in self-test run and controlled using the JTAG port. This was designed to show the results of the test on the output JTAG output pin with a given code. 19 chips out of 20 passed the built-in self-test, while 1 experienced failure code. Even if 20 chips did not do not allow to draw conclusions, it can be said that the built-in self-test is as a very simple and reliable test for chip selection. Other test benches were employed to stimulate CARLOS such as 48k-word events with random generated values, gaussian generated values and data originating from a test beam.

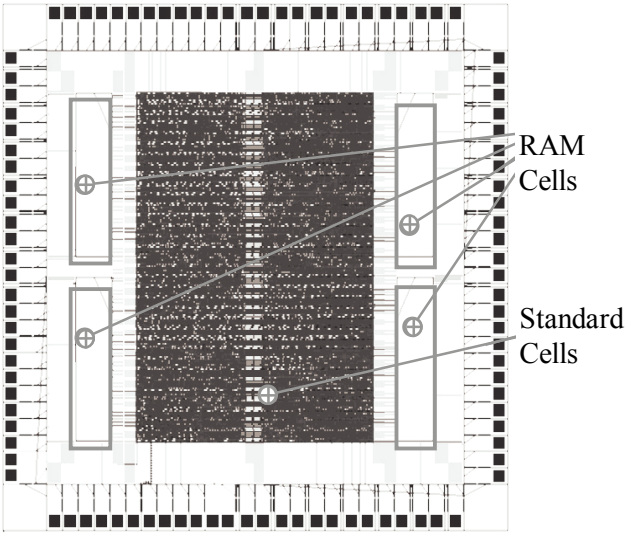

Figure 3 - CARLOS layout

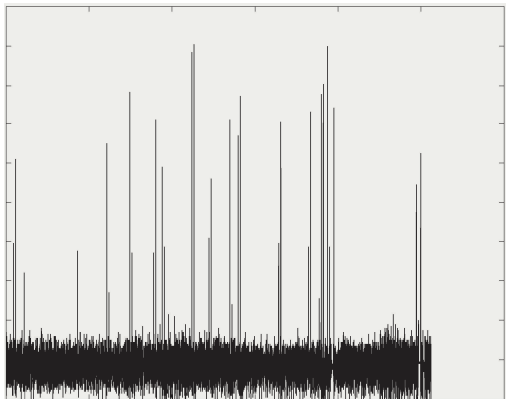

Figure 4a - Original 256 x 200 event before 2D compression

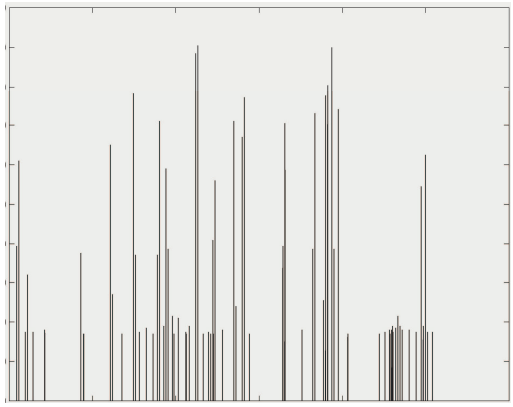

Figure 4b - Reconstructed 256 x 200 event after 2D compression

As for data deriving from the test beam, the chip was tested as outlined above using the internal bi-dimensional compressor. Figs. 4a and 4b show two plots, an incoming dataset event and a reconstructed one respectively. The pictures show about 50k data samples deriving from 256 anodes, each containing 200 timing samples. All data were plotted on the same X axis from the first anode to the 256th. Figs. 4a and 4b represent the same event before and after the bi-dimensional compression. Each peak can be interpreted as the higher datum of a cluster. If adjacent anodes have corresponding peaks that satisfy the bi-dimensional algorithm, the cluster is confirmed; otherwise the peak is considered as a mere noise spike. Nevertheless the figures show that all peaks are properly reconstructed both in position and in height while the background noise is present in the original event but is

significantly absent in the reconstructed one. This test was performed on several sets of data to ensure the bi-dimensional compressor does not reject any real clusters. The data were extracted in a physics experiment: this involved a 256 x 200 x 8-bit event corresponding to a silicon drift detector consisting of 256 anodes. The latter were time-scanned for 200 timing slots. The compressor's lower and higher thresholds were set to two given values. If they had been set to higher levels, Fig. 4b would have shown fewer clusters since the higher the thresholds (even if just one), the smaller the number of clusters detected.

VI. Conclusion

The chip CARLOS has been implemented using CERN library 0.25µm CMOS technology that employs radiation tolerant layout design. CARLOS is a prototype tailored to fit in the ALICE SDD readout architecture. The final version of the chip has been sent to the foundry in May 2004 and is going to be tested in the next future. All the implementations and tests on the ALICE SDD DAQ chain have been carried out so far on prototype versions of the chip that did not differ significantly from the last final one.

The CARLOS chip is inserted on an end-ladder prototype card of the ALICE SDD experiment. Now the prototype board is almost complete and ready for full tests. This will allow the data acquisition on a complete experimental chain of ALICE SDD. So far, the preliminary tests carried out on a chain composed of different cards connected each other have shown that the full chain works well and for this reason has been designed a full end-ladder prototype card.

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