Design and Realization of an ALICE SDD End-Ladder Prototype

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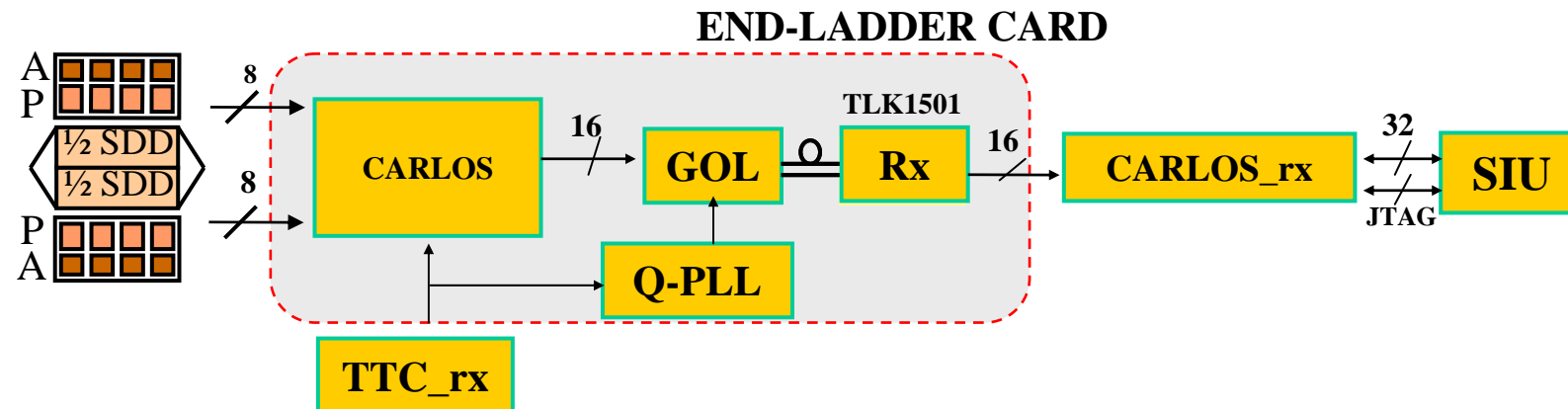
Physics Department University of Bologna

I.N.F.N. Sezione di Bologna

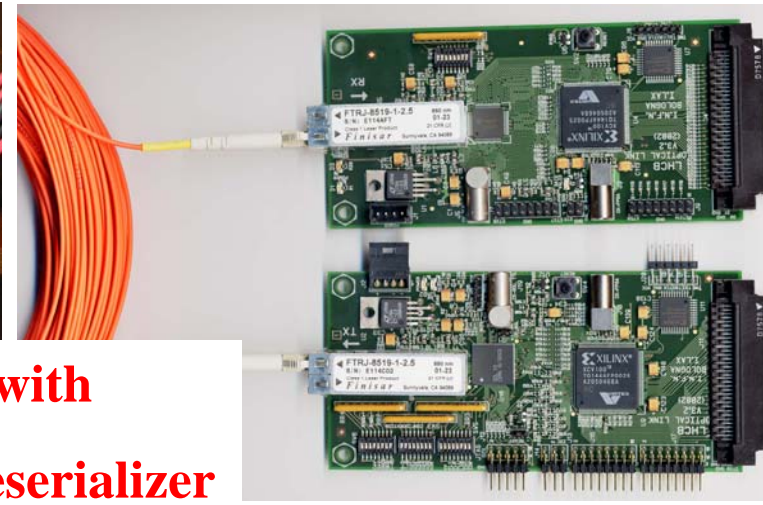# The Full ALICE SDD Readout Chain

END-LADDER CARD

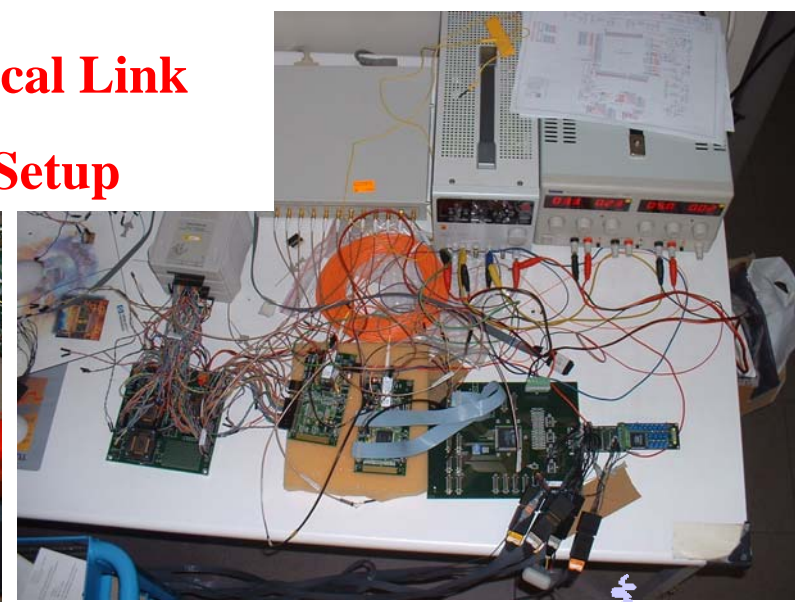**Test of the chain performed first in Bologna and then at CERN (2-3)**
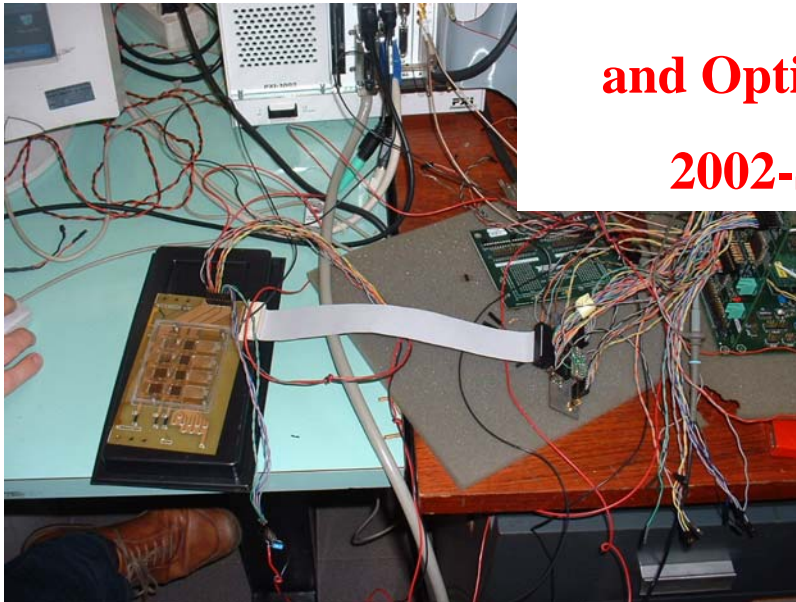

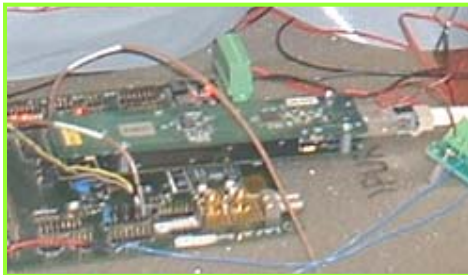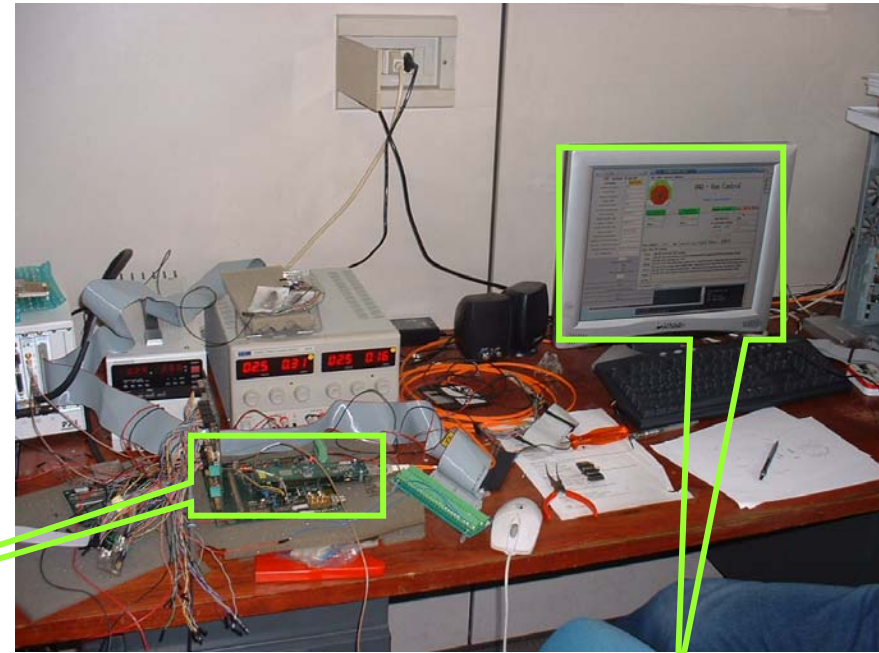**CHAIN #3 was used at Test Beams on August 2003-2004 at CERN**
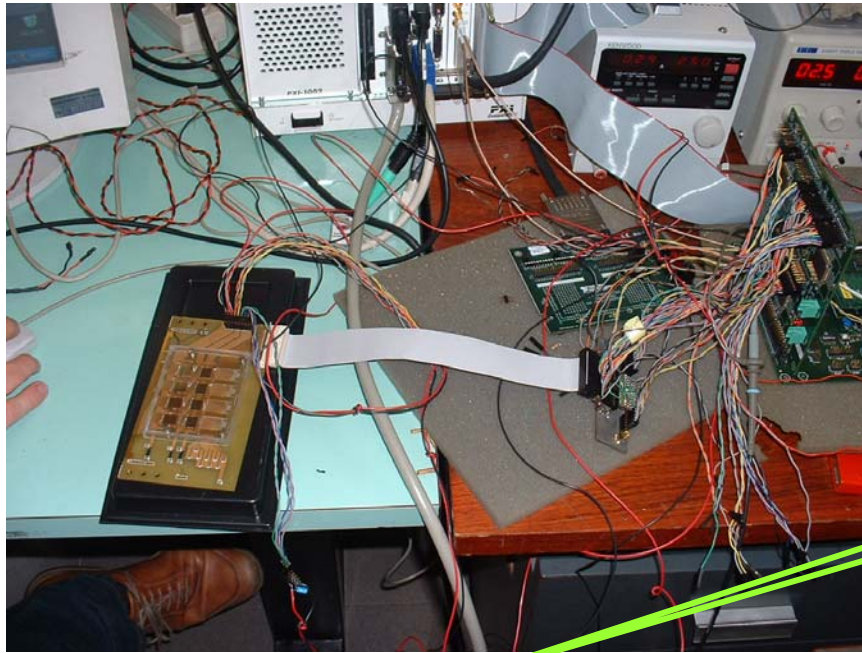
The SDD Readout Chain in Bologna Lab

This is with

Serializer-Deserializer

and Optical Link

2002-Setup

Implementation of the DDL card in Bologna (2004)

This is without Serializer-Deserializer and Optical Link between FEE and Carlos_rx receiver card

Chain used for Test Beam 2004 at CERN

DDL monitor when the chain is under test in Bologna Lab

Number of triggers sent

Number of events recorded

PCI-6533
DIO-32HS

Applying compression to the input pattern

saw-tooth
shaped artificial
dataset
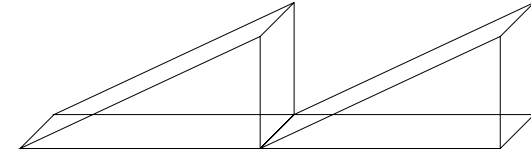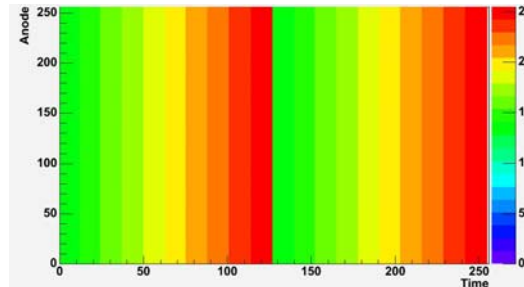
DAQ readout chain with a given setup for 2D compression

2D compression disabled
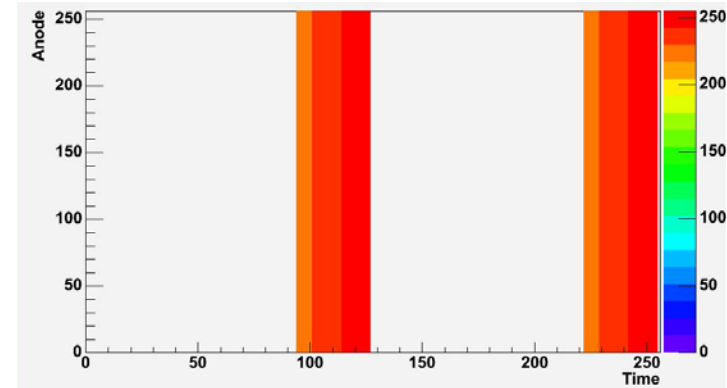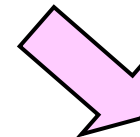
2D compression enabled

Home-made Verification SW

100k-event runs

decoding SW (*carlosrx*)

verification OK

verification failed
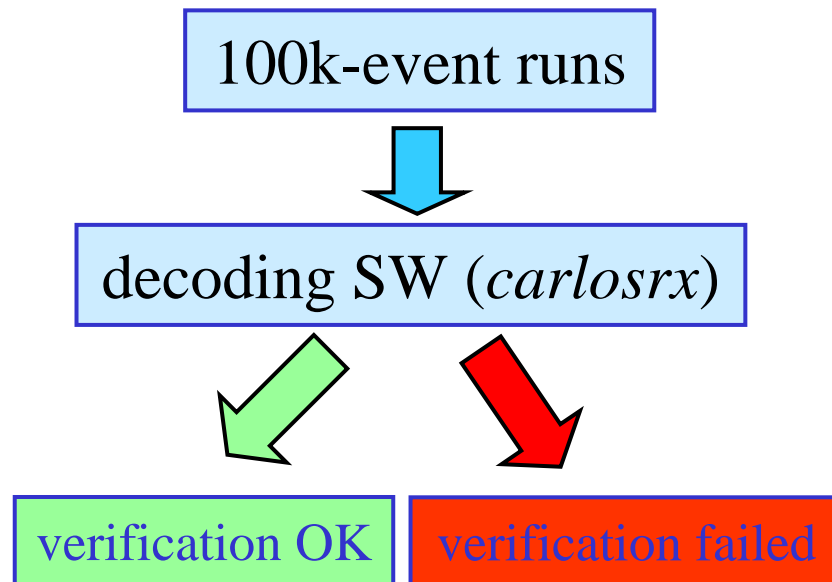
Test features:

- CARLOS programming via JTAG
- One Looped Event: 2.5k, 16k e 64k
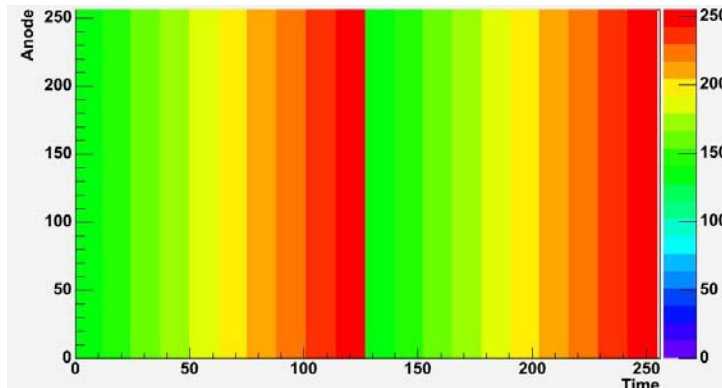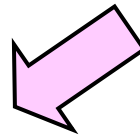- Back-pressure of CARLOSrx over CARLOS
- Trigger frequency (up to 550 Hz)
  Upper limit (FEE) is 625 Hz

SDD

Options

Insert RAW number(press return to confirm)   0

Insert file number (return)   0

Inserisci l'anode length (invio)   0

Insert TH 0 (return)   0

Insert TH 1 (return)   0

Insert TL 0 (return)   0

Insert TL 1 (return)   0

Compression enable?
  ○ Yes
  ○ No
Insert limit number (return)
    0

Print

Start

Controlla gli eventi uguali

TOT

GRAPH

MEDIA

Exit

Tests with the FEE board

Noise + test pulse
provided by FEE without
2D compression

Implementation at Test-Beam on August 2004

Carlos_rx card

Carlos card with prototype chip

SDD plus FEE with final chips

This is without Serializer-Deserializer and Optical Link

Prototype Card: End Ladder with CARLOS (ALICE SDD)
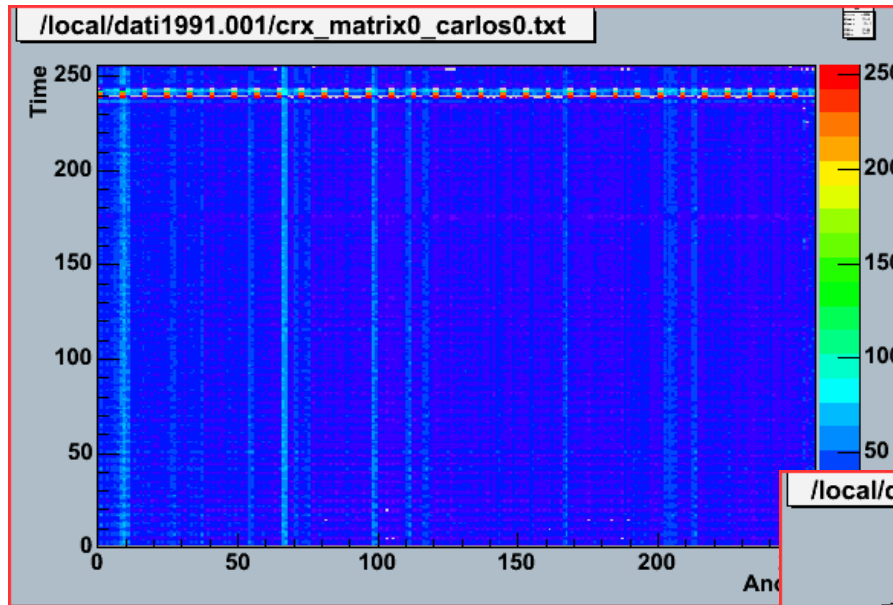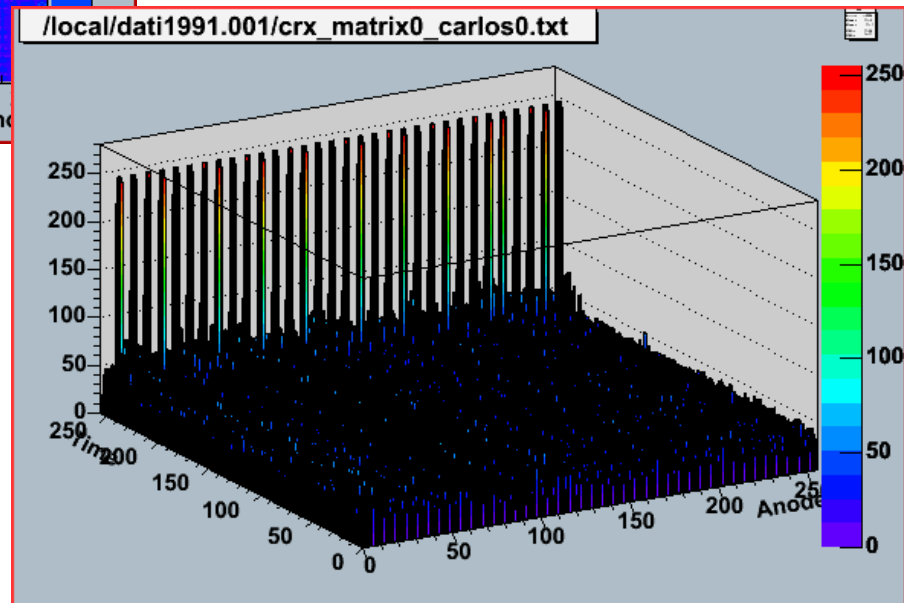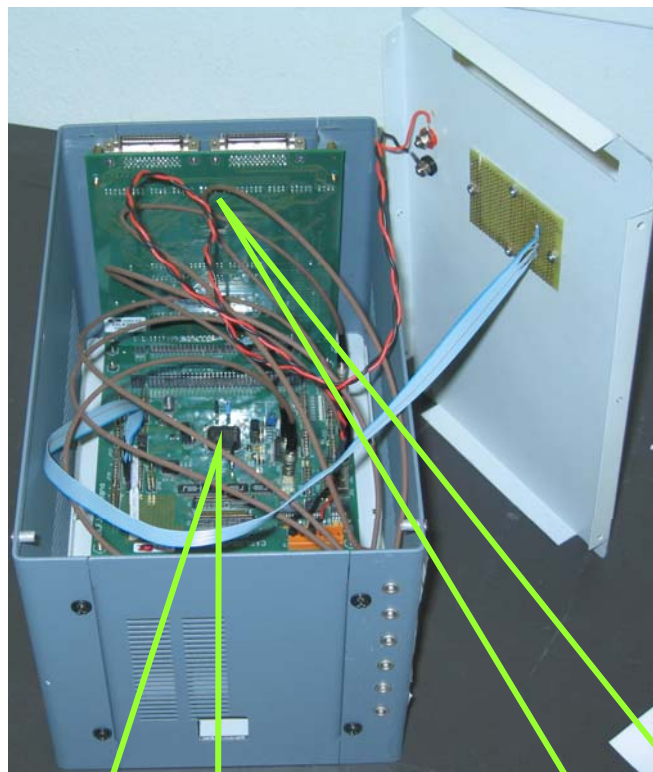
End-Ladder Prototype Sketch

Third LEMO: board clock. It can be connected to another LEMO or to the crystal oscillator

- 5V (input 3.3V),
- 3.3V (input LHC4913),
- 2.5V (output LHC4913),
- GND,
- LV_DIG,
- LV_ANLG
- GND_DIG,
- GND_ANLG

VirtexII250 I/Os

+3.3V for Transceiver Finisar and RX board

Oscillator

VirtexII 250

TLK 1501

Finisar FTRJ1319-1

Finisar FTRJ1319-1

XC 18V04

Oscillator

90-100 mm

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Prototype Card: End Ladder with CARLOS (ALICE SDD)

CMOS-LVDS

Molex

43.5 mm

54 mm

Inner Board Prototype End_Ladder (54 x 43.5 x 16) mm

CMOS-LVDS

CMOS-LVDS

Molex

CMOS-LVDS

plexiglass for fibers

End-Ladder Prototype Picture

Counting Room
Emulator Card

End_Ladder
Prototype

43.5mm

54 mm
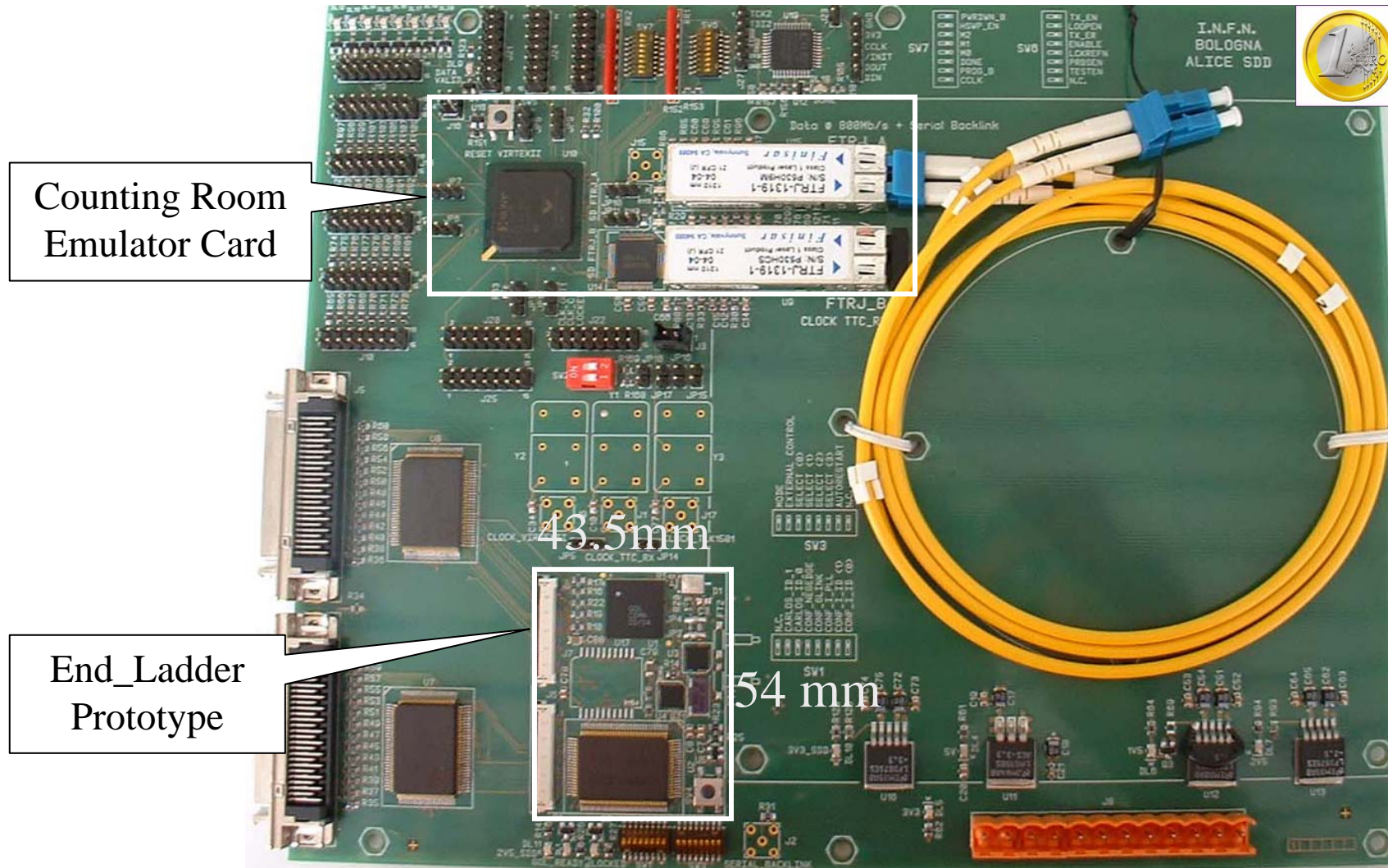
Work Plan

5/04:   New and last CARLOS prototype submitted on MPW13

                 as half-production

9-10/04:   Test of last CARLOS prototype on 20 packaged samples

10/04:   Second part of the production on MPW14

10-12/04:   Test of the complete DAQ chain from FEE to DDL

                 (prototype of the end-ladder board)

12/04-01/05:   Packaging of the CARLOS production on BGA

1st_Q/05:   Test of the production (600 BGA packaged chips)

                 Possible design of a more accurate and-ladder card

End-Talk