

Calorimeter Trigger Synchronization in CMS, Implementation and Test System

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Abstract

The final implementation of the Synchronization and Link Board (SLB) used in the Calorimeter Trigger system of CMS is presented in this paper. The board allows the synchronization of electromagnetic and hadronic trigger primitives at the LHC frequency (40.08 MHz) and its transmission to the Regional Calorimeter Trigger using Vitesse electrical links at a rate of 1.2Gb/s. The system developed for the SLB production tests and commissioning of the full production (1300 boards) is also presented.

I. INTRODUCTION

The trigger system of the Compact Muon Solenoid (CMS) experiment at the Large Hadron Collider (LHC) is a synchronous and pipelined system working at 40.08 MHz. The system can be viewed as a massive parallel processor that computes local trigger objects, followed by a tree like structure that selects the highest rank objects in the detector or performs global energy sums [1]. At each processing stage data must be synchronized.

Calorimeter trigger data are primarily generated at the Trigger Primitive Generators and must be processed by the Regional Calorimeter Trigger (RCT) processors housed in the RCT crates. Non-negligible differences on the trigger primitives arrival time to the processors are introduced by different particle flight paths, different optical transmission fiber lengths and different phase lock delays in the electronic serializers. A synchronization stage therefore must exist. The synchronization is performed in the Synchronization and Link Boards described in this paper.

Channel synchronization [2] relies on the Timing Trigger and Control (TTC) Bunch Crossing zero (BC0) broadcast command that can be adjusted relative to the LHC orbit signal, on a synchronization FIFO and on the accumulator histogram that reflects the LHC bunch crossing structure. A common hardwired control signal distribution guarantees aligned trigger data transmission through all high speed (1.2 Gb/s) transmission links.

The SLB is a PMC-like daughter board and is used in the Electromagnetic Calorimeter (ECAL) and in the Hadronic Calorimeter (HCAL) trigger boards of the CMS experiment. In total, 1300 of these boards need to be tested and commissioned. The SLB is described in Section II, the synchronization core circuit in Section III and the trigger data alignment in Section IV. The developed test system and the integration test results are presented in Section V.

II. SYNCHRONIZATION AND LINK BOARD

The SLB (Figure 1) is a custom mezzanine board, with slim dimensions (12,25 cm × 3.8cm) allowing the accommodation of up to 9 SLBs per 9U-VME mother board. The trigger data synchronization is performed in two synchronization circuits (Sync-S). The Sync-S (Figure 2) is implemented in an ALTERA Cyclone EP1C6 FPGA and is composed by four identical Sync Core blocks, each one responsible for the synchronization of one trigger tower. Almost all (~90%) of the components used in the SLB have JTAG Boundary Scan pins for test and reprogrammability purposes and are connected on a unique JTAG chain.



Figure 1: The SLB rear and front view.

A. Input Interfaces

The SLB has three 64 pin PMC like connectors. Two connectors receive trigger data from up to 8 trigger towers at 40.08 MHz. The trigger primitives are encoded in 9-bit, with 8-bit coding the trigger tower transverse energy and one extra bit used in electron identification in the ECAL or in muon identification in the HCAL.

The third connector is dedicated to the control interface, receiving the TTC broadcast commands, a low jitter clock (100 ps peak-to-peak, Rx_Clk) and the synchronization signal (Rx_BC0). This interface also provides the board register access for configuration, control and monitoring. The second clock needed by the SLB, the Tx_Clk, is synchronized with the input trigger tower data.

The Rx_Clk and the Rx_BC0 are generated and time adjusted on a common fan-out board and distributed (LVDS) in a tree like structure to the different trigger boards.

B. Output Interfaces

After synchronization, data from two trigger towers are merged along with five Hamming code bits and one synchronization bit. The resulting 24-bit data frames are multiplexed into three 8-bit words at 120.24 MHz (as required by the 4-channel Vitesse VSC7216 link) and transmitted to the RCT.

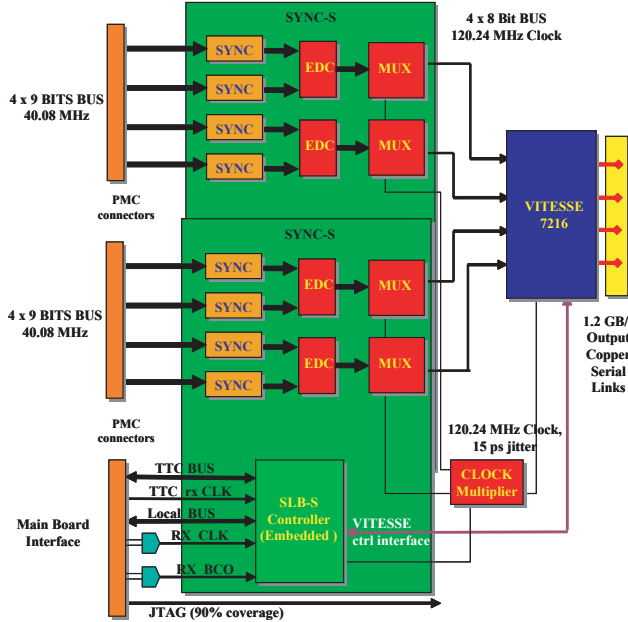


Figure 2: The SLB block diagram.

III. THE SYNCHRONIZATION CORE

The Sync Core (Figure 3) provides the synchronization functionalities for one trigger tower. Synchronization channels can be enabled or disabled by configuration to match different detector partitions.

The Sync Core is divided in two main blocks, the SyncTx and the SyncRx. At each LHC main gap the synchronization FIFO (128 × 9 bits) in the receiver side is cleared and the first word written in the FIFO should correspond to the trigger data of the first bunch.

The multiplexer in the transmitter side allows switching between real and synchronization data. Synchronization data are generated by the Sync Data Generator and implemented as a clock counter. During the gap the multiplexer inputs synchronization data and a decoder identifies the pre-programmable Clear FIFO command, which must arise after all data from the previous orbit were readout.

Upon reception of the BCO broadcast command the Tx_BCO signal is generated after a given channel delay. This signal disables the command decoder, switches the multiplexer to input real data and enables write access in the FIFO. Correspondingly the read accesses of the FIFOs are enabled by the common synchronization signal Rx_BCO. The

write access is driven by the Tx_Clk while the read access is driven by the Rx_Clk.

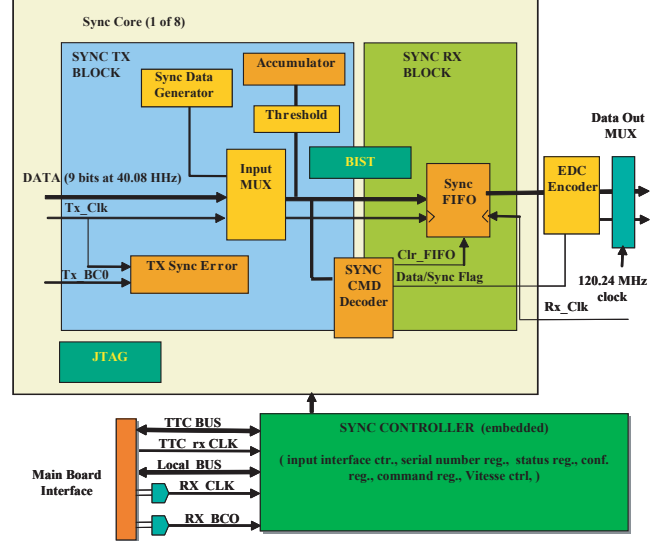


Figure 3: The Sync Core block diagram.

Write and read accesses are disabled 3445 clocks (programmable value) after the Tx_BCO and Rx_BCO signals have been raised. This 86.1 μ s period corresponds to the number of clocks from the first bunch until the start of the main gap. When the write access is disabled the command decoder is enabled and the SyncTx starts once more inputting synchronization data. On the other hand when the read access is disabled the circuit outputs zeros in the bus to ensure the link activity.

The SyncTx block has a RAM (1024 × 11 bits) used to implement the synchronization accumulator. The Tx_BCO resets the accumulator address, which is updated at each Rx_Clk cycle. The accumulator content is incremented if the received trigger tower transverse energy is higher than a pre-programmable threshold.

IV. TRIGGER DATA ALIGNEMENT

The accumulator histograms reflect the bunch occupancy and allow the monitoring of the trigger data alignment. The alignment is achieved in a two-steps operation:

1. Coarse adjustments on the timing of the BCO through the TTC system in order to identify the LHC main gap.
2. Fine adjustment on the channels delays to perform the inter-channel alignment, guaranteeing that the first data written in the FIFOs correspond to the start of the orbit.

The time adjustments must assure that the Rx_BC0 signal is received after all Tx_BC0 have been generated. At the same time the latency between the Rx_BC0 and the Tx_BC0 should be minimized to prevent that the FIFO reach the full state. The circuit has a latency register to monitor this timing. Error counters are implemented to ensure that the Rx_BC0 and the Tx_BC0 occur at every 3564 consecutive bunches, i.e the size of a complete LHC orbit.

V. TEST SYSTEM

A. Test Bench

The test bench (Figure 4) for the SLB test and commissioning of full production comprises one 6U-VME crate, a PCI-VME interface, one SLB Tester card (SLB-T) and five Serial Tester Cards (STCs).

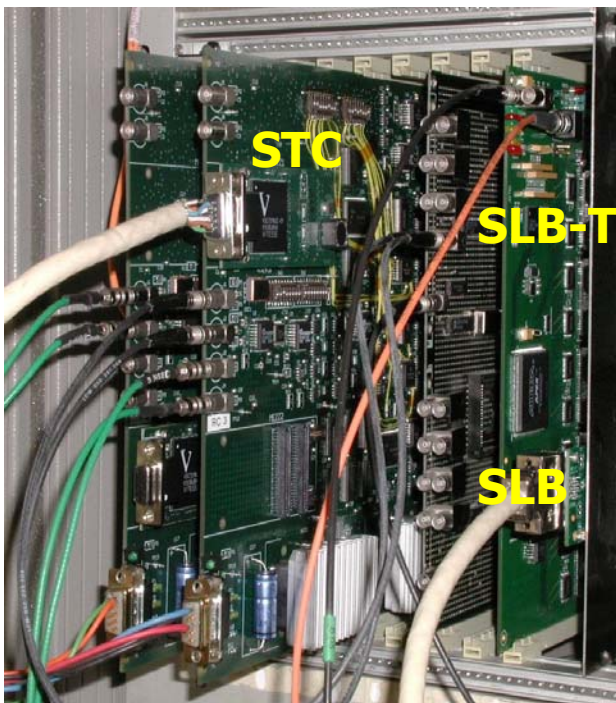


Figure 4: The SLB Test Bench.

The SLB-T can house up to five SLB daughter boards and it provides the high quality clock, Rx_Clk, required by the Vitesse links, the Rx_BC0 signal and the broadcast control commands as by the TTC system. The SLB-T has an internal Trigger Pattern Generator, which emulates the calorimeter trigger primitives at the LHC frequency and with the LHC bunch structure.

The STC was developed by the Wisconsin University. This card is configured as a receiver and it compares on fly the serial stream data transmitted by the SLB with the

expected received data. An electrical cable of 20 m connects the SLB with the STC. Preliminary test indicates a Bit Error Rate (BER) lower than $8.0 \cdot 10^{-16}/s$, corresponding to an operation of more than 72 hours without errors.

B. Software

Software for control and monitoring the hardware modules was developed in C++ within XDAQ (CMS Distributed DAQ framework) [4] and ROOT (object oriented data analysis framework) [5]. An external package [6] was used for module configuration. The ROOT Graphical User Interface (GUI) clients are shown in Figure 5.

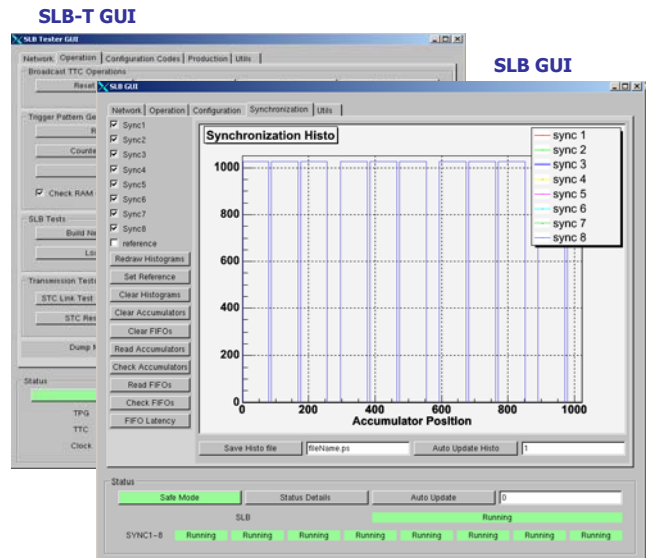


Figure 5: The SLB-T and the SLB GUIs. In the SLB GUI is shown the Synchronization Tab where the accumulator histograms for each channel are presented. In this particular case all channels are aligned.

The developed test applications for the SLB production includes the board configuration test, the state machine transition test both by VME and by TTC commands emulation, the synchronization FIFOs readout test, the accumulator contents analysis with different channel delays and thresholds and finally the data transmission test with BER measurements. The test results are encoded in a XML format file and are organized as a function of the board serial number and test id.

References to log files are kept to track the test procedure and to identify the cause of possible errors. A java script application allows the user to access the test results and associated statistics through the use of a common browser (Figure 6).

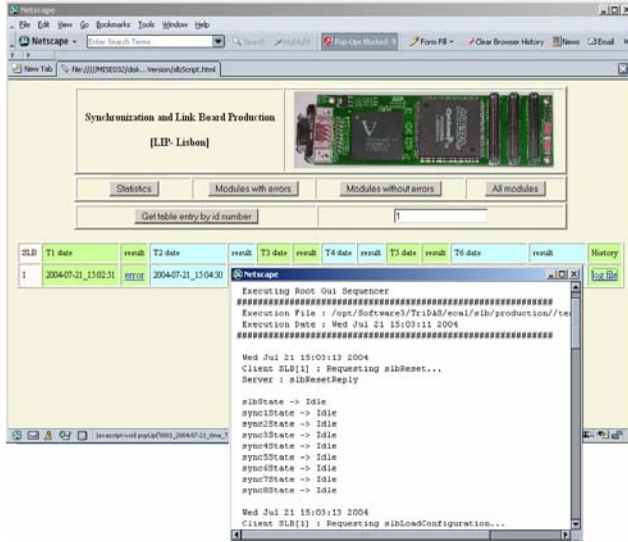


Figure 6: Netscape browser, displaying test results for SLB with serial number 1. The text window shows the log file contents.

VI. CONCLUSIONS

A synchronization scheme used to synchronize calorimeter trigger data in CMS was implemented in the SLB mezzanine card. A test system based on the SLB-T and on the STC was developed. Software for the test setup, including GUIs and a set of application tests foreseen for the production series are available. The pre-production module was proven to fulfil the CMS needs by performing channel synchronization in LHC like conditions and by working with a BER lower than $8.0 \cdot 10^{-16}/s$.

VII. REFERENCES

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