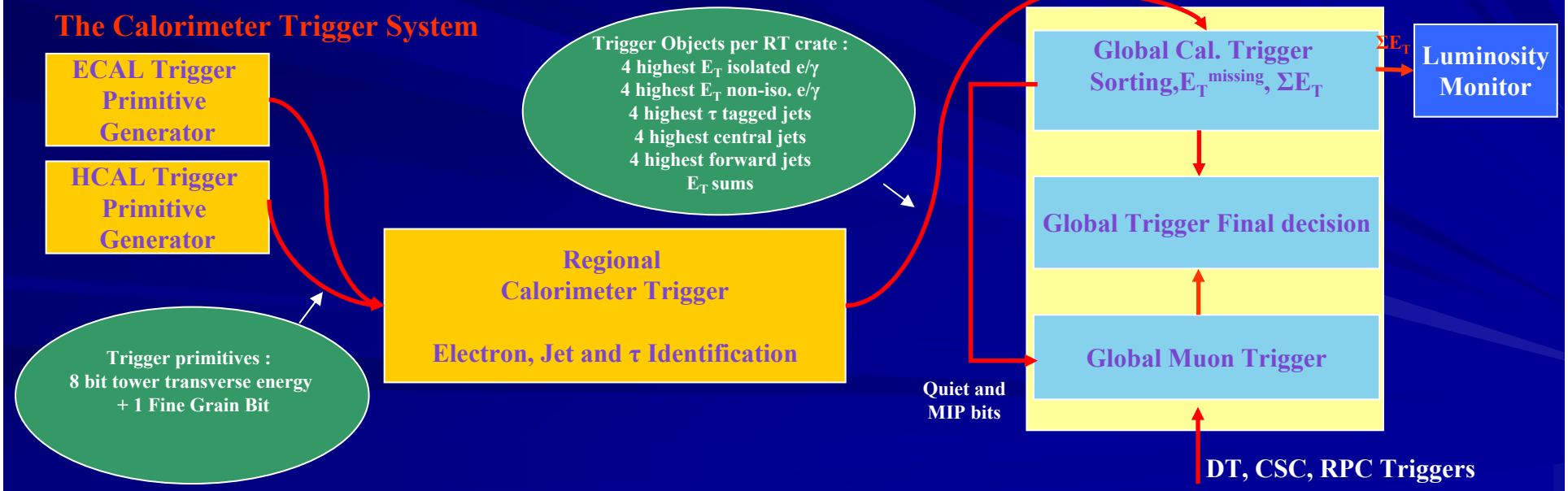
Calorimeter Trigger Synchronization in CMS, Implementation and Test System

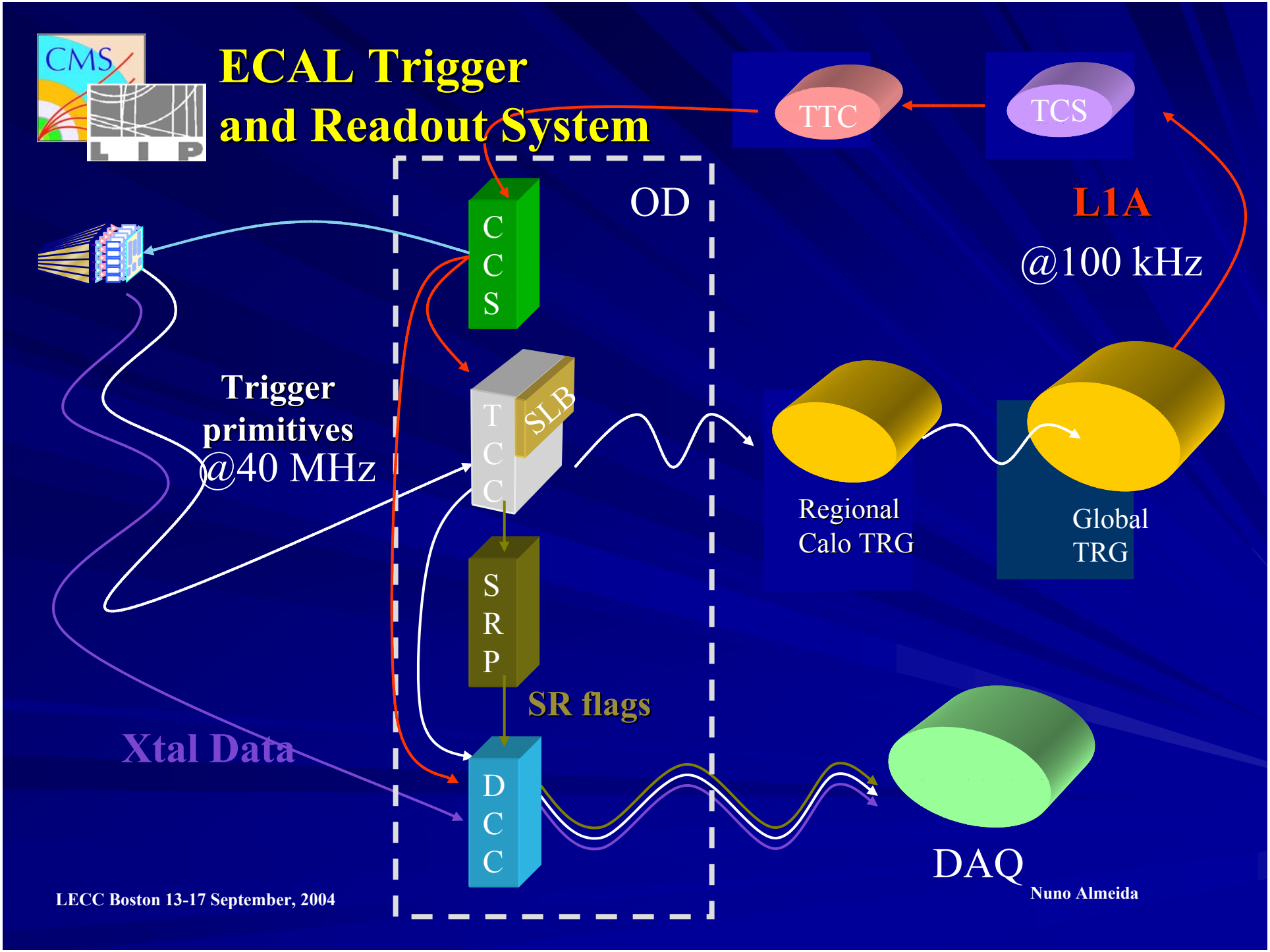
N.Almeida, J.C.DaSilva, R.Alemany and J.Varela

The CMS Trigger System Overview

- Synchronous and pipelined system working at 40.08 MHz.
- Computes local trigger objects , selects the highest rank objects in the detectors, performs global energy sums and combines trigger data in order to accept or reject the event.
- At each processing stage data must be synchronized.

The Calorimeter Trigger System




ECAL Trigger
and Readout System
TTC
TCS
OD
L1A
@100 kHz
CCS
Trigger
primitives
@40 MHz
TCC
SLB
Regional
Calo TRG
Global
TRG
SRP
SR flags
Xtal Data
DCC
DAQ
LECC Boston 13-17 September, 2004
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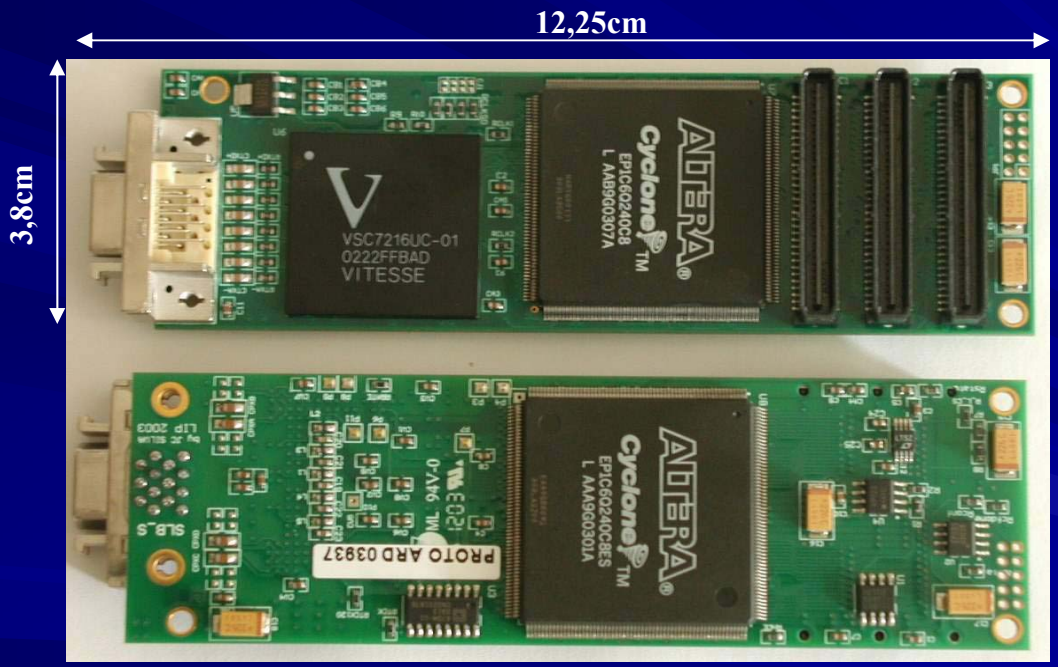
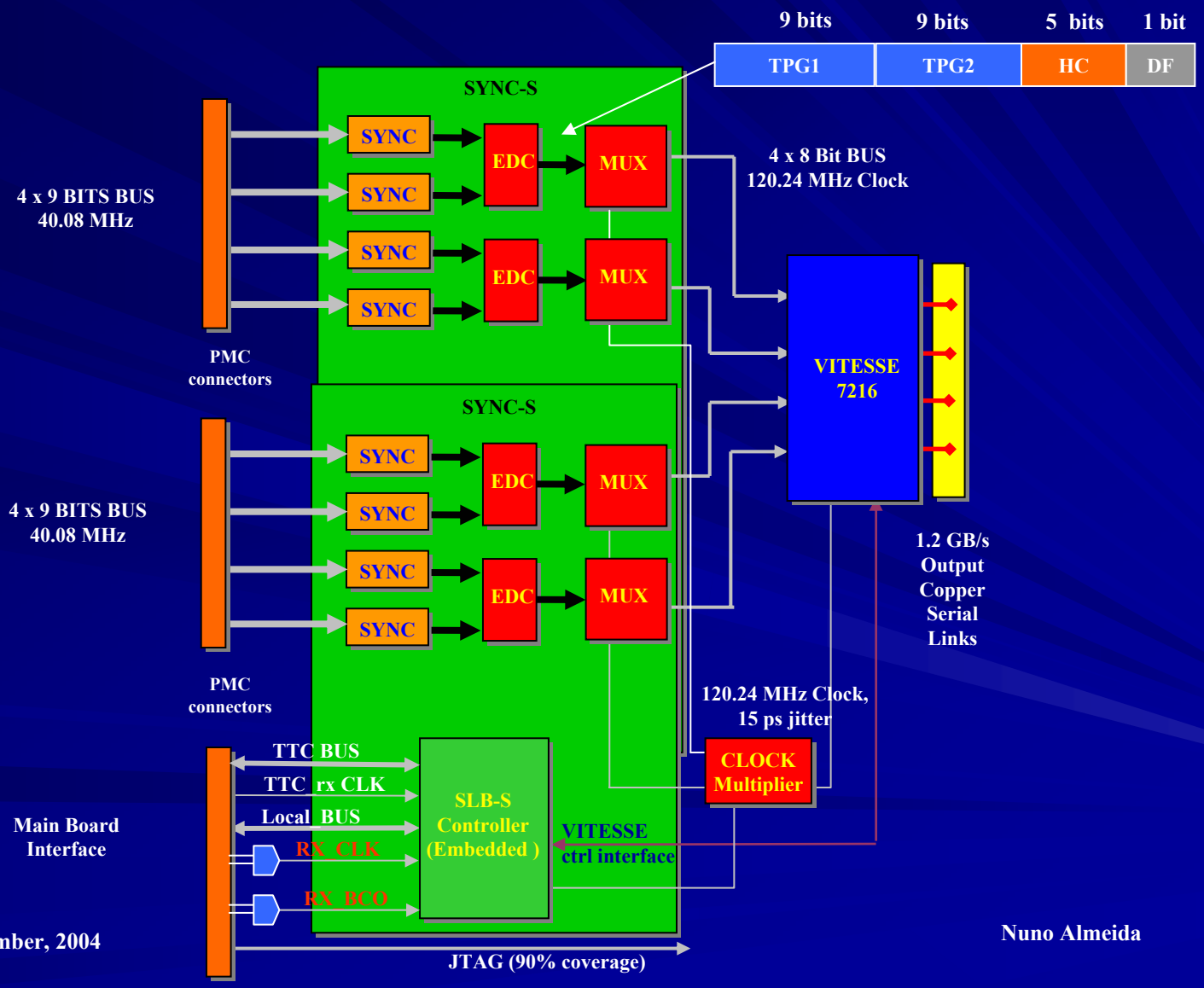
Synchronization and Link Board (SLB)

Calorimeter trigger data are synchronized by the SLB housed in the TCC(ECAL) and HTR (HCAL) Trigger boards before transmission to the Regional Trigger Processors.



Slim dimensions allows up to 9 SLBs per 9U Trigger Board

SLB Block Diagram



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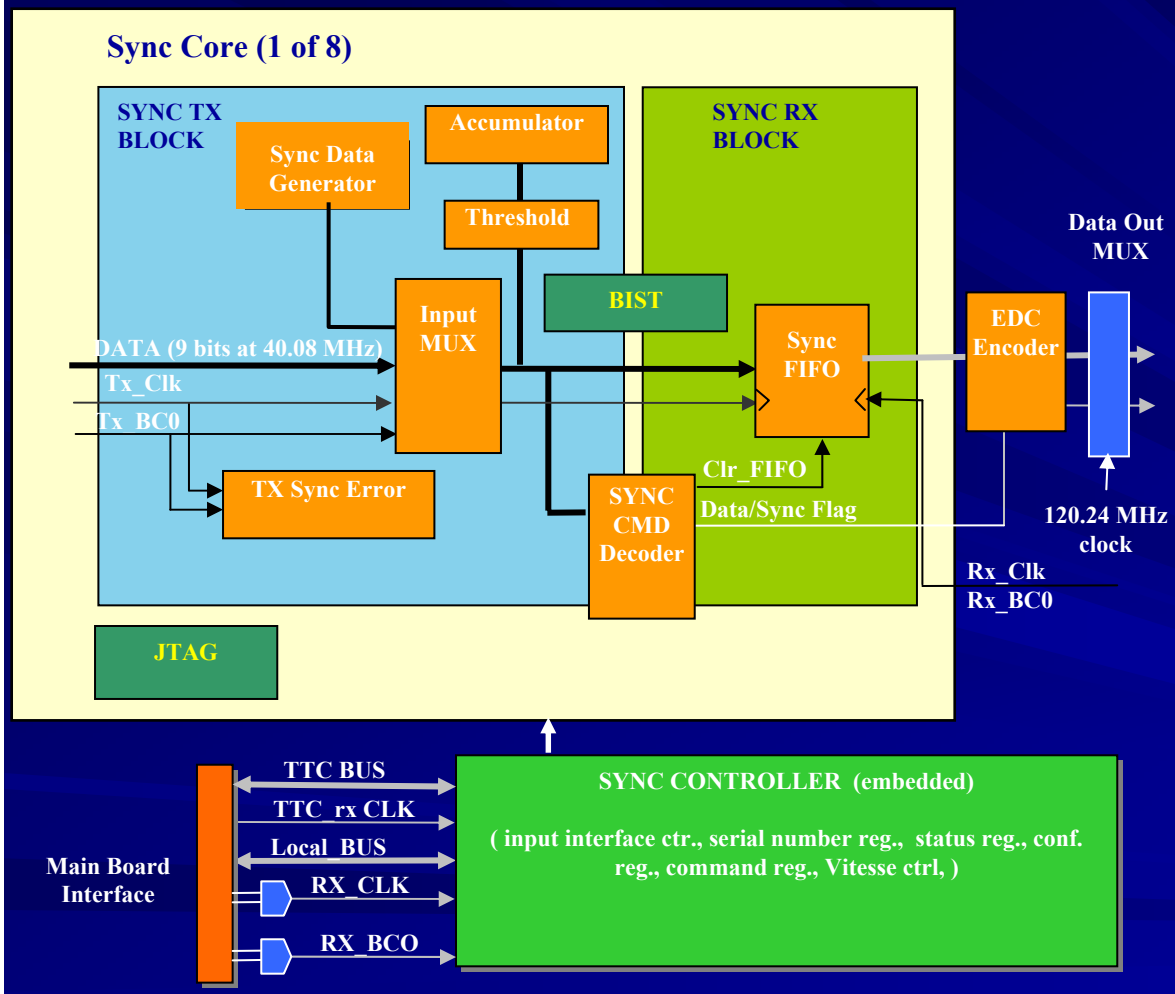
SLB – Functional Description

- Handles 8 Trigger Towers (8x 9bits @ 40.08MHz).
- Channels can be enabled/disabled to match different detector geometry.
- Trigger data alignment is performed in a channel basis using a FIFO stage.
- Accumulators that produce histograms reflecting the LHC orbit bunch structure are used to monitor the data alignment.
- Hamming code bits are added to the transmitted trigger data for data protection.
- Data are transmitted to the Regional Trigger over high speed links (1.2Gb/s).

Sync-Core Block Diagram



- Sync FIFO:
  - input with Tx_Clk; output with Rx_Clk.
  - FIFO is cleared every gap
  - Tx_BC0 synchonizes FIFO input
- Accumulator:
  - Histogram of Bunch Occupancy
  - Programmable Energy Threshold
- Rx_BC0 and Rx_Clk:
  - received synchronously by all channels
  - Rx_BC0 enables the read access of all FIFOs.
  - distributed by dedicated tree

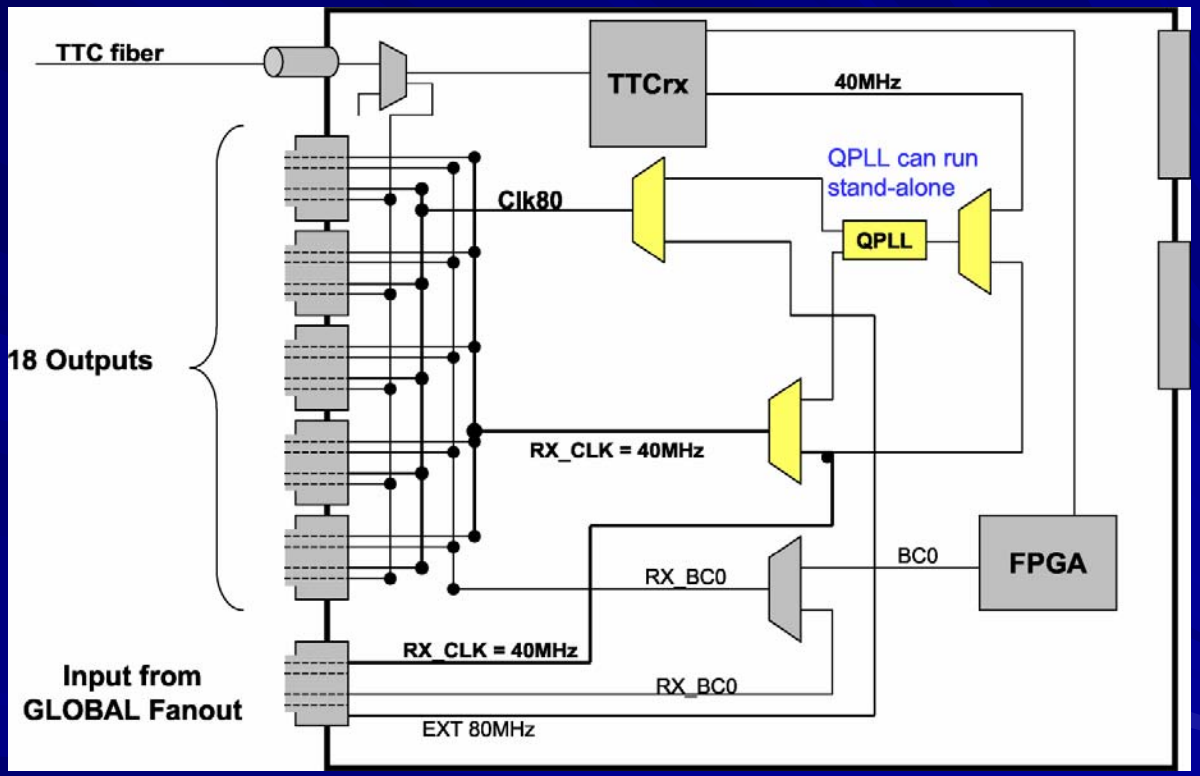
SLB – Implementation

- Functionality implemented in 2 Altera Cyclone EP1C6 FPGAs, EPC2 used.
- FIFOs with 128 words.
- Accumulators with 1024 positions.
- Data are protected with 5 Hamming Code bits per TT pair.
- External PLL clock multiplier to achieve jitter requirements for the high speed serialisers (100 ps pk-pk).
- Output bus with 4 x 8bits @ 120MHz , 4 copper high speed links (1.2Gb/s) using a Vitesse VSC7216 circuit with 8b/10b protocol.
- 90% of JTAG coverage.

Distribution of Clock and Sync Signals

- Local distribution tree of Rx_Clk and Rx_BC0 is build with Fanout Boards
- Common clock and BC0 is provided by TTC link

Fanout Board (2 operating modes: Global or Crate)

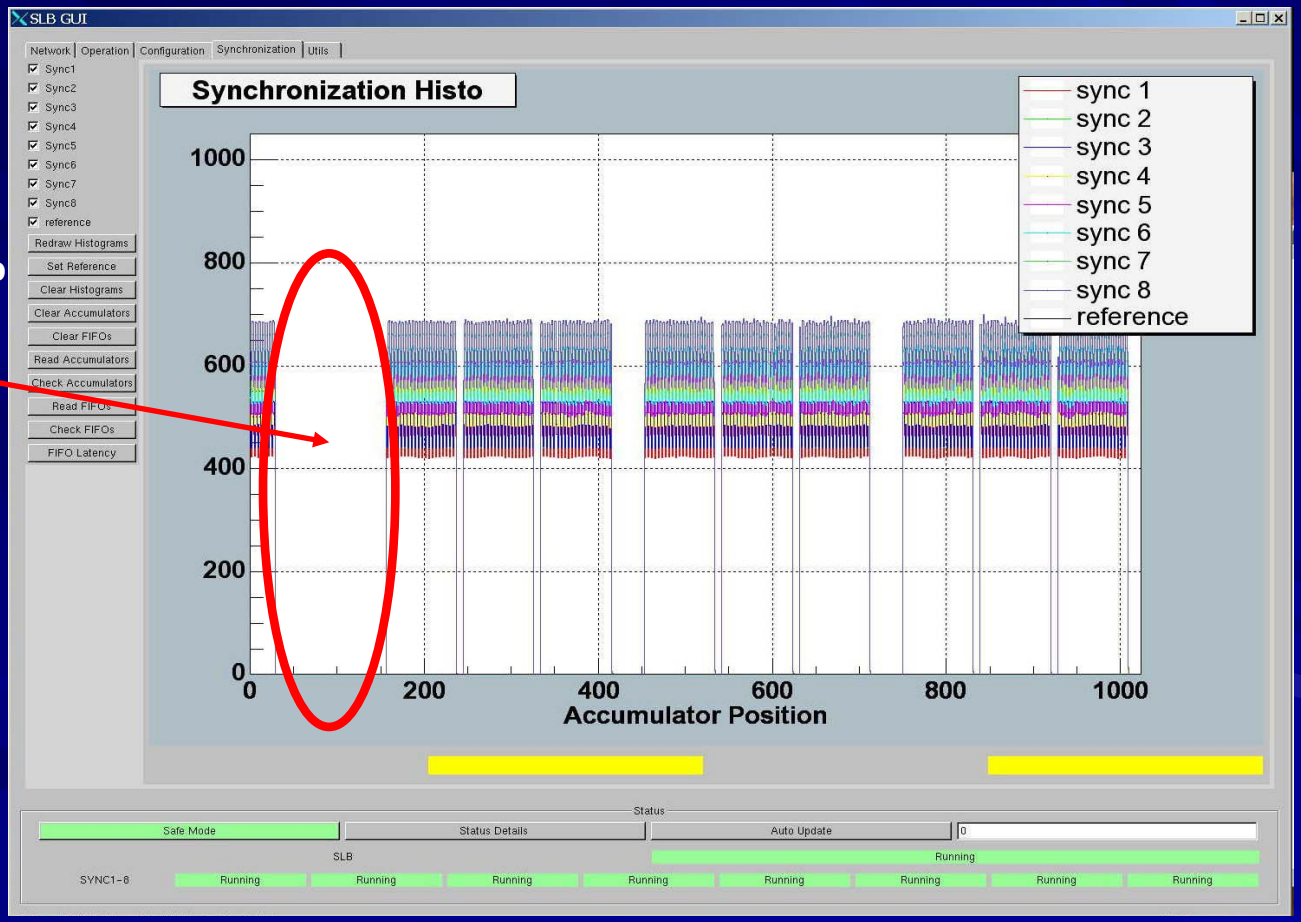


Developed by Princeton group

Trigger Data Alignment and Monitoring

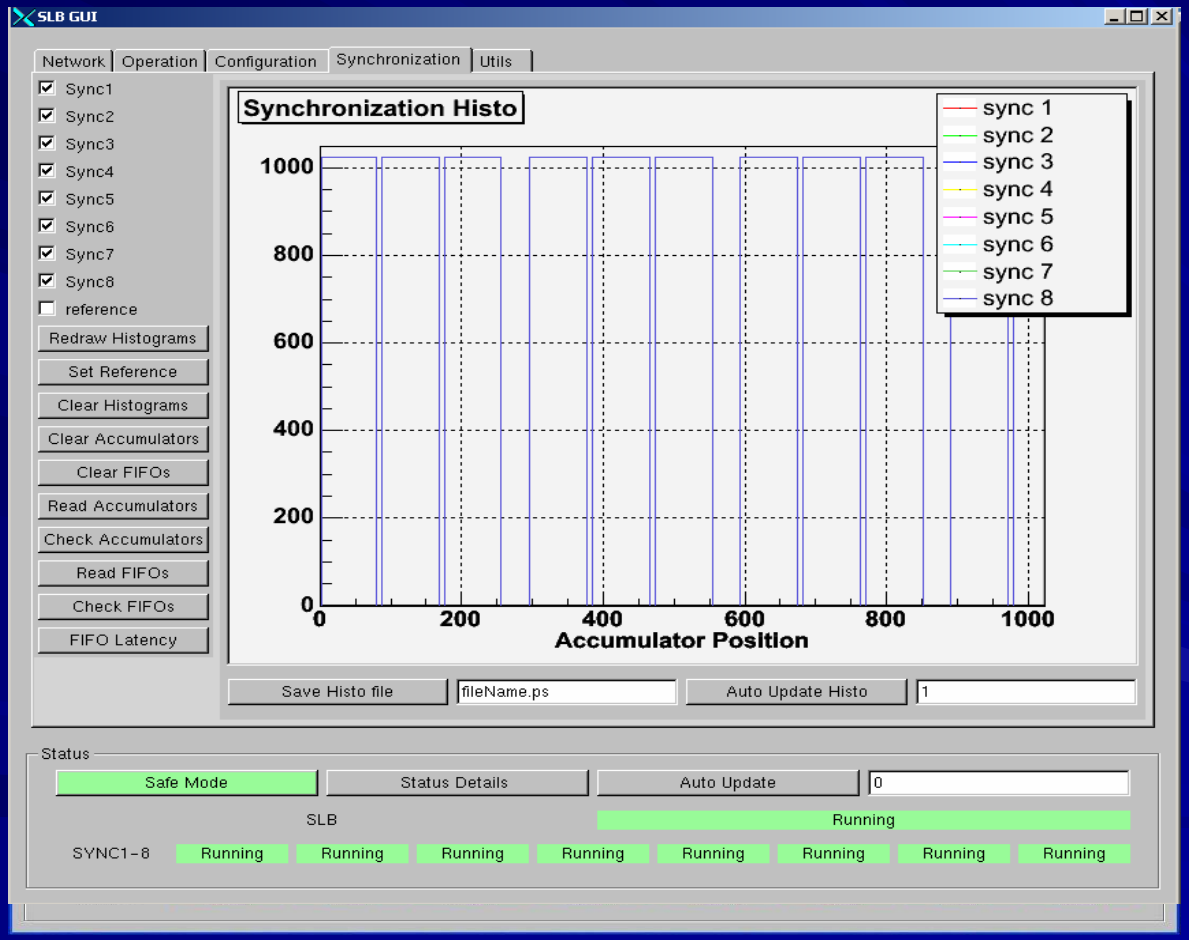
1) Coarse adjustments of the BC0 timing in the TTCci

Find the LHC main gap and align the first bunch written in the FIFOs with the start of the orbit



Trigger Data Alignment and Monitoring

2) Fine adjustments of Tx_BC0 using channel synchronization delays



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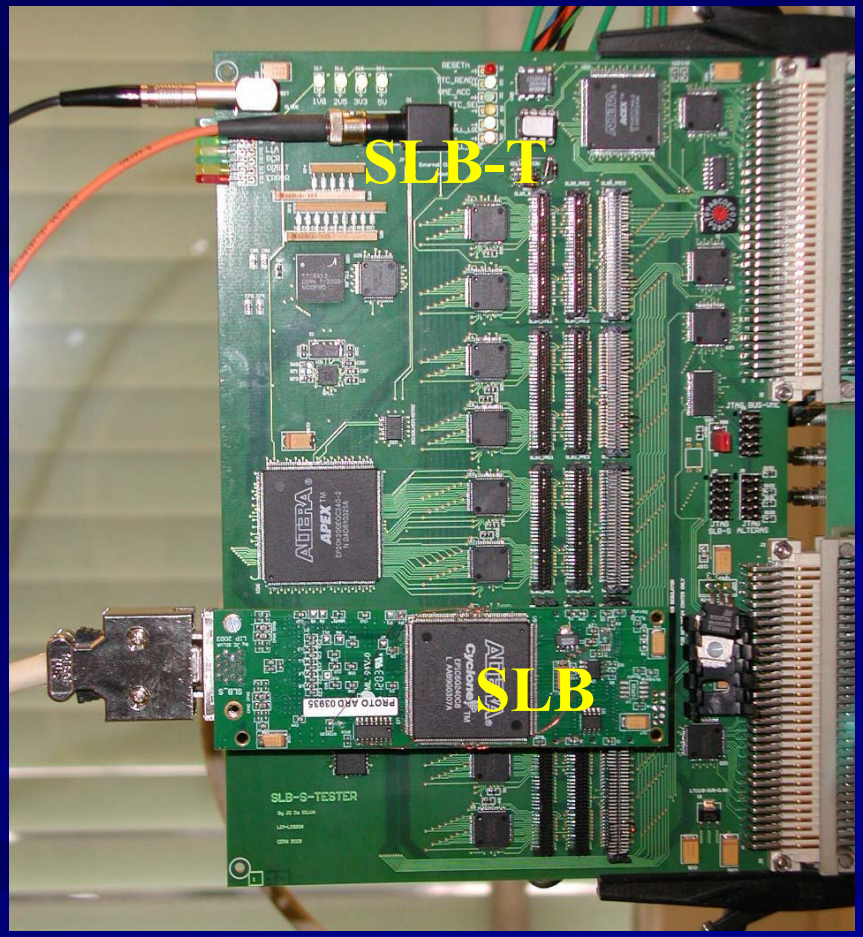
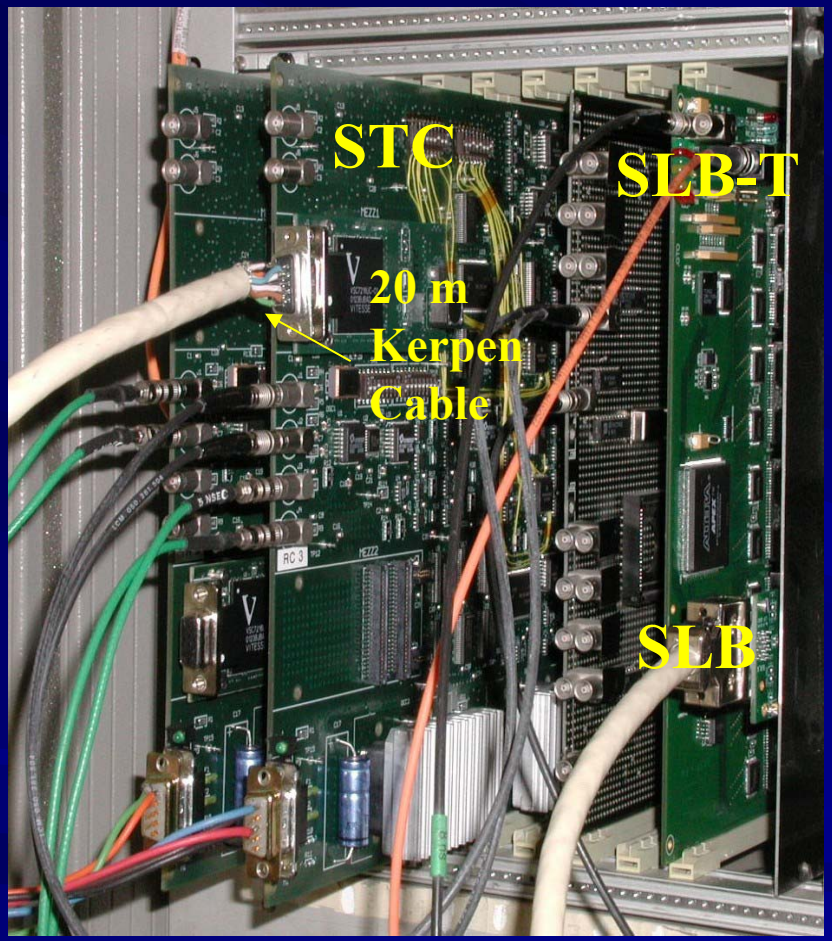
SLB Test Bench



SLB Tester (SLB-T)

- 6U VME board with 5 SLB slots.
- SLB Bus Controller.
- Trigger Data Emulator (3564x9bit).
- TTC Emulator.
- Low Jitter Clock Rx_Clk (QPLL).
- Synchronization Signal Rx_BC0.
- JTAG Port .

SLB Test Bench



Serial Transmitter Card (STC)

- Developed at the Univ. Wisconsin (Regional Calorimeter Trigger Test Bench).
- It works as a receiver/transmitter (Used in the test bench as a receiver).
- On fly SLB serial stream data comparison (32 bits at 120.24 MHz).

Production Test Bench

- 6U VME Crate , VME-PCI Interface, 5 STC, 1 SLB-T and 1 PC.
- Used to test 1300 SLB boards (650 ECAL and 650 HCAL).

SLB Production Tests

- **Check SLB Serial Number**

  VME readout of serial number must be equal to the board number.

- **Basic Test**

  Power-on configuration, reconfiguration, state transitions (VME and Broadcast).

- **FIFO Test**

  FIFO readout and cross-check against trigger data transmitted from SLB-T .

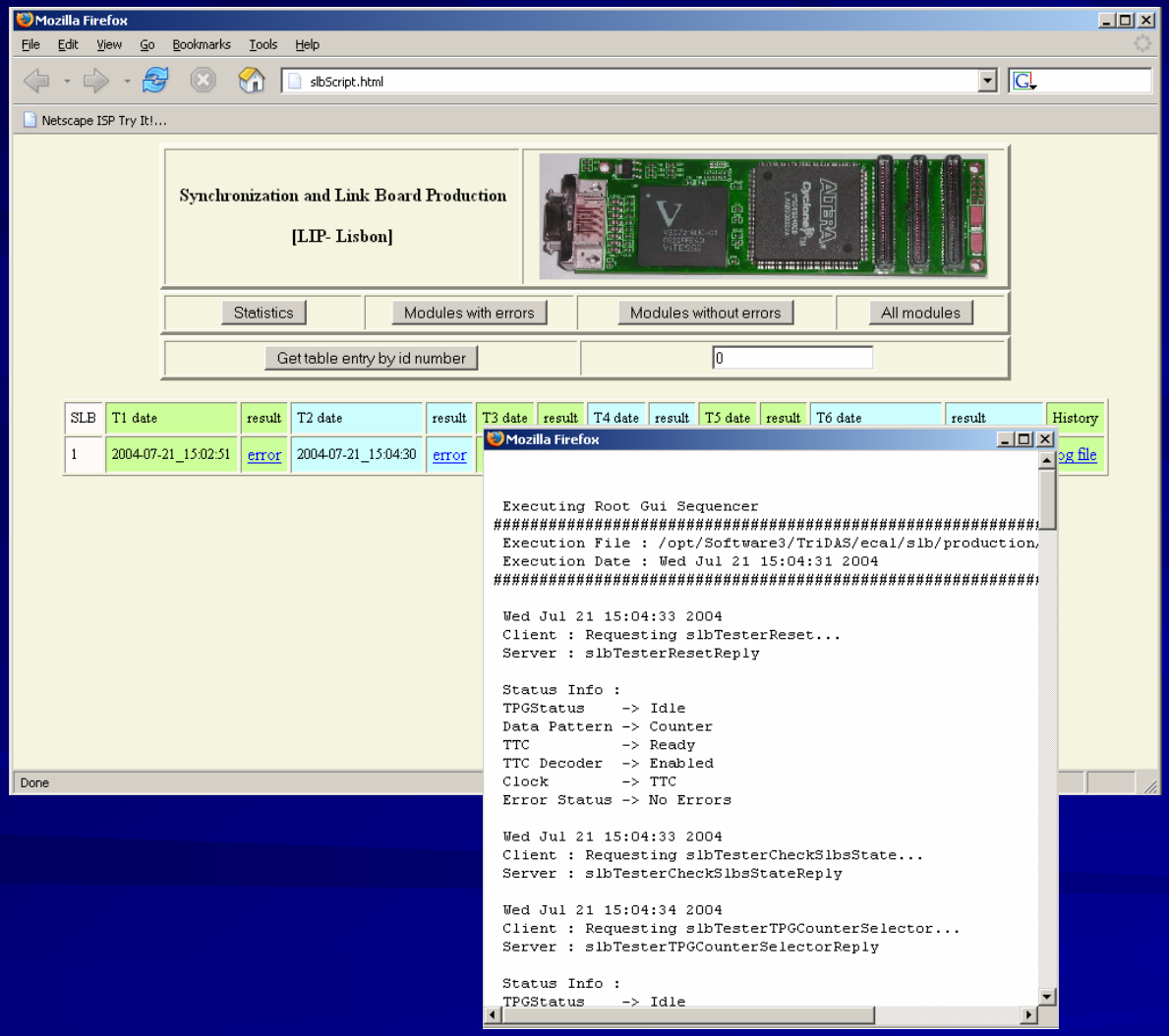
- **Accumulator Test**

  Test accumulator contents against different energy thresholds and channel delays.

- **Link Test**

  STC RAM readout and cross-check against the data transmitted from the SLB.
  BER measurements for some SLBs.

SLB Production Tests



- Test results are written in a XML file.
- A java script application allows users to query test results by SLB serial number and perform test statistics.
- Test log files are kept for reference.

SLB Pre-Production Performance Results

- Latency of 2 clock cycles on the trigger path.
- Data alignment stable for all synchronization channels.
- Link BER lower than 8.0×10^{-16}/s:
  No errors in 4 SLB links working at 1.2 Gbit/s during 72 hours.

Software

- **Developed in C++ and runs on Linux**
  - Code can be easily re-used in other systems and a user guide is available.

Dependencies :

- **XDAQ (CMS Distributed DAQ Framework)**
  - HAL (Hardware Access Library) for driver implementation and XDAQ applications to export the system functionality over the network.
- **Generic Configurator (developed by LIP)**
  - Hardware Configuration and data register manipulation.
- **ROOT (OO Analysis Framework)**
  - GUI and Histogramming.

Conclusions and Planning

- A method to synchronize the CMS Calorimeter Trigger Data (ECAL and HCAL) was developed and implemented with the SLB mezzanine board.
- Final pre-production SLB prototypes were produced and tested.
- A production test system based on SLB-T and STC boards was developed and implemented.
- A software package for SLB operation and testing based on XDAQ was developed.
- Integration tests with the TCC (ECAL), HTR (HCAL) and RC (Calo Regional Trigger) are under way.
- Production of 1300 SLBs is foreseen in Q4 2004.