CMS ECAL FENIX ASIC design methodology

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Abstract

A technique estimated to decrease risk when developing complex digital ASICs is presented. Specification errors as well as discrepancy between the product and the specification are addressed. The CMS ECAL FENIX ASIC development [1] is presented as an example.
The ASIC features a fully synthesizable and highly testable implementation of triple-redundancy.
The RAM blocks are individually tested by a built in self test, and an error correction code is protecting the data integrity during normal operation.

The ASIC has been irradiated during operation together with the complete CMS ECAL front end system, and a preliminary result is presented.

I. INTRODUCTION

The implementation of future electronics systems for HEP experiments will require highly sophisticated radiation hard electronics in order to meet the physical requirements and to be cost effective. A live example of such an electronics system is the CMS ECAL front end, which uses the FENIX application specific integrated circuit (ASIC). The FENIX ASIC functionality includes digital signal processing for trigger primitive generation, RAM for temporary data storage, and a large number of configuration registers and finite state machines.

II. THE FENIX ASIC DEVELOPMENT

By the time the development of the new CMS ECAL front end and the FENIX ASIC started, the physics and the system requirements were well known. The physical requirements were, however, to be defined taking the available space inside the already existing detector design into account.

The previous readout system had all main functions implemented in FPGAs, thus upgradeable by uploading new firmware. Efforts have been made to make the new system, implemented in ASICs, flexible enough for the changing environment at LHC and beyond.

The development of the FENIX ASIC was made in six steps:

0) Development of a design kit for a 0.25u CMOS process [2]

1) Specification based on physics as well as on physical and system requirements

2) HDL code development

3) Validation of the HDL description by implementing the full functionality in an FPGA

4) Implementation of an ASIC based on the validated HDL description

5) Verification of the functionality of the system, as well as of the system performance under radiation

In order to achieve a seamless design flow, step 2, 3 and 4 where performed partly in parallel. Obviously, step 0 was not performed at all within the project.

The ASIC has been implemented using Synopsis for synthesis and Silicon Ensemble for place and route. The design flow provides a very short design turnaround of two weeks and in theory even less than a week.

Silicon ensemble is a powerful place and route tool, providing the operator with a functionality approaching a place and route tool for modern FPGAs. In order to achieve a predefined pin-out the bond pad placement is entered by hand. The tool set is then capable of a fully automatic power supply rail definition, clock tree insertion, component placement and final routing.

The practical work has been split between three institutes. LLR, France has contributed with the algorithm and verification of the trigger primitive generation functions, CERN, Switzerland, has contributed with the global functionality, system integration and FPGA demonstrator, and RAL, UK, has performed the ASIC implementation and the preliminary tests of the ASIC. The concept permits to keep the complex functionality close to the physics community while leaving the complicated and skill demanding ASIC layout to an expert, thus to gain time and possibly decrease the number of iterations.

III. RADIATION HARDNESS

The main technique for radiation hardness is obviously to implement the ASIC in a radiation hard or at least a radiation tolerant technology. In the case of the FENIX ASIC, a mature 0.25u CMOS process associated with a well debugged and validated custom library have been used [2]. The chosen technology provides a very high resistance to total dose, but registers are subject to Single Event Upsets (SEU). Well known techniques, described below, have been used to cope with SEU. Specifically, the configuration registers as well as the finite state machines have been made triple-redundant, any data stored in RAM receive an error correction code (ECC), and DSP blocks are doubled in order to allow error detection followed by adequate action.

A. Triple redundant configuration register

The triple redundant register in a configuration register is in fact three standard registers connected as shift registers. The "first" register has a two input multiplexer on the input. In normal operation the voted value of the three registers is fed back to the input. When updating the content, the new value is fed for at least two clock cycles while enabling the “wena” line. Please see Figure 1.

B. Triple redundant finite state machine register

The registers in a finite state machine have to be able to change value in a single clock cycle. In order to allow this, the "first" and the "second" register have both a two input multiplexer on the input, and a new value need then to be fed for only one clock cycle. It can be noted that the architecture is efficient especially when the register is updated rarely. Please see Figure 2.

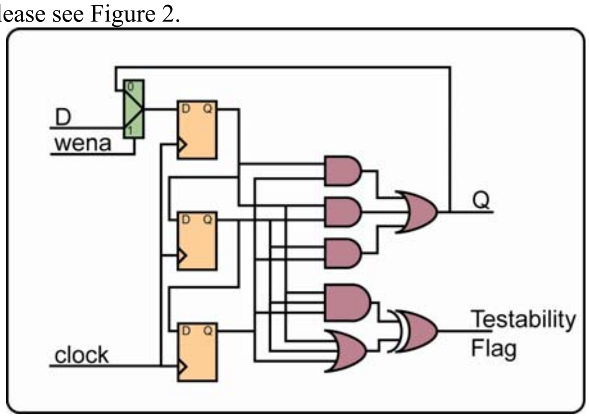

Figure 1: Triple redundant configuration register

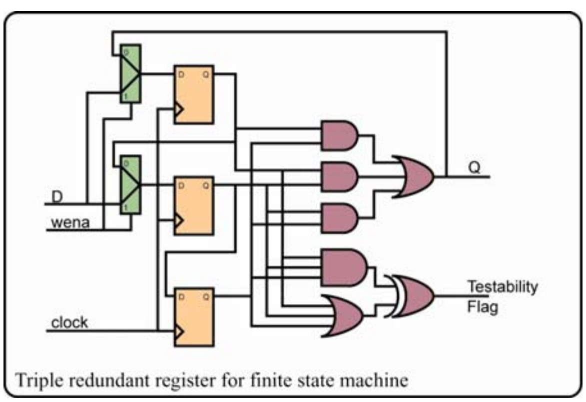

Figure 2: Triple redundant Finite State Machine register

C. ECC in RAMs

Any data written in a RAM has a hamming code attached in order to cope with SEU. The RAM cell used in the FENIX ASIC [3,4] has logically adjacent cells located also physically adjacent. In a study done within the ATLAS pixel community it has been shown that the probability of having a two bit single event upset (SEU) in two physically adjacent RAM cells is between 2 and 4 times as high as if the two RAM cells are physically separated.

The ECC scheme adopted for the FENIX ASIC is slightly more elaborated than just adding a hamming code to the 16 bit data word, as visualised in Figure 3.

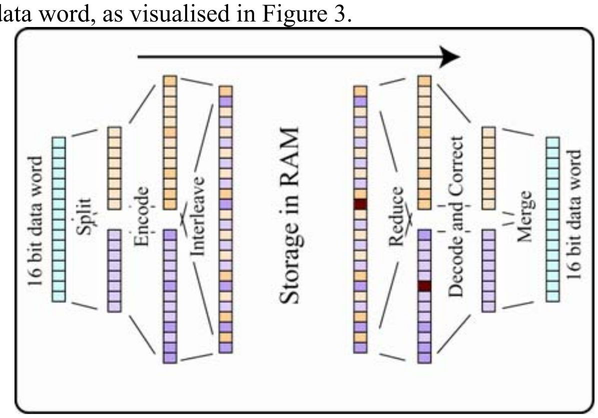

Figure 3: ECC Encoding, Decoding and Correction scheme

The 16 bit data word is split the word into two 8 bit words. An individual hamming code [5] is calculated and added to each of the two. As a last step before storage the two encoded words are interleaved in order to prevent a double adjacent bit SEU from being part of the same encoded word.

The decoding and correction is done in the reverse order. The correction can be completely disabled.

In case of detected errors the immediate reaction is programmable depending on the type of data contained in the RAM. In the FENIX, two types of data are stored in RAM: Channel data and Pointers. The action strategy upon error is different between the two as follows:

1) Channel data SEU correction strategy

Single error detected:

- Correct error and send without flag (default)
- Correct error and send with “parity” error inserted
- Set to zero and send
- Set to zero and sent with “parity” error inserted

Double error detected:

- Send uncorrected
- Send uncorrected with “parity” error inserted
- Set to zero and send
- Set to zero and sent with “parity” error inserted (default)

2) Pointer data SEU correction strategy

Single error detected:

- Correct and send (default)
- Cancel and send empty event

Double error detected:

- Send uncorrected
- Cancel and send empty event (default)

D. DSP Error Detection

The DSP in the FENIX ASIC is used for level 1 trigger primitive generation. It consists of one lineariser per channel, one five channel adder, and a five tap Finite Impulse Response (FIR) filter with a peak finder for bunch crossing identification.

In the FENIX ASIC, the FIR with the peak finder is duplicated. The two instances of the FIR are receiving the same input data. If the two filters are configured identically, they should produce identical results unless calculation error or SEU.

In order to detect SEU, or calculation errors, the two outputs are simply compared. In case of discrepancy, proper action is taken. The action is programmable: Discrepancy can be flagged only, or set to zero and flagged, or set to zero without flagging.

The dual filter is adding a few interesting features:

1) SEU detection, as mentioned above, is the default
2) One bunch crossing identification filter and one energy estimation filter
3) Fault tolerance by selecting one or the other filter without comparing with the other filter output
4) Changing filter depending on VFE gain, then using different configuration for the two filters
5) Sending the output of the filter with the largest output, while flagging the decision. This is the mode foreseen for 80 MHz operation; a flag is informing about the filter, and subsequently the bunch crossing, or pseudo-bunch crossing, selected to higher levels

Especially operation mode 5 need studies in order to achieve optimal operation. Under some circumstances it might be the optimal mode even at LHC operation. However, it is to be noted that calculation errors can only be detected in mode 1.

IV. TESTABILITY

The testability of the ASIC is an issue due to the relatively complex functionality of the ASIC itself and the fact that the system will be mounted on the detector, inaccessible for the life time of the experiment. Any undetected defect may deteriorate the performance of the system or may induce hot spots on the chip surface which in turn may lead to a premature failure of the chip thus the system.

A. Triple redundant registers

The triple-redundant registers, please see figure 1 and 2, are testable by the implementation of a testability flag, flagging any discrepancy in the content of the three registers forming one effective single triple-redundant register. The flag of every triple-redundant register is XORed to form a global testability bit which can be considered as a "signature of operation", since discrepancies occur very often during normal operation. During the operation of the chip in the test rig, the bit is monitored as any other bit and is used to screen defective chips during production testing. Once mounted on a module, the bit can be left unwired or wired to a test point as currently on the CMS ECAL Front End card.

B. RAM BIST

The RAM blocks are production tested by a built in self test (BIST), testing all bits for stuck-at faults and shorts between adjacent bits, as well as for faults on the address bus. The sequence is:

1) Write all locations in the RAM
2) Read all locations and compare to the written values

The start address is programmable with the slow control and defaults to 0xA. The operation is performed on each of the 16 RAM blocks with five more or less classical patterns:

1) 2AAAAAA- 5555555 - 2AAAAAA etc.
2) 5555555 - 2AAAAAA - 5555555 etc.
3) 0000000 – 7FFFFFF – 0000000 etc.
4) 7FFFFFF – 0000000 - 7FFFFFF etc.
5) Counter starting at 0

The BIST is started by pulling an input pin active for at least three clock cycles. The BIST structures are not triple-redundant, only the start register is. The BIST can also be initiated or completely disabled through the slow control port. The result can be read back through the same channel, making it possible to test and re-test the RAM blocks in situ. It is to be noted that the BIST is operating on the bare RAM. The ECC encoder and decoder are tested with operational test vectors.

V. RADIATION HARDNESS VERIFICATION

The complete CME ECAL Front-end has been irradiated in order to confirm the resistance to radiation and to verify the immunity to single event upset (SEU).

The Optis facility at PSI was used as a source of 63 MeV protons at an intensity of 1.25 E+9 p/cm2/s, corresponding to 1.7 E+2 RAD/s. The targeted dose, corresponding to around 10 years of LHC operation in the CMS ECAL barrel, is received in 2h30m. A picture of the setup can be seen in Figure 4.

The system was operated during the irradiation, and the resulting data was read out. The result is difficult to analyze due to the lack of errors detected in the data. However, some problems were detected while operating the slow control system. It is not clear what caused the problems, forcing the exclusion of a part of the system under test during the second half of the test period. The full system was recovered the day after the irradiation stopped and no errors were detectable. The result is considered satisfactory, and the production of the ECAL electronics can be started. More studies will be performed as soon as production units are available.

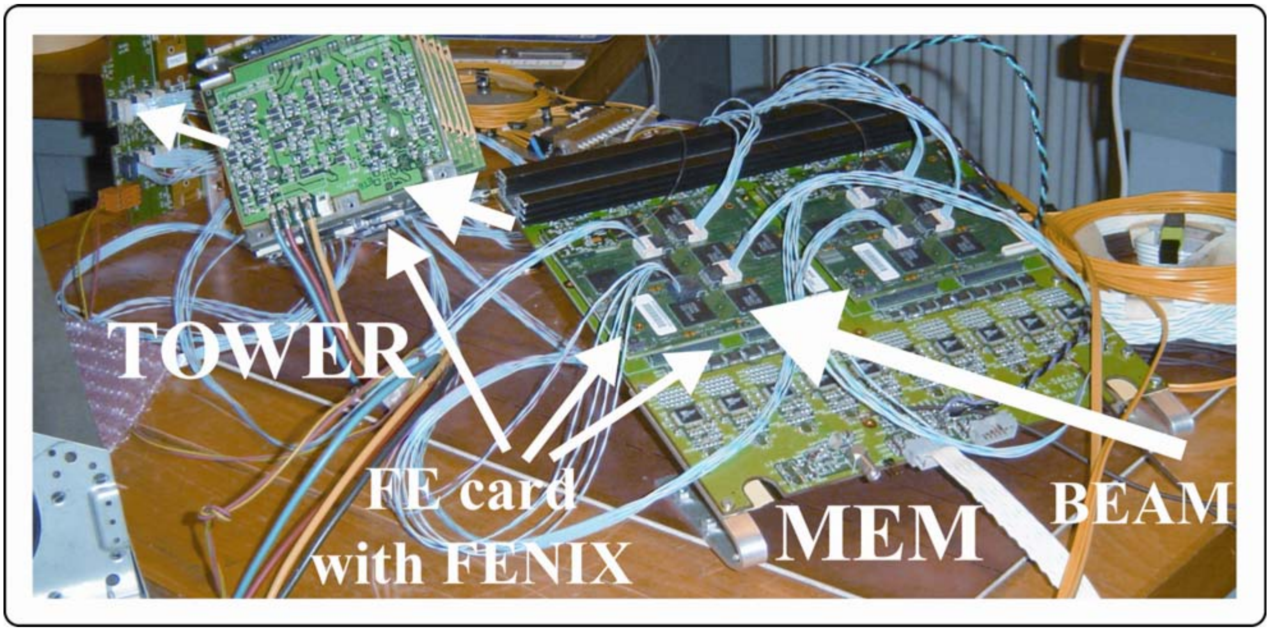

Figure 4: Irradiation setup for the CMS ECAL front end

VI. VI. REFERENCES

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