CMS ECAL FENIX ASIC design methodology

For the CMS ECAL electronics community (Magnus.Hansen@cern.ch)

Introduction

The implementation of future electronics systems for HEP experiments will require highly sophisticated radiation hard electronics in order to meet the physical requirements and to be cost effective. A live example of such an electronics system is the CMS ECAL front end, which uses the FENIX application specific integrated circuit (ASIC). The FENIX ASIC functionality includes digital signal processing for trigger primitive generation, RAM for temporary data storage, and a large number of configuration registers and finite state machines.

The FENIX ASIC Development

By the time the development of the new CMS ECAL front end and the FENIX ASIC started, the physics and the system requirements were well known. The physical requirements were, however, to be defined taking the available space inside the already existing detector design into account.
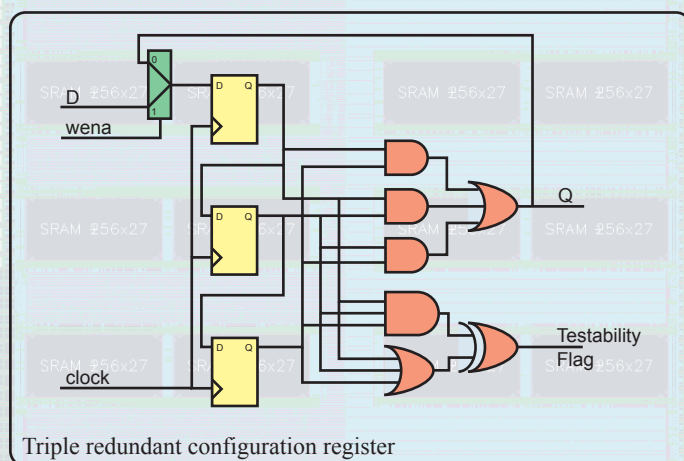
The previous readout system had all main functions implemented in FPGAs, thus upgradeable by uploading new firmware. Efforts have been made to make the new system, implemented in ASICs, flexible enough for the changing environment at LHC and beyond.

Well known techniques have been used to make the system radiation tolerant. Specifically, the configuration registers as well as the finite state machines have been made triple-redundant, and any data stored in RAM receive an error correction code (ECC). The development of the FENIX ASIC was made in six steps:

0) Development of a design kit for a 0.25u CMOS process
1) Specification based on physics as well as on physical and system requirements
2) HDL code development
3) Validation of the HDL description by implementing the full functionality in an FPGA
4) Implementation of an ASIC based on the validated HDL description
5) Verification of the functionality of the system, as well as of the system performance under radiation

In order to achieve a seamless design flow, step 2, 3 and 4 where performed partly in parallel. Obviously, step 0 was not performed at all within the project.

The ASIC has been implemented using Synopsis for synthesis and Silicon Ensemble for place and route. The design flow provides a very short design turnaround of 2 weeks, and in theory even less than a week.

Silicon ensemble is a powerful place and route tool, providing the operator with a functionality approaching a place and route tool for modern FPGAs. In order to achieve a predefined pin-out the pad placement is entered by hand. The tool set is then capable of a fully automatic power supply rail definition, clock tree insertion, component placement and final routing.

Triple redundant configuration register

Triple redundant register for finite state machine

ECC encoding and decoding scheme

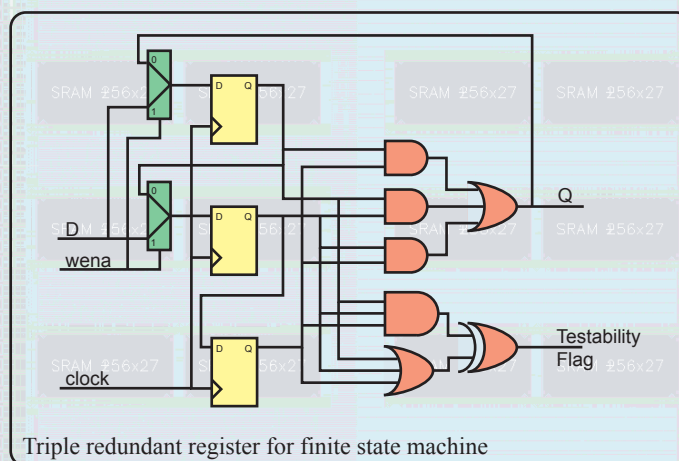### Triple redundant configuration register

The triple redundant register in a configuration register is in fact three standard registers connected as shift registers. The "first" register has a two input multiplexer on the input. In normal operation the voted value of the three registers is fed to the input, and when updating the content, the new value is fed for at least two clock cycles.

Triple redundant finite state machine register

The registers in a finite state machine have to be able to change value in a single clock cycle. In this case, the "first" and the "second" register have both a two input multiplexer on the input, and a new value need then to be fed for only one clock cycle.
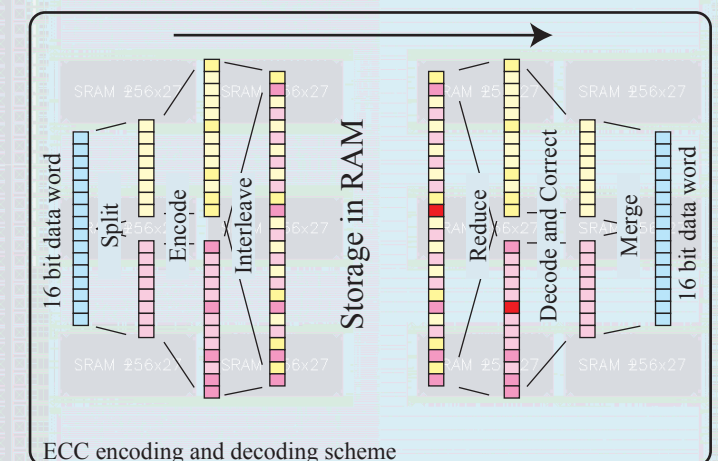
ECC in RAMs

Any data written in a RAM has a hamming code attached in order to cope with SEU. In a study done within the ATLAS pixel community it has been shown that the p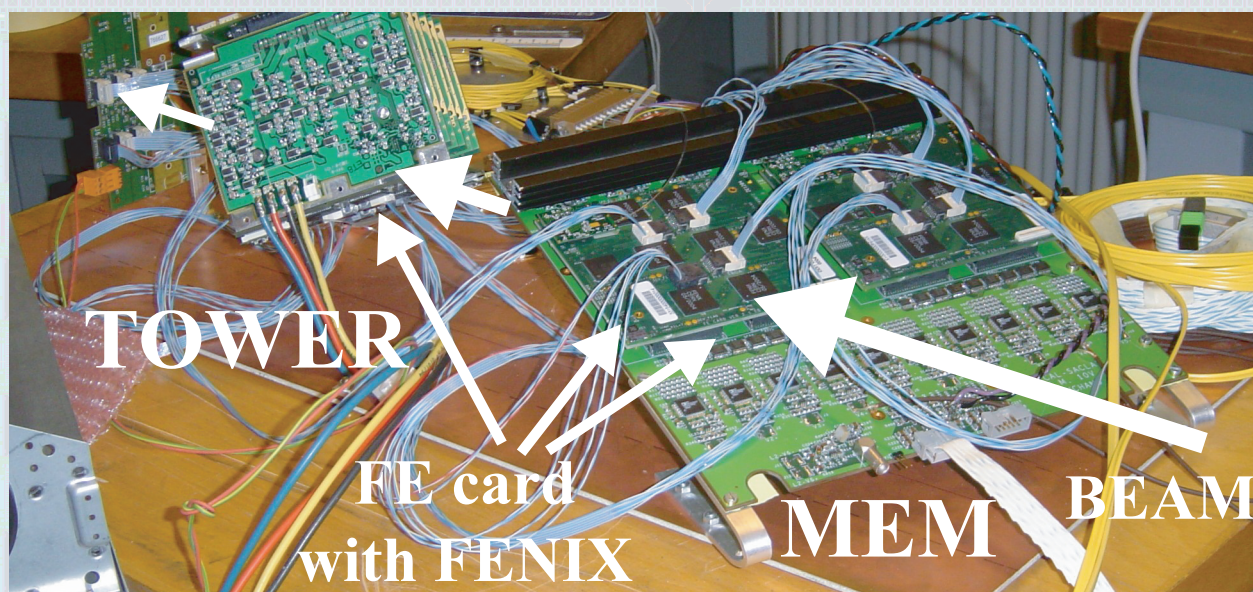robability of having a two bit single event upset (SEU) in two physically adjacent RAM cells is between 2 and 4 times as high as if the two RAM cells are physically separated. The ECC scheme adopted for the FENIX ASIC is to split the word into two, add the hamming code for each of the two, and interleave the two words. Thus, any SEU in physically adjacent cells belong to two different encoded words, and can thereby be correctly decoded with a higher probability compared to a single hamming code. Nevertheless, the error handling strategy is programmable in order to be able to decide at a later stage what to do in case of errors. Among the possibilities are "correct and send", "correct, flag and send" and "flag and cancel".

Testability

The testability of the ASIC is an issue due to the relatively complex functionality of the ASIC itself and the fact that the system will be mounted on the detector, inaccessible for the life time of the experiment. Any undetected defect may deteriorate the performance of the system and, worse, may induce hot spots on the chip surface which in turn may lead to a premature failure of the chip thus the system.

The triple-redundant registers are testable by the implementation of a testability flag, flagging any discrepancy in the content of the three registers forming one effective single triple-redundant register. The RAM blocks are production tested by a built in self test (BIST), testing all bits for stuck-at faults and shorts between adjacent bits, as well as for faults on the address bus. It is to be noted that the BIST is operating on the bare RAM. The ECC encoder and decoder are tested with operational test vectors.

Radiation Hardness Verification

The complete CME ECAL Front-end has been irradiated in order to confirm the resistance to radiation and to to verify the immunity to single event upset (SEU).

The Optis facility at PSI was used as a source of 63 MeV protons at an intensity of 1.25 E+9 p/cm2/s, thus the targeted dose, corresponding to 10 years of LHC operation in the CMS ECAL barrel, in 2h30m.

The system was operated during the irradiation, and the resulting data was read out. The result is difficult to analyze due to the lack of detected errors in the data. Some problems were, however, detected while operating the slow control system. It is not clear what caused the problems, forcing the exclusion of a part of the system under test during the second half of the test period. However, the full system was recovered the day after the irradiation stopped and no errors were detectable. The result is considered satisfactory, and the ECAL electronics can be produced. More studies will be performed as soon as production units are available.

Irradiation Setup for the CMS ECAL Front end

TOWER

FE card with FENIX

MEM

BEAM