FED board parameters:
- Each board reads out 25,000 silicon strips (multiplexed analogue data)
- Each board provides data reduction from 3 Gbytes/s to 200 Mbytes/s
- 9U x 440 mm VME64x form factor
- Optical/Analogue/Digital logic; 96 ADC channels
- Double-sided (secondary side with half of analogue channels)
- 6,000 components (majority of passives 0402) (finest pitch < 20 μm)
- 25,000 tracks
- 37 BGAs (typical FPGA 676 pins on 1mm pitch). All BGAs located on primary and secondary sides
- 14 layers (incl. 6 power & gnd)
- controlled impedance

FED board production history:
- 5 prototypes FEDv1 successfully made by September 2003
- 6 further prototypes all had major manufacturing faults (shorts and cold spots)
- Subsequent 8 prototypes made by a candidate company for full production
Responsible for pcb manufacture and assembly (and component required). “One stop shop” solution.

Data for pcb manufacture accepted in ODB++ format.

Pcb tested by flying probe.

Results of re-flow for FED second.

Other Issues:
- Cost of components (FPGAs, Opto-Rx modules) dominates.
- BGA rework is problematic.
- High channel count per board. Need close to 100% accuracy.
Production:

Assembling several hundred large and complex boards in ~12 months. An important goal is to identify and fix almost all minor manufacturing faults early, i.e. at the early plant need to be quick and simple to operate yet thorough. The plant has been designed with testing in mind.

Testing by Assembly plant operatives.

Digital testing at Assembly plant:
- All digital devices on JTAG Boundary Scan.
- Verifies connectivity between digital inputs.
- Custom loop back cards to test plane connectors.

Analog testing at Assembly plant:
- DACs on all 96 analogue channels perform separate standalone tests without the need for optical inputs.
- Opto-Rx modules tested at CERN being custom Linux based LabView & C++ tester to Assembly company for single board.
- Lookup tables to associate reported hardware components for quick diagnosis.

Digital: Boundary Scan.

Full system tests at RAL:
- Carried out by RAL engineers.
- Full soak tests with multiple FE.
- Using optical inputs and fast DACs.

Final commissioning at CERN: