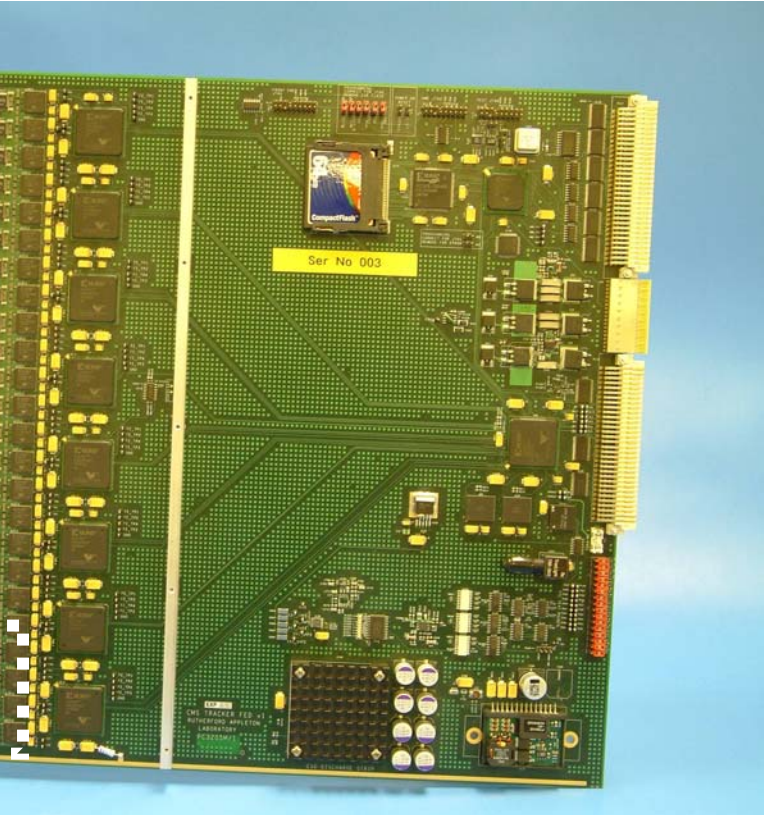
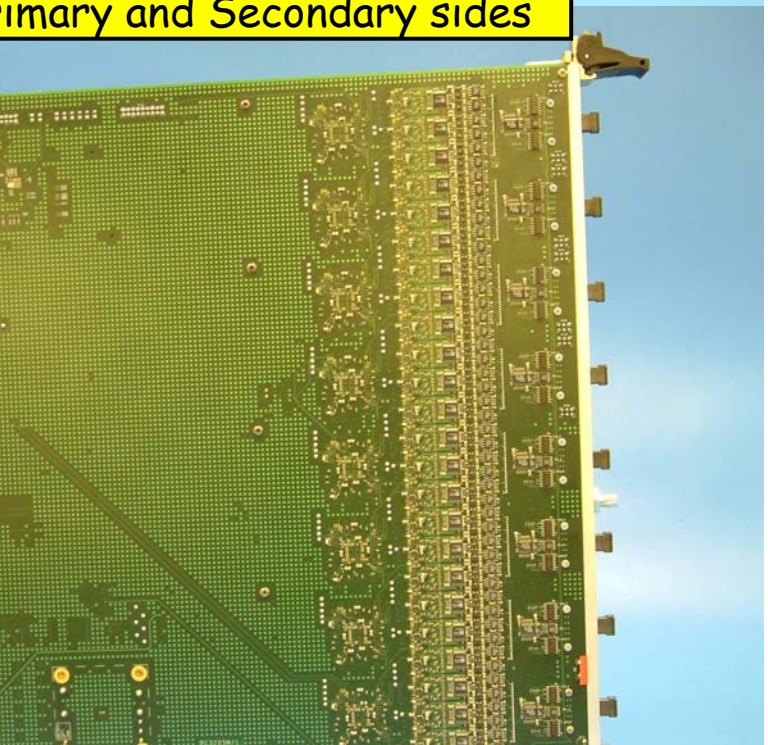
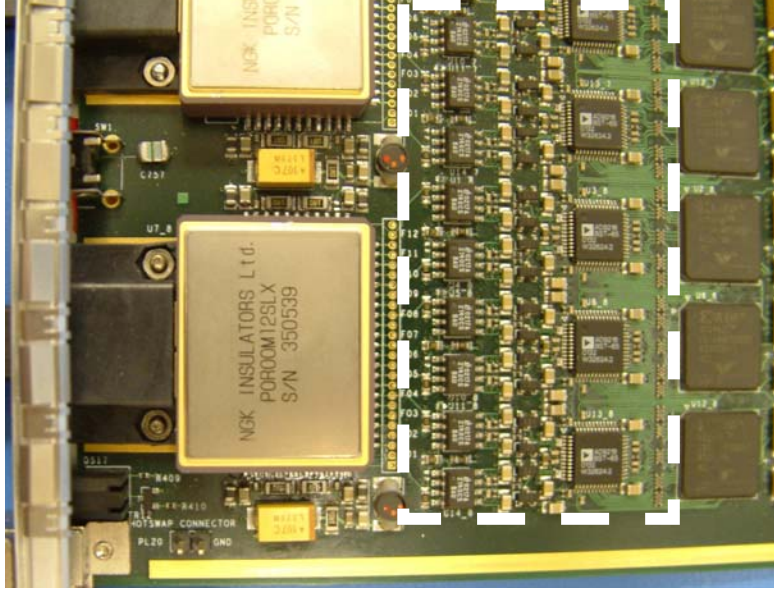


imary and Secondary sides





High density components.
Close up of analogue sect
on primary side (indicate
region is repeated on
secondary side).

Almost all components on
board are surface mount.

FED board parameters:

- Each board reads out 25,000 silicon strips (multiplexed analogue
- Each board provides data reduction from 3 Gbytes/s to 200 Mby
- 9U x 440 mm VME64x form factor
- Optical/Analogue/Digital logic ; 96 ADC channels
- Double-sided (secondary side with half of analogue channels)
- 6,000 components (majority of passives 0402) (finest pitch < 20 t
- 25,000 tracks
- 37 BGAs (typical FPGA 676 pins on 1mm pitch). All BGAs located
- 14 layers (incl. 6 power & gnd)
- controlled impedance

FED board production history:

- 5 prototypes FEDv1 successfully made by September 2003
- 6 further prototypes all had major manufacturing faults (shorts
- Subsequent 8 prototypes made by a candidate company f or full p

e:

esponsible for pcb manufacture and assembly (and component equired). "One stop shop" solution.

a for pcb manufacture accepted in ODB++ format.

e pcb tested by flying probe.

dance measurements provided.

ss:

ed for programming assembly and test machines.

nachines (e.g. MyData 12, 20,000 placements/hour).

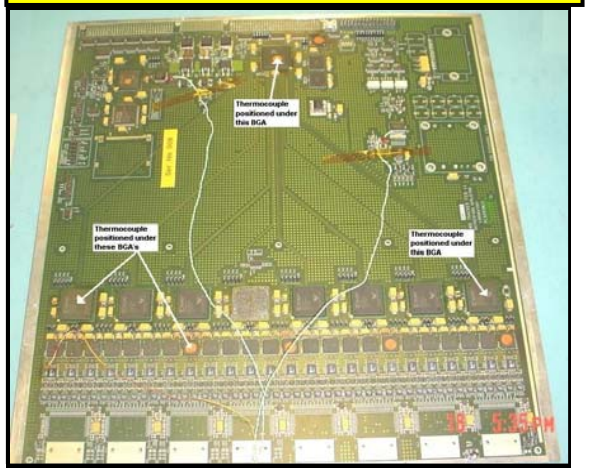
rofiled using populated scrap boards.

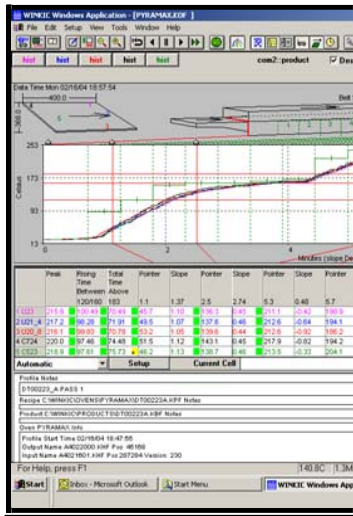
frames used to hold 9U boards during assembly.

ocedures	Quality Controls
le	
	Paste Height check
e machine assembly	
	1st off AOI inspection
	Paste Height check
e machine assembly	BGA placement check with Ersascope™
	1st off AOI inspection
	Standard AOI inspection
	Surface Mount manual inspection
	X-Ray inspection of BGAs Ersascope inspection of BGAs

Example of a surface mount assemb

Scrap FED fitted with thermocouples for oven profile.





Results of re-flo for FED seconda

Other Issues:

- Cost of components (FPGAs, Opto-Rx modules) dominat
- BGA rework is problematic.
- High channel count per board. Need close to 100% acce

uction:

sion several hundred large and complex boards in ~12 months.

ntify and fix almost all minor manufacturing faults early, i.e. at the

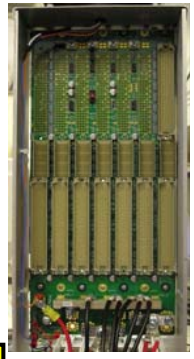
ly plant need to be quick and simple to operate yet thorough.

been designed with testing in mind.

Digital testing at Assembly plant

- All digital devices on JTAG Boun
- Verifies connectivity between di
- Custom loop back cards to test s plane connectors.

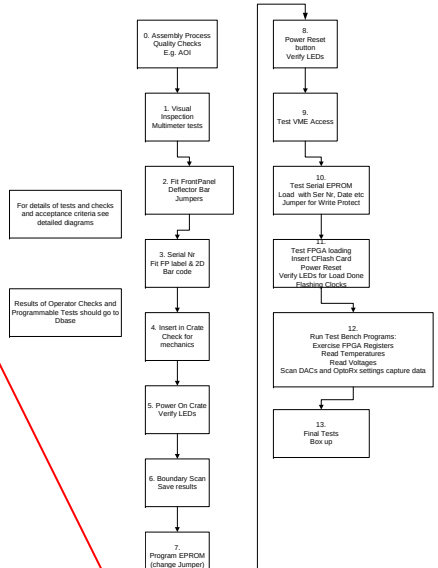
Testing by Assembly plant operatives.

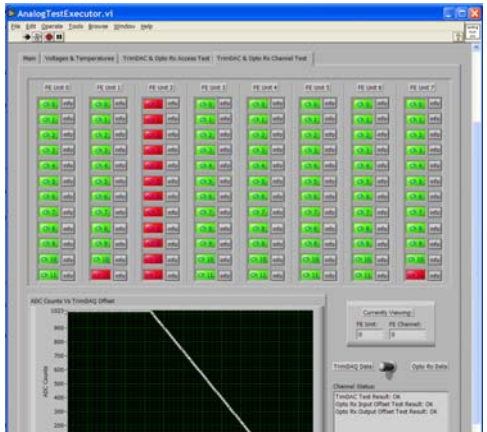


Analogue testing at Assembly plant:

- DACs on all 96 analogue channels per rate standalone tests without the nee inputs.
- Opto-Rx modules tested at CERN be
- Custom Linux based LabView & C++ te to Assembly company for single board
- Lookup tables to associate reported hardware components for quick diagno

Digital: Boundary Scan.





Full system tests at RAL:

- Carried out by RAL engineers.
- Full soak tests with multiple FE
- Using optical inputs and fast DA

Final commissioning at CERN: