ALICE DDL Radiation Tolerance Tests for the FPGA Configuration Loss

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Abstract

The ALICE Detector Data Link (DDL) is a high-speed optical link designed to interface the readout electronics of ALICE detectors to the DAQ computers. The Source Interface Unit (SIU) of the DDL will operate in radiation environment. We have tested the radiation tolerance of the semiconductor components of the SIU card. The configuration loss of the logic devices has proved to be the only critical point where the prototype design does not fulfil the requirements. We developed special tests to investigate the configuration damage of FPGAs. Several series of tests have been carried out for the different FPGAs based on SRAM and on flash technologies. The results of these measurements are compared and discussed in the paper.

I. INTRODUCTION

ALICE will use 400 detector data links (DDL) for the data transmission from the detectors to the computers [1]. Each link consists of two interface cards – the Source Interface Unit (SIU) and the Destination Interface Unit (DIU) – and a duplex, multimode optical cable of up to 300 meters. The SIUs will be attached to the Front End Electronics (FEE) of the detectors. On the other side, DIUs will be connected to Read-Out Receiver Cards (RORC), that are PCI cards in the host computers. The SIU cards of the DDLs have to work in the radiation field of the ALICE detector. The radiation level will be the highest for those SIUs that are installed at the inner radius of the TPC subdetector [2]. The expected doses and hadron fluences were obtained from simulations by assuming a specific running scenario for 10 years of LHC operation [3]. (See Table 1).

Table 1: The expected doses and hadron fluences for 10 years

Total dose	D=16 Gy = 1.6 krad
Neutron fluence	$F_{neutron} = 3.9 \cdot 10^{11}$ cm^{-2}
Charged hadron fluence	$F_{ch.\ hadron} = 8 \cdot 10^{9}$ cm^{-2}
Neutron fluence rate in Pb-Pb	dF/dt = 460 cm^{-2}s^{-1}
Neutron fluence rate in p-p	dF/dt = 330 cm^{-2}s^{-1}

The *Detector Data Link* has to meet all the requirements concerning lifespan and reliability i.e. low error rate and effective error detection. Therefore, it was inevitable to investigate the radiation tolerance of the components beforehand.

II. RADTOL MEASUREMENTS

The radiation tolerance tests of the DDL SIU card concentrated on the investigation of the Total Ionising Dose (TID) effects and of the so-called Single Event Effects (SEE) in the semiconductor components of the SIU cards. For practical reasons the irradiation time in the tests were between 20 min and 1 hour. Since we wanted to determine the effects of 10 years of irradiation (i.e. the life time of the experiment), we had to apply much higher dose rates and fluxes than it would happen in the real life. This may influence the results to some extent.

The TID measurements were carried out by means of γ-irradiation using a γ-decaying point source (^{60}Co). Under this geometry the dose rate is inversely proportional to the distance from the source, thus, the dose rate can be changed easily by moving the sample/target from or towards the source. Assuming that the dose rate does not vary much in time during the measurement, one can easily calculate the applied dose. The γ-irradiation tests were performed in the Institute of Nuclear Research (ATOMKI) of the Hungarian Academy of Science, in Debrecen, Hungary.

In order to measure SEEs, the components were exposed to high-energy proton and neutron irradiation. These measurements were carried out at ATOMKI with 1-14 MeV neutrons and at TSL (Uppsala, Sweden) with 50, 100, and 180 MeV protons.

During the last years the following possible SIU card components were investigated and tested in terms of radiation tolerance.

A. Clock Oscillators and Voltage Regulators

The signal quality of crystal clock oscillators largely affects the quality of the high speed serial data transmission in the DDL links. The frequency and jitter of four different clock oscillators (Pletronics PL75108A, Saronix SDB0149N, CFP IQXO-71C, Ecliptek PLE5144A) were measured while the waveforms of the signals were being monitored. In case of all the oscillators neither frequency change nor increase of jitter has been observed during neutron and gamma irradiation, no phase jumps were observed, and only negligible changes of the signal waveforms have been noticed after gamma irradiation up to 100 krad. We found that, concerning radiation tolerance, any of these four oscillators can be used on the SIU card.

Low drop-out linear voltage regulators produce the required supply voltages (1.8V, 2.5V) on the DDL cards. The low noise and output stability of these regulators are important for the proper operation of the entire circuit. We performed some basic tests on two different type of linear regulators, namely on the 1.8V and 2.5V members of the Linear Technology LT1963 and the Micrel 5209 families. The output voltage, latch-ups, and output noise were measured at static load while irradiated. We found that the LT1963 ones passed the tests and did not show degradation, while the Micrel ones failed these tests. They produced extra noise while irradiated with neutrons. Even worse, that their output voltage shifted out of the specification and this proved to be a permanent degradation. We chose LT 1963 to be used in the SIU design.

B. *Electrical Transceivers (SerDes) and Optical Transceivers*

During the last years we tested the following components at ATOMKI and TSL. Electrical transceivers (i.e. serializer/deserializer chips): Vitesse VSC7211 and Texas Instruments TLK2501. Small Form Factor (SFF, SFP) optical transceiver (OT) modules: Agilent HFBR5910E, HFBR5921L, HFBR5720L, Infineon V23818-K305-L57, V23818-N305-B57, partly as individual components, partly as parts of a more complex design.

We can summarize the results of these tests as follows. None of these components show TID effects irradiated with the gamma source or with protons. The electrical transceivers were exposed to an ionizing dose of 40 krad, at least; the optical transceivers were exposed to 10-30 krad.

Tested with neutrons of 1-14 MeV at ATOMKI, the electrical transceivers did not produce any malfunction while irradiated with 10^{12} n/cm^2. In the same test setup the optical transceivers tested show ~10 data transmission errors while irradiated with 10^{12} n/cm^2. These symbol errors will be detected by the 8B/10B coding scheme and the CRC of the data frames and do not add much to the expected Bit Error Rate (BER) of these components. (The specified BER of these optical transceivers *without* irradiation is < 10^{-12}.)

C. *FPGA Tests*

The goal of these measurements was to determine the SEU cross sections of the FPGA device used on the SIU card. Before the radiation tolerance tests we considered the ALTERA *APEX 20KE* FPGA as the baseline solution to implement the logic of the DDL SIU card. This is the device with which we build the prototype cards that have been tested and work very well in laboratory environment. However we considered the use of other FPGAs depending on the results of the radiation tolerance measurements. *Figure 1* shows the current architecture of the prototype SIU card.

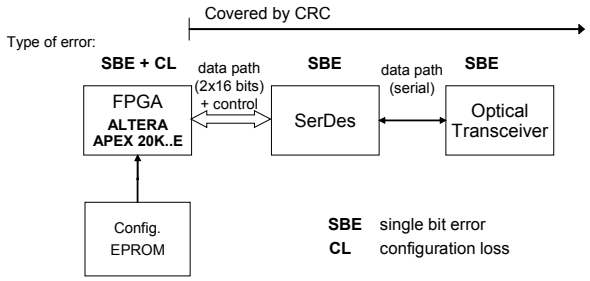

Figure 1 The block diagram of the current SIU card

Two different types of "memory cells" can be found in the FPGAs: those that store the device configuration and those that serve as application memory. A SEU in the application memory causes bit-flips of the memory, however a SEU in the configuration memory causes the loss of configuration or at least a corrupted configuration (and operation) of the device.

Memory tests: In these tests all the application memories built up a single memory block (2048x16 bit) pre-loaded with a known data pattern. Then, this pattern was read out and transferred via the DDL to the PC where the data were compared with the result of the previous read-out.

Register test: In these tests a register pipe (128x16 bit). fed by an internal data generator was realised in the device. In order to maximize the resource (logic cell, LC) utilization in the FPGA, the length of the shift register was chosen carefully. The output data of the register pipe was transferred via the DDL to the PC where it was compared with the expected (original) pattern.

1) *High Energy Proton and Neutron Irradiation of* ALTERA EP20KE

During the tests the SIU card with the ALTERA FPGA was installed in the radiation area while the other end of the DDL link (that is a DIU and a PCI RORC card) was placed outside the room. The full setup is shown in *Figure 2*.

The high energy proton (180 and 100 MeV) irradiation tests were carried out at TSL *(*November, 2003*)* and the neutron irradiation measurements were done at ATOMKI (December, 2003).

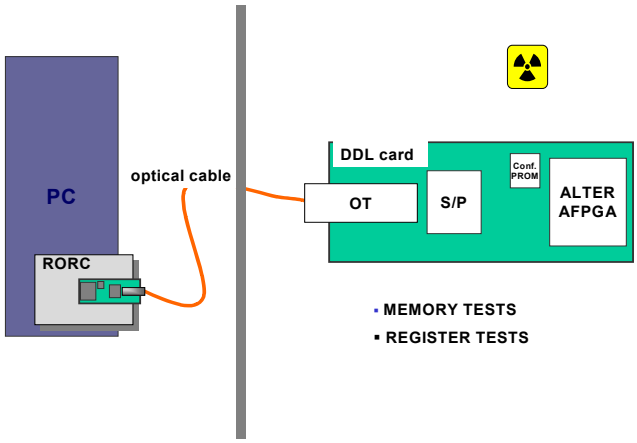

Figure 2 Test set-up for ALTERA tests using the SIU card

A computer program visualized the difference between the expected and than actually read out data patterns and calculated the total number of errors. Examples for the visualization of memory errors *(bit-flip)* and the so-called configuration loss errors (CL) are shown in *Figure 3*.

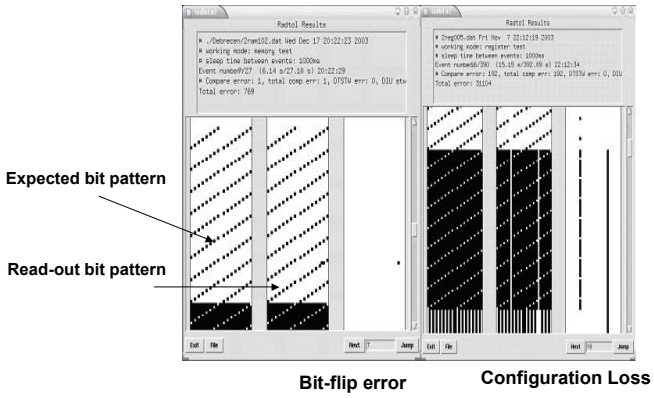

Figure 3 Examples of bit-flips error and configuration losses

The measured data and the calculated results are all shown in Table 2. Both the SEU and the CL cross sections for 5-14 MeV neutrons were one order of magnitude lower than for 100 and 180 MeV protons which may be explained with the different cross sections for nuclear reactions.

In spite of this difference, more SEU errors will be induced by neutrons than by protons because of the higher neutron fluence.

These radiation tolerance tests of the SIU card with ALTERA *EP20KE* FPGA have shown that the cross section for bit-flips in the application memory is acceptable, but the cross section for errors in the configuration memory is too high. This results in loss of the correct configuration of the device. Expectedly, during the run of the beam, in every hour, one of the 400 DDLs may loose its correct configuration. This can not be tolerated by the DAQ system.

D. Configuration EPROM Tests

On the SIU card an (E)EPROM stores the configuration data of the FPGA. At every power-on this configuration device initializes the FPGA. After every configuration loss or damage in the FPGA we had to perform a power off-on cycle to re-load the configuration to the FPGA from the EPROM. During the tests we found that the re-initialization of the FPGA is a safe and stable process and the content of the EPROM was not lost or damaged. (It is CRC checked during the initialization.) The configuration EPROM always got the same amount and rate of irradiation as the FPGA. This is not strange as the EPROMs are intrinsically much less sensitive to the radiation then the SRAM based FPGAs.

E. Alternative Solutions

After the results on the configuration loss of the ALTERA EP20KE SRAM based FPGA, we investigated other programmable devices to use in the SIU design. Fortunately, there are several alternatives, such as ALTERA Cyclone, XILINX Virtex II, or ACTEL ProASIC+ FPGAs.

The ALTERA *Cyclone* family has the same SRAM technology so very similar radiation tolerance results can be expected. However, this chip provides an internal automated configuration error detection mechanism based on CRC of the configuration. If the configuration changes by error the chip signals this to its environment. External control logic (e.g. a radiation tolerant EPROM based CPLD) can re-initialize the FPGA. Every configuration loss is detected, but the correction causes about 80 ms of lapse in the operation of the link card.

The *XILINX Virtex II* device family is also based on a similar SRAM technology, so similar frequency of configuration loss can be expected. This device provides such features as 'configuration read-back' and 'partial reconfiguration during operation' that support configuration error detection (with external logic) and configuration re-load in user mode (i.e. without stopping the normal operation of the device). Using these features, a continuous operation can be maintained, but, for the error detection, more logic has to be implemented in an external (radiation tolerant) device. Virtex II also supports radiation tolerant firmware design (e.g. Triple Redundancy Modules) at the expense of the use of much more logic resources. In this case a significantly bigger FPGA may be needed.

See *Figure 4* for the block diagrams of possible solutions with different SRAM based FPGAs.

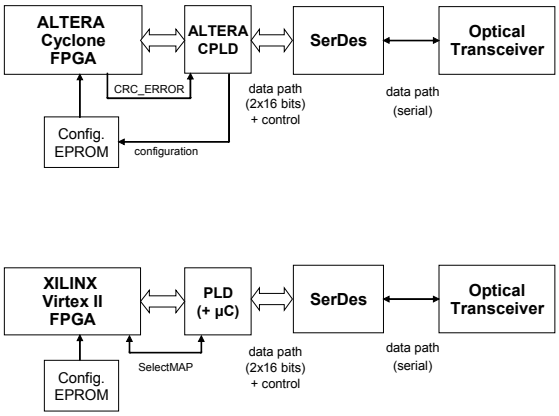

Figure 4 Possible solutions for radiation tolerant SIU using SRAM based FPGAs

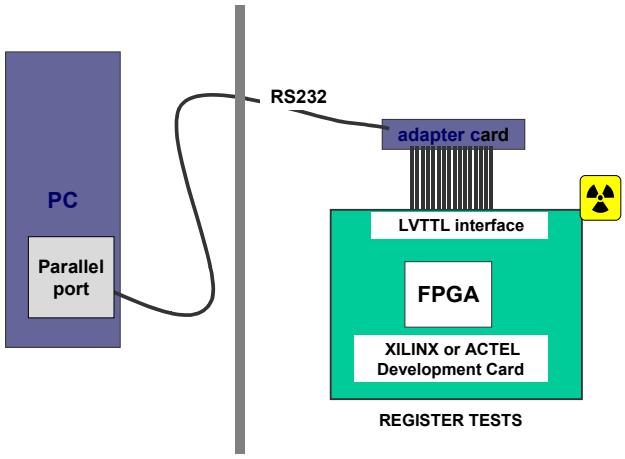

Figure 5 Test set-up for XILINX and ACTEL tests using development boards

Both solutions have advantages and disadvantages, but both need a more complex hardware and firmware design and additional logic chips on the board.

The third alternative is more promising as it does not want to patch the problem, but it wants to prevent it.

The *ACTEL ProASIC+* FPGAs are based on flash memory technology that is inherently much less sensitive to SEUs. Thus, these devices are expected to work without damages in configuration in the ALICE environment. It does not require external configuration EPROM, either. ProASIC+ devices are big enough to fit the entire SIU logic into them. However, it may be necessary to split the logic and implement the most speed critical part into a smaller external device to achieve the required speed of operation. (This device can be a radiation tolerant EPROM based CPLD, or a small flash based FPGA).

F. High Energy Proton Irradiation of XILINX Virtex II *and ACTEL* ProASIC+ *FPGAs*

Hence, we continued the irradiation tests on the XILINX Virtex II and ACTEL ProASIC+ FPGAs. The ALTERA Cyclone tests were skipped as we did not expected new results due to the same silicon technology.

The tests were carried out on standalone (XILINX Virtex II and ACTEL ProASIC+) FPGA test boards. In our setup the test boards had parallel cable interface to the test PC through an adapter card. The tests were very similar to the ones used for testing the ALTERA FPGAs on the SIU card. Actually only the register tests were repeated with 128x8-bit register pipes as we were interested only in the configuration errors. The tests were carried out on three energies (171 MeV, 94 MeV and 48 MeV). See *Figure 5*.

The ACTEL *ProASIC+* FPGA was also γ-irradiated with a dose rate of approximately 20krad/h with a ^{60}Co-source at ATOMKI, Debrecen. During the test, the waveform of the signal was being monitored on an oscilloscope.

According to the measurements, no problem occurred up to 10 krad. The ALICE requirement is 1.6 krad. At about 12 krad the device stopped working and could not be reconfigured. After one hour of annealing, it became totally recovered. We have to keep in mind that the dose rate in this measurement was 80 000 000 times the rate in ALICE.

All results of the measurements are presented in *Table 2*. Where both configuration and memory tests were made (i.e. the ALTERA chip) the upper lines shows cross section values for the configuration loss and the lower lines show the cross section of the memory errors. For the XILINX and ACTEL chips only configuration loss tests were done.

Table 2: Configuration loss results for the 3 types of FPGAs

Upper lines: σ (config. cell) [10-13 cm^2/LC] Lower lines: σ (memory cell) [10-14 cm^2/bit]	ALTERA APEX-E (0.18 µm CMOS) SRAM-based	XILINX Virtex II (0.15 µm CMOS) SRAM-based	ACTEL ProASIC+ (0.25 µm CMOS) Flash-based
5-14 MeV (n)	0.166 - 0.706 0.290 – 0.509		
48-50 MeV (p)		5.5 - 10.7 -	no config. loss -
94-100 MeV (p)	- 4.64-5.86	5.5 - 10.2 -	no config. loss -
171-180 MeV (p)	4.90 – 8.20 3.08 – 4.24	4.5 – 9.0 -	no config. loss -
TID			Temporary damage at 120 Gy
# of configuration loss in 10 years at one SIU	20 – 50 (n) 400 – 800 (p) - -	20 – 50 (n) 400 – 800 (p) - -	No configuration loss
# of link failures/hour in one of the 400 SIUs	~ 1 Not acceptable	~ 1 Recoverable	No link failure

Comparing the cross sections for the different FPGAs, one can see the ALTERA and XILINX have similar behaviour in radiation environment. The ACTEL FPGA did not show any degradation so it is a promising candidate for a SIU card working *without* configuration loss. However, it is a little bit slower than the ALTERA chip used on the prototype design that may cause difficulties in the logic design.

Figure 6 shows the proposed architecture of the radiation tolerant SIU card. A small or FPGA (e.g. CPLD will do the time critical calculations (mainly the CRC calculations).

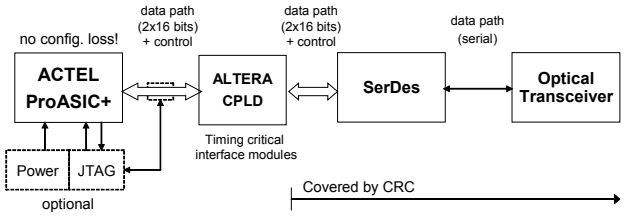

Figure 6 The block diagram of the radiation tolerant SIU

III. ACKNOWLEDGEMENT

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IV. REFERENCES

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