ALICE DDL Radiation Tolerance Test for FPGA Configuration Loss

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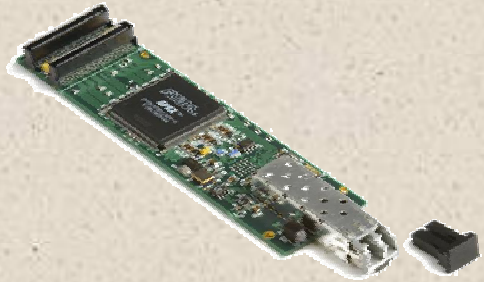
- **Collaboration between:**
  - * Research Institute for Particle and Nuclear Physics (KFKI-RMKI), Budapest
  - ** Institute of Nuclear Research (ATOMKI), Debrecen
  - *** Technical University of Budapest
  - **** Royal Institute of Technology, Stockholm
  - ***** CERN
- **Test facilities:**
  - – Debrecen, Hungary (gamma and neutrons 1 to 14 MeV)
  - – Uppsala, Sweden (protons 50, 180 MeV)
- **The main goal of the project:**
  to test COTS components that are going to be used for the ALICE Detector Data Link
- **http://cern.ch/ddl**

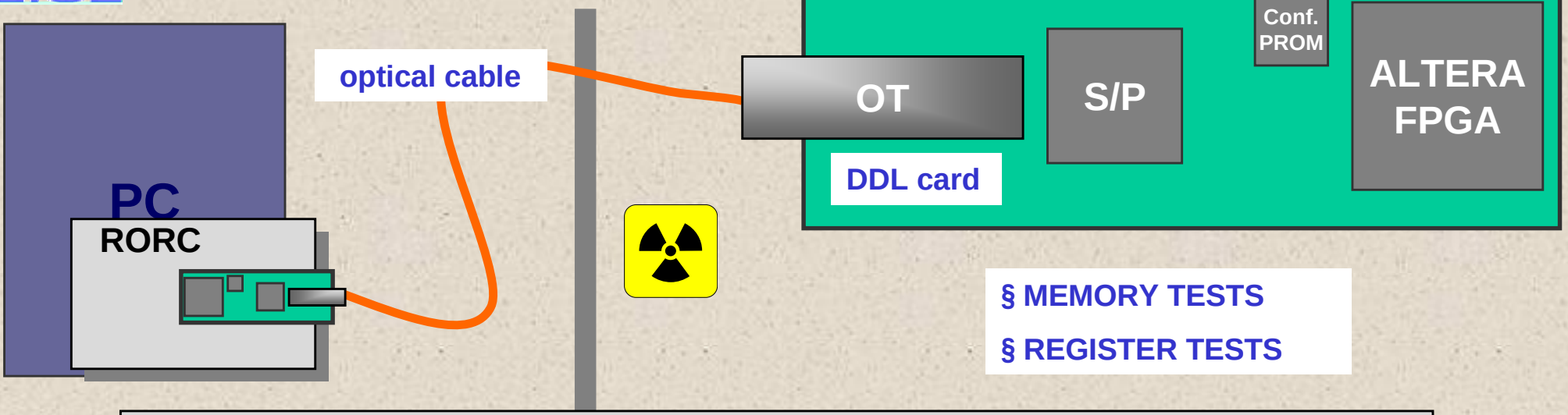
ALICE Detector Data Link (DDL)

- **High-speed (200 MB/s), duplex, point-to-point optical link**
- **Standard I/F between ALICE readout electronics and the DAQ**
- **Consist of**
  - **a Source Interface Unit (SIU)**
  - **an optical cable up to 300 m**
  - **a Destination Interface Unit (DIU)**

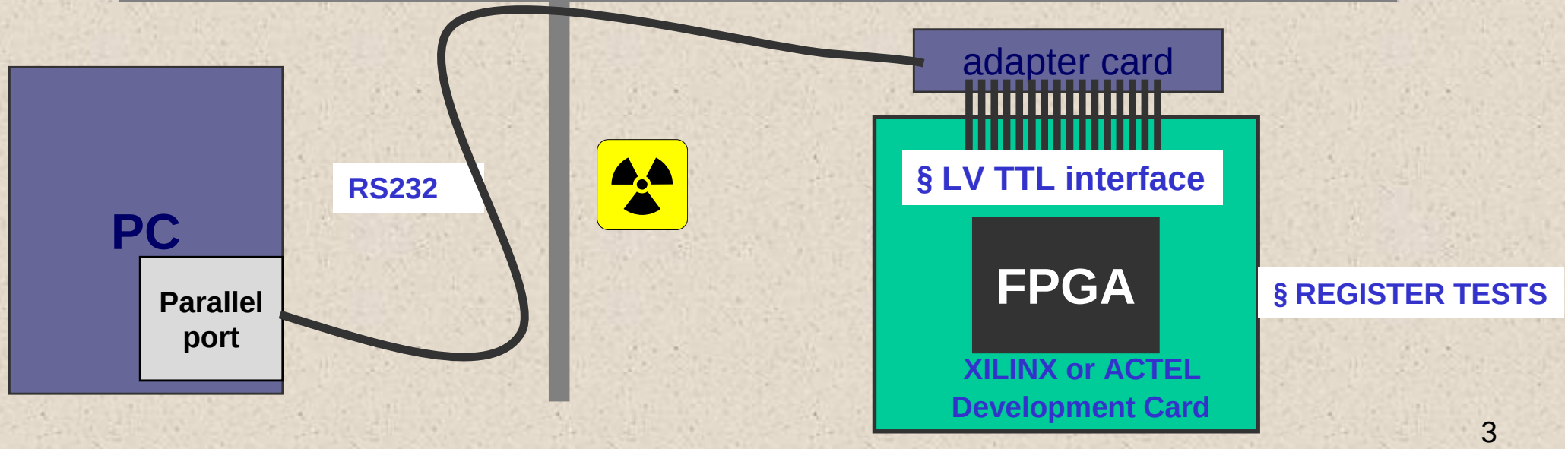


- **The SIU card works in radiation environment**
  - **Total ionizing dose: 16 Gy/10 years**
  - **Neutron fluence: 3.9×10^{11} n/cm^2 /10 years**
  - **Charged hadron fluence: 8.9×10^{11} n/cm^2 /10 years**
- **Focus on FPGA Configuration Loss**
- **FPGAs under test**
  - **ALTERA: APEX-E (EP20KE...) SRAM**
  - **XILINX: Virtex II SRAM**
  - **ACTEL: ProASIC+ FLASH !**

Test Setup - 1



Test Setup - 2



Test Firmware and Software

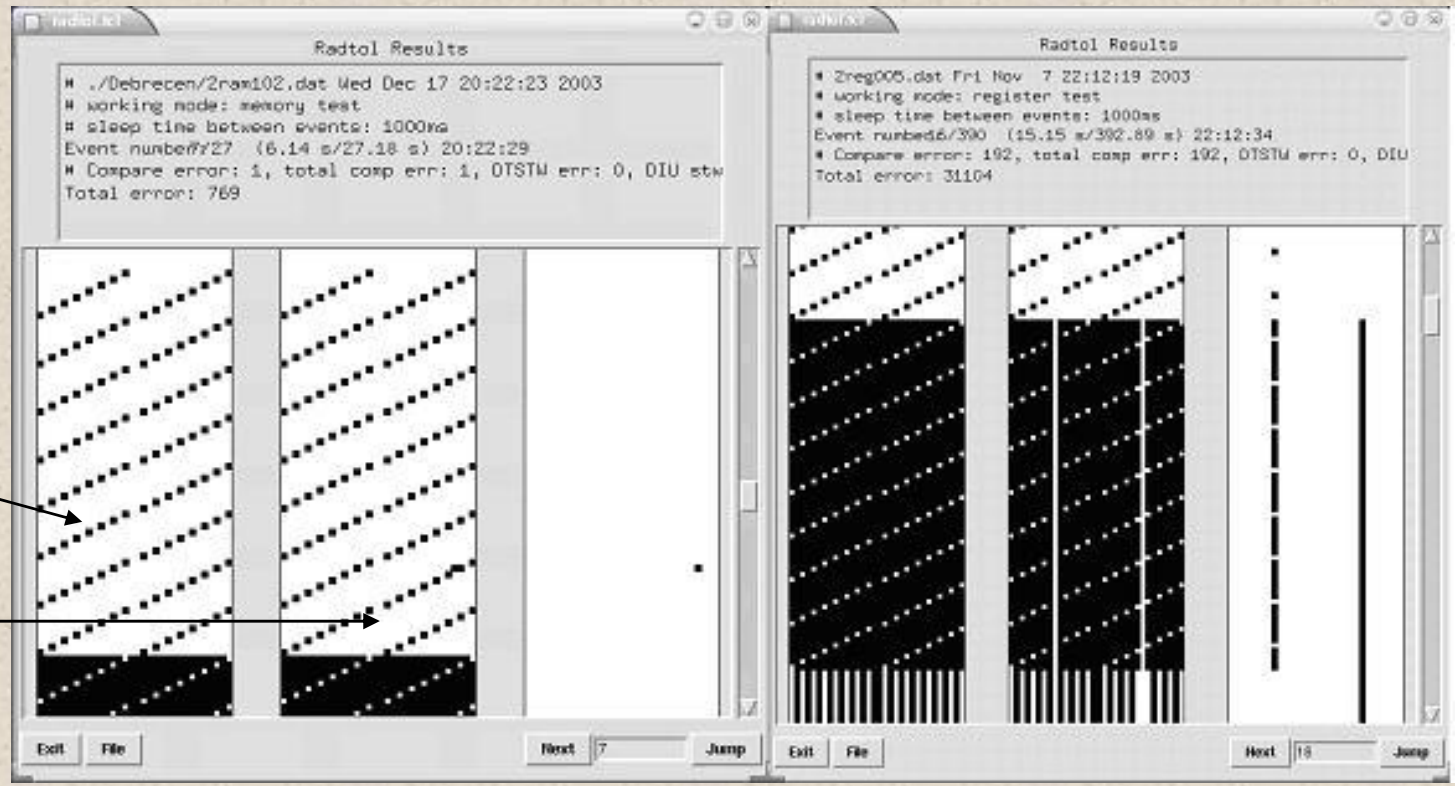
Tests: Register and RAM tests

– RAM test: FPGA internal memory cells filled with bit pattern (2048 x 16 bit).

– REGISTER test: long chain of shift registers (128 x 16 bit, 128 x 8 bit)

SW:

read and compare



Expected bit pattern

Read-out bit pattern

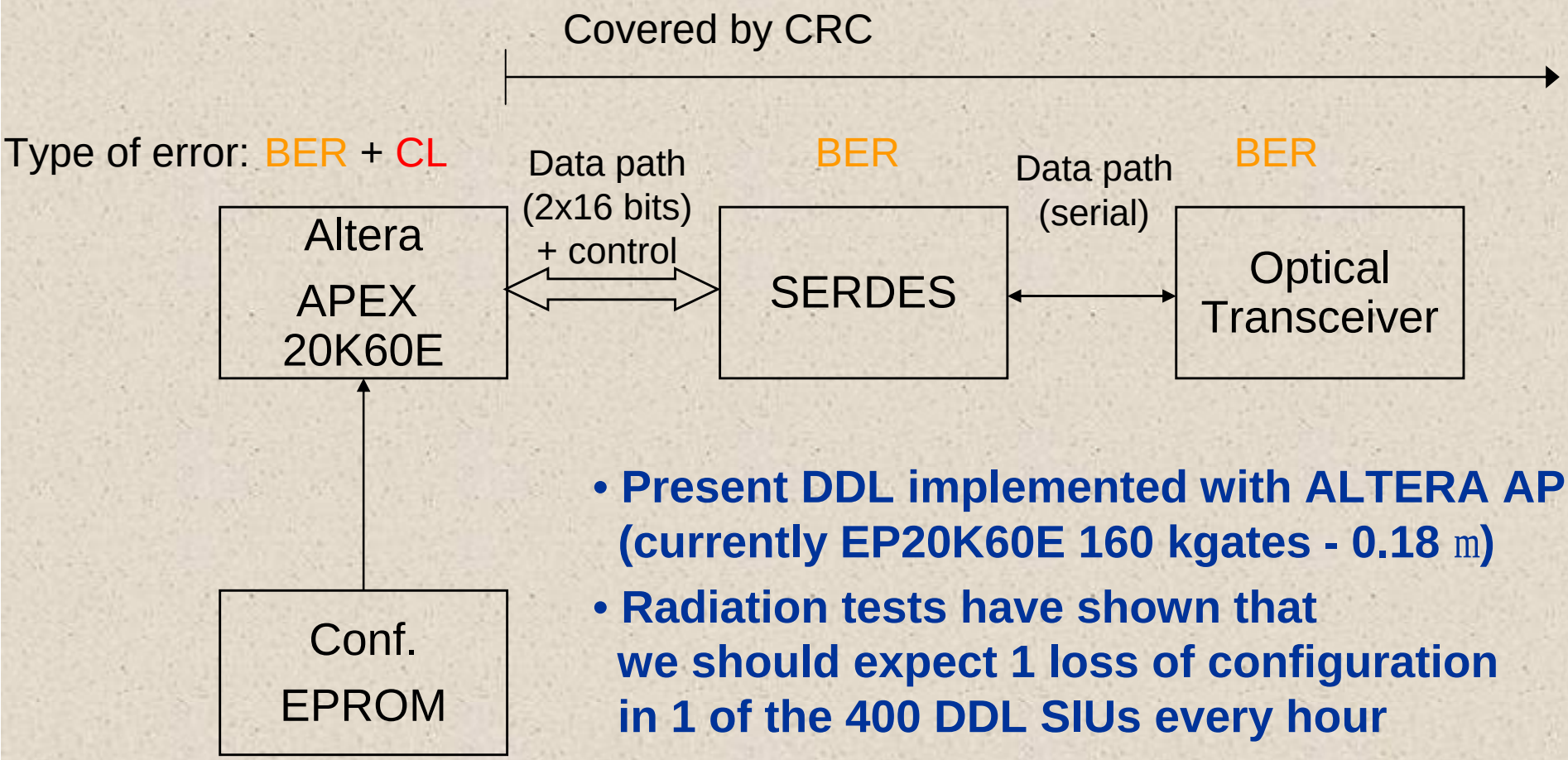
Bit-flip error

Configuration Loss

RadTol Project Results

$\sigma_{config\ cell}$ [10^{-13} cm^2/LC] $\sigma_{memory\ cell}$ [10^{-14} cm^2/bit]	ALTERA APEX-E (0.18 mm CMOS) SRAM-based	XILINX Virtex II (0.15 mm CMOS) SRAM-based	ACTEL ProASIC+ (0.25 mm CMOS) Flash-based
5-14 MeV (n)	0.166 - 0.706 0.290 – 0.509		
48-50 MeV (p)		5.5 - 10.7	< 0.71
94-100 MeV (p)	4.64-5.86	5.5 - 10.2	< 1.19
171-180 MeV (p)	4.90 – 8.20 3.08 – 4.24	4.5 – 9.0	< 2.03
TID			Temporary damage at 120 Gy (80 000 000 times the rate in ALICE!)
# of configuration loss in 10 years at one SIU	20 – 50 (n) 400 – 800 (p)	20 – 50 (n) 400 – 800 (p)	No configuration loss
# of link failures/hour in one of the 400 SIUs	~ 1 Not acceptable	~ 1 Recoverable	No link failure

Current DDL Design (ALTERA)



BER bit error rate

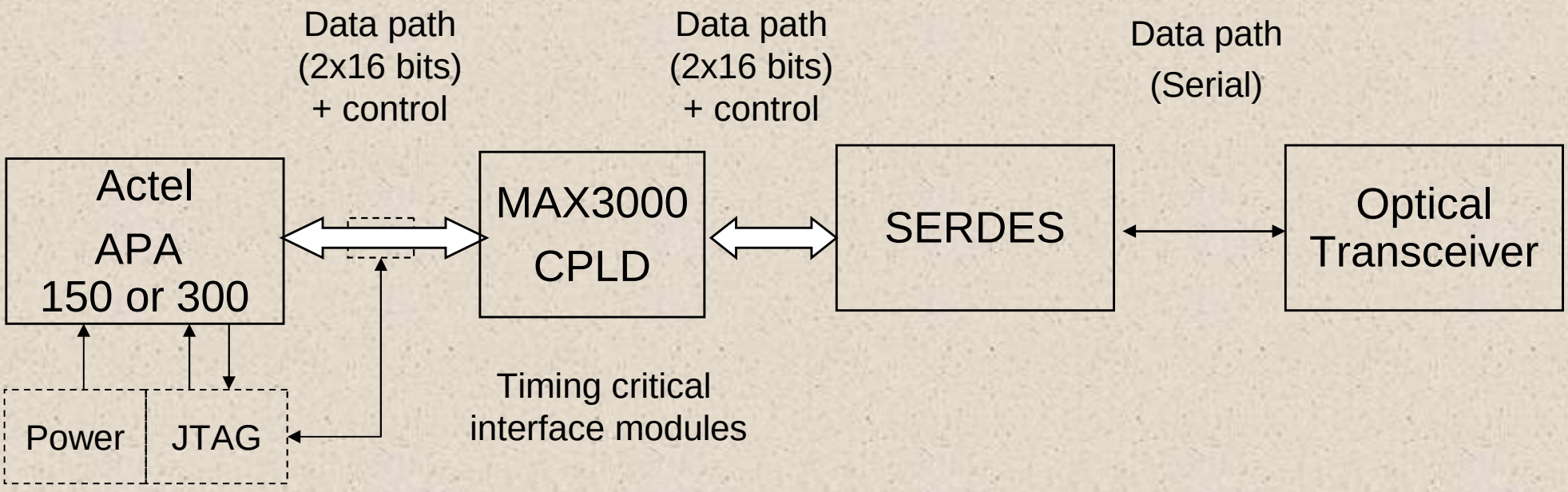
CL configuration loss

- **Present DDL implemented with ALTERA APEX-E (currently EP20K60E 160 kgates - 0.18 m)**
- **Radiation tests have shown that we should expect 1 loss of configuration in 1 of the 400 DDL SIUs every hour**
- **With the present design, some of these loss will not be detected**

Solution

Cure the problem in the implementation

- Use a flash-based FPGA (e.g. ACTEL)

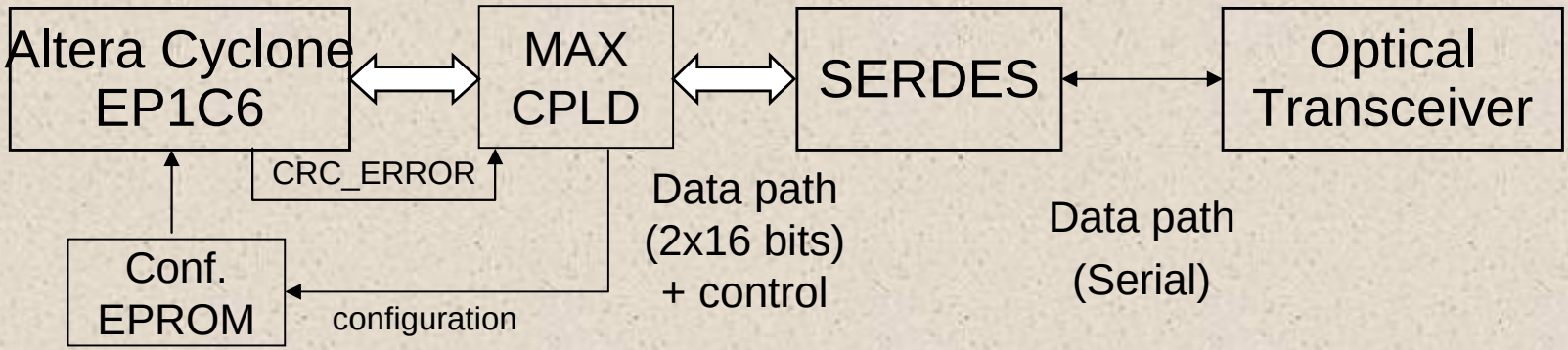


Note: device programming shouldn't be performed during beam activity (i.e. in radiation) to avoid SEL and SEGR

Possible Design with Cyclone or Virtex II

Detect and fix the problem

- **Use a SRAM-based FPGA signaling loss of configuration (ALTERA)**
  - No functionality during configuration



- **Use a SRAM-based FPGA allowing to check the configuration (XILINX)**
  - Configuration during user mode