Integration and test of the ALICE SPD readout chain

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Abstract

The silicon pixel detector (SPD) is the innermost element of the ALICE inner tracking system (ITS).

The on-detector electronic system consists of several ASICs in a commercial 0.25μm CMOS process (radiation-hardened by design), a low-mass multi layer Kapton cable for power and signal distribution (pixel bus), and a multi-chip module that includes a custom designed, very compact optical transceiver. The control and readout data transmission is done via optical fibres. Prototypes of the full read-out chain have been produced and tested. Integration issues and test results are presented and discussed.

I. System Overview

The SPD is organised as 2 barrel layers at radii of 3.9cm and 7.6cm from the beam axis, respectively. The basic unit of the SPD is called half-stave (Figure 1). The inner layer contains 40 half-staves while the outer layer contains 80 half-staves.

A half-stave consists of two ladders, glued and wire-bonded to the pixel bus, which at one end is connected to a multi chip module (MCM).

Each ladder consists of a silicon pixel sensor matrix of 160x256 cells bump bonded to 5 front end readout chips (pixel chips) with 32x256 channels each. The ladder has a sensitive area of 69.6mm x 12.8mm, the pixel cell size is 50μm (r ϕ) x 425μm (z).

The pixel bus is a custom developed, low-mass, multi-layer Kapton cable for power and signal distribution.

The MCM performs the functions of a) readout, multiplexing and serialization of the outgoing data, b) generation of the precision voltage references required by the pixel chips, and c) handling the timing and control signal communication with the DAQ module (Router) located in the control room. On receipt of an L2-accept trigger all the half-staves are read-out in parallel.

The 40MHz clock, the trigger and the configuration commands, are delivered to the MCM on two optical fibres. The outgoing data stream is transmitted to Link-Rx mezzanine cards on the Router via an optical fibre using a G-Link compatible, 800Mb/s communication protocol. Each Link-Rx card serves two half-staves. A zero suppression algorithm is implemented in FPGAs on the Link-Rx cards to reduce the data volume.

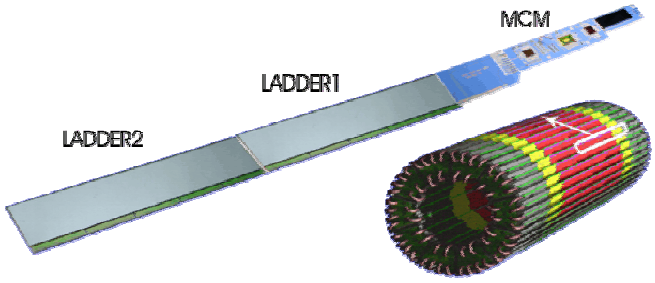

Figure 1: The SPD structure and a half-stave without pixel bus

The Router is a 9U VME module. Each Router contains 3 Link-Rx cards (figure 2).

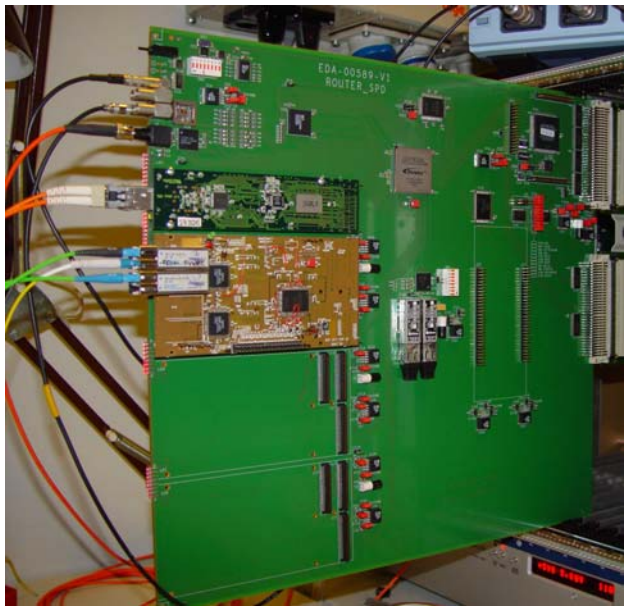

Figure 2: A Router board with a Link-Rx

The Router reads the zero suppressed data from the Link-Rx memories and transfers them to the ALICE DAQ via a Detector Data Link (DDL) [1]. The trigger commands from the ALICE TTC system [2] are broadcasted to the 3 Link-Rx cards. There will be 20 Routers in the ALICE control room for the readout and control of the 120 half-staves.

II. The MCM

The MCM (Figure 3) contains three radiation tolerant ASICs developed at CERN in a commercial 0.25µm CMOS process: the Digital Pilot, the AnaPil (Analog Pilot) and the GOL (Gigabit Optical Link). It also contains an optical transceiver from ST-microelectronics containing 2 pin diodes and a 1300nm laser diode. The optical module is a custom development with extremely tight space requirements. In particular, the height of the module is limited to 1.2mm. The optical components are pigtailed to single mode fibres.

Figure 3: The ALICE SPD MCM. From left to right the Analog Pilot, the Digital Pilot, the GOL and the optical package

The Digital Pilot [3] performs the readout of the 10 pixel chips and the formatting of the readout data. The Digital Pilot also broadcasts the clock to the other chips in the half-stave and controls them according to the commands received from the control room.

The Digital Pilot receives clock and slow control signals as current signals from the respective pin diodes by an integrated optical receiver amplifier, the Rx40 **[4].** For test purposes, LVDS input pads are also provided for the corresponding electrical signals.

The AnaPil provides the voltage references for the pixel chips and monitors voltages and temperatures on the half-stave. To perform its task it integrates six 8bit DACs and an analogue multiplexer followed by a 10bit ADC.

The GOL [6] receives the readout data from the Digital Pilot on a 40MHz, 16bit bus and serializes them in an 800Mb/s G-Link compatible stream. The laser driver is integrated in the GOL.

The high frequency clock needed for the transmission is synthesized inside the GOL from the 40MHz clock received from the Digital Pilot. The GOL for the locking of its internal PLL requires a maximum jitter peak to peak of 100ps [5].

The main challenge in the integration of this module is the density of components and interconnections. The available space for the active components is 45mm x 11mm. The standard FR4 process was found inadequate; ceramic prototypes were successfully developed, but the final implementation uses Kapton on account of lower cost and simpler production process.

III. MCM Test results and implemented improvement

To test and characterize the various elements of the SPD readout chain an FPGA based test board with a VME interface has been developed.

The test vectors have been studied with the aid of a Verilog based simulation of the full system comprising the test board.

The test board has connectors for a half stave, an MCM and a Link-Rx. Each component can be tested separately or as full chain. During the test of a specific element of the chain the other components are emulated by FPGAs on the test board. This leaves full control on all the inputs of the component under test.

The DAQ system of the test board can perform four different sequences of commands. Three of those are fixed while the fourth sequence can be programmed via software to address specific problems.

The test vector is sent in parallel to the device under test and to a model of it instantiated inside an FPGA. The response of the two is synchronised and compared. All the differences are stored in a log file with a time stamp.

A. Functional Test

The functionality of the system has been tested in a laboratory setup. The incoming signals to the MCM were test arrays of DAQ sequences at 3.6 kHz, 5 times the expected average trigger frequency for the SPD in ALICE. The occupancy of the events, coming from an FPGA simulating a half stave, was 50%, 25 times the expected occupancy in ALICE.

The MCM output data were monitored and any detected errors were reported in a log file with their time stamp. No missing data or errors of any kind were observed even throughout the longest test extending continuously over 12 hours.

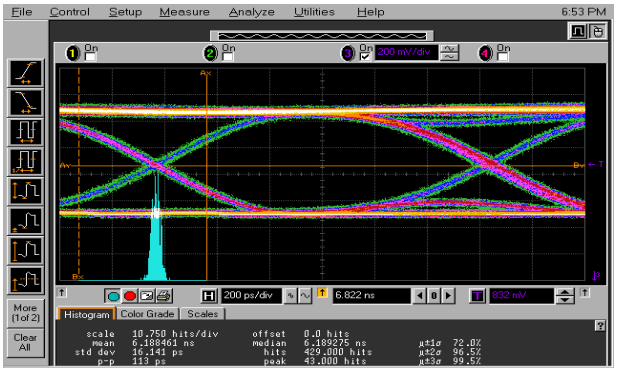

Figure 4: Eye pattern of the G-Link communication and jitter measurement ($\sigma_t \approx 16$ps)

The G-Link communication was evaluated using the eye diagram (Figure 4). The eye opening is 400μW for 400ps and the jitter is 16ps (standard deviation).

B. Optical Power Margins

The power budget of the optical link is affected by component ageing, number and quality of breakpoints, and possible degradation due to radiation effects. A certain level of optical power in excess of what would otherwise be adequate in an ideal system - the power margin - is required in order to assure full functionality over time and in all conditions. In the SPD we expect 1dB loss in all the 3 links due to the number of breakpoints required. A splitter in the G-Link communication will add a 3dB loss. Finally, we require 3dB of safety margin to compensate for possible loss of efficiency in the optical components (lasers, fibres and pin diodes) due to ageing and radiation effects. Summing up all the contributions the required margins are 4dB on the clock and slow control signals and 7dB on the G-Link communication (data readout).

With the MCM layout as shown in Figure 3, the measured margins were 1dB for the incoming links and 8dB for the G-Link communication. The system was functional, but missing the required additional 3dB of safety margin on the clock and slow control signals. The problem has been deeply investigated to find the reason and possible solutions.

The input current signals to the Digital Pilot were measured to be 350μA and the integrated amplifier itself had been tested with signals amplitudes down to 10μA. The origin of the reduced power safety factor was found to be a synchronous noise interference due to the excessive length of the signal lines.

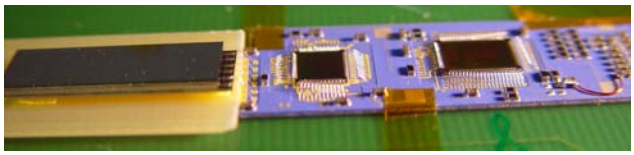

Figure 5: The optical Package, GOL and Digital Pilot positions in the MCM missing optical power margin

Two possible modifications to the MCM layout have been implemented to shorten those lines: (a) exchange the positions of the Digital Pilot and the GOL (MCM2), and (b) introduce an external amplifier (Rx40 stand alone version) in front of the other components using LVDS signals for the Digital Pilot inputs (MCM3)(Figure 6).

Figure 6: Part of an MCM with an external optical receiver. From Left to right: the optical package, the external Rx40, the GOL, the Digital Pilot

A test version of the optical input part of the MCM2 was obtained from an existing MCM. A full prototype of the MCM3 was already available and tested.

The optical power margin on the incoming links is 7dB in the two prototypes.

In the two modified layouts the line between the GOL and the laser is longer than in the previous layout. This might have degraded the G-Link communication; the amplitude of the clock driving the laser is ≈ 30x larger than the one provided by the pin diodes and its frequency is 20x higher.

In the MCM3 not only the margin on the G-Link communication remained 8dB, but the jitter on it went also down to 11ps due to the improved quality of the clock.

The same parameter will be measured for the MCM2 on a full prototype.

For an equivalent performance of MCM2 and MCM3, the preferred solution is MCM2 as it does not require the additional Rx40 chip.

C. Total Ionizing Dose Test

The total ionising dose (TID) in the inner layer of the SPD, integrated over 10 years of operation, is calculated to reach 250krad [7].

The Digital Pilot and the AnaPil have been irradiated to 1Mrad using 10keV X-rays. During the irradiation the chip functionality and the signal integrity of the chips were monitored.

The functionality of the Digital Pilot was not affected. A slight degradation in signal integrity was observed; it recovered after a few hours of annealing at room temperature.

The AnaPil was proven fully functional after the irradiation, but suffered of a shift in its bandgap voltage reference of 175mV after 500krad, bringing its output DACs out of the required precision and making the ADC measurement not reliable. The output of this element is available on a pad of the chip, making it possible to fix it to the required value using an external voltage divider. The AnaPil has been submitted to a different foundry (of the same company) because such sensitivity to radiation is suspected to be induced by the process. First tests on the new AnaPil chips seem to confirm this hypothesis: the shift is limited to less than 17mV after 500krad.

The GOL chip had already been qualified for radiation tolerance up to 10Mrad in a different test setup [8].

D. Single Event Upset Test

The integrated hadron flux in the inner layer of the SPD over 10 years operation is calculated to be ≈ $3.5 \times 10^{12}/cm^2$ (1MeV neutron equivalent) [7].

The Single Event Upset (SEU) test has been performed with a 58MeV proton beam. The integrated levels were: proton flux ≈ 3.5×10^{12}protons/cm^2 , TID ≈ 500krad.

During the irradiation the same electrical test patterns, consisting of $4x10^8$ readout sequences, were provided to the MCM and to its FPGA implementation on the test board in order to compare the two responses. All the errors in the readout data or in the feedback signals were recorded in a log file.

In the course of the test 4 errors were detected. They were identified as 1 bit flip in the readout data and 3 losses of synchronization in the GOL's PLL. The synchronization was found to recover within 12ms as expected from the GOL design. In the 12ms in which the G-Link was not available the Digital Pilot suspended the transfer.

The configuration registers of the 3 chips are protected against SEU using a triple modular redundancy. During the test the configuration registers of all the 3 chips were periodically checked. No change in the configuration was detected.

As a cross-check, no errors were observed when running the system continuously without irradiation over a period 4x longer than the one of the irradiation. This supports the interpretation that the errors detected during the irradiation test were effectively SEUs.

From this test the cross section for a SEU in the MCM is estimated at $\approx 1x10^{-8}cm^2$.

E. Full System Test in Test Beam 2003

A full prototype readout chain was used in the 2003 test beam with protons and with secondaries from indium ions on a lead target. A full half-stave was read out using an MCM. The data acquisition was performed using the Link-Rx connected to a Router prototype.

The control and data links proved their stability during the two weeks of the run, when 700MB of zero suppressed data have been acquired from the half stave.

IV. CONCLUSIONS

The functionality of the ALICE SPD readout chain has been validated in laboratory tests and in the 2003 beam test.

Improvements in the layout of the on-detector readout electronics (MCM) have increased the power margins on the clock and slow control optical signals to more than 7dB assuring reliable operation of the links in all conditions.

The power margin on the G-Link compatible optical communication at 800Mb/s is 8dB.

The MCM electronics has been tested to TID ≈ 1Mrad, well above the calculated level in the experiment, and has shown flawless performance.

The measured cross section for SEUs corresponds to an expectation of 4 SEUs per MCM in 10 years operation of the detector.

V. REFERENCES

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