CDF Level 2 Trigger Upgrade: The Pulsar Project

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(for the CDF Pulsar group)

10th Workshop on Electronics for LHC and Future Experiments

Pulsar web page:
http://hep.uchicago.edu/~thliu/projects/Pulsar/
CDF Detector

- Muon System
- Central Calor.
- Solenoid
- Fwd Calor.
- Plug Calor.
- Time-of-Flight
- Drift Chamber
- Silicon Microstrip Tracker

- New
- Old
- Partially New

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CDF Data Acquisition System

- **Level 1 trigger**
  - pipelined and “dead timeless”
  - fully synchronous
  - designed for 132ns operation
  - on L1A, write data to 1 of 4 local L2 buffers

- **Level 2 trigger**
  - asynchronous
  - L1 + supplemental info

- **Level 3 trigger**
  - full detector readout
  - PC farm runs reconstruction
  - output to mass storage
Technical requirement: need a FAST way to collect/process many inputs...

→ With the technology available back then (1990s), had to design custom (alpha) processor & backplane (magicbus) ...

→ had to deal with the fact that each data input was implemented in a different way ...

→ 9U VME crate with 6 different types of custom interface boards + custom processor & custom backplane ...
Each L2 input data path has been implemented differently:

<table>
<thead>
<tr>
<th>Silicon Vertex Trigger</th>
<th>Fast Track Trigger</th>
<th>Level1 Decision</th>
<th>Calorimeter Cluster &amp; Isolated Cluster Trigger</th>
<th>Muon Systems</th>
<th>Shower Max</th>
<th>Interface hardware</th>
<th>Input data clock</th>
<th>Data size range</th>
<th>Data length</th>
</tr>
</thead>
<tbody>
<tr>
<td>SVT</td>
<td>XTRP</td>
<td>L1</td>
<td>CList</td>
<td>ISO</td>
<td>Muon</td>
<td>LVDS cable (svt type)</td>
<td>30 MHz</td>
<td>117 bits/trk</td>
<td>Variable n svt-trks</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td>LVDS cable (svt type)</td>
<td>7.6 MHz</td>
<td>21 bits/trk</td>
<td>Variable n tracks</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td>LVDS cable (L1 type)</td>
<td>7.6 MHz</td>
<td>96 bits/evt</td>
<td>fixed</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td>optical fiber (hotlink)</td>
<td></td>
<td>optical fiber (hotlink)</td>
<td>20 MHz</td>
<td>46 bits/clu</td>
<td>Variable n cluster</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td>optical fiber (Taxi)</td>
<td></td>
<td>optical fibers (hotlink)</td>
<td>12 MHz</td>
<td>145 bits/clu</td>
<td>Variable n isoclue</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td>optical fibers (Taxi)</td>
<td>32 MHz</td>
<td>11k bits/evt</td>
<td>fixed</td>
</tr>
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<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td>Optical fibers (Taxi)</td>
<td>7.6 MHz</td>
<td>1.5k bits/evt</td>
<td>fixed</td>
</tr>
</tbody>
</table>

(This table just lists a few examples to give the flavor)
Requirements for a new L2 System

Base line performance of legacy L2 System (CDF RunIIa):
input rate to L2: 20 kHz, output rate to L3 300 Hz

Baseline for upgrade (RunIIb):
inst. Luminosity increase by factor ~3 \rightarrow increased occupancy
input rate to L2: 30 kHz, output rate to L3 300Hz to 1kHz

Goals for new Level2 system:
reduce execution time on L2
increase flexibility, reliability and testability
guarantee long term maintainability (end of CDF)
need to be compatible with all legacy input systems
Pulsar Approach:

- Built one universal interface board
- send all data to a commercial available CPU via a standardized link

**Pulsar** is designed to be:
Modular, universal & flexible, fully self-testable (board & system level)
Each board has ALL interfaces

L2 decision crate has

“Personality cards”

user defined interfaces

all interfaces: bi-directional (Tx & Rx)

“Personality cards”

Hotlink IO

Taxi IO

SVT/XTRP

Level 1

TS IO

S-LINK IO

“In God we trust, everything else we test”

**Pulsar**

Puser And Recorder

SRAMs (lookup Tables)

FPGAs (program-able logic)

VME CDFctrl

S-LINK

S-LINK

AUX

Spare lines

S-LINK to PCI

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Pulsar Design Methodology

A major fraction of the effort was dedicated to extensive design optimization & verification:

**Firmware:**
- Leonardo Spectrum: VHDL synthesis
- Altera Quartus II: place and route, FPGA level simulation

**Printed circuit board (PCB) design:**
- Mentor Graphics QuickSim: (multi)-board level simulation
- Interconnect Synthesis tool: trace & cross talk analysis
- IS_MultiBoard tool: signal integrity between motherboard & mezz cards

Design work done mostly by Fermilab Physicist/student & Univ. of Chicago engineer
Example: Multi-board (9 boards) simulation (from input connector pins to output connector pins)

It took 1.5 GB memory on a 2GHz/2GB modern PC to simulate 9 boards together at the same time.
Pulsar Board

connectors for all LVDS interfaces of legacy input systems (Rx & Tx)

mezzanine card Connectors (optical fiber interfaces)

VME interface

FPGAs DataIO

SRAM (lookup)

FPGA Data merging & control

L1 decision & Tracks visible to all 3 FPGAs

Slink interface
Pulsar Design & Verifications: ~ 3 people in ~ 9 months

Benefits of Pulsar design methodology:
No blue wire on all prototypes
All prototypes became production boards

4 types of custom mezzanine cards (Tx/Rx)

Design & Verifications: ~ 3 people in ~ 9 months

Initial checkout ALL interfaces: ~ 2 people in ~ 1 month

AUX Card
CERN SLink

works up to 100 MHz

TAXI
HOTLINK
Pulsar
1st Application

L2 Muon Interface Board for CDF IIa
The Challenge:

• The CDF management requested to evaluate the application of a Pulsar board as an muon interface board for the current (RunIIa) system

• Due to Pulsar’s flexibility, this was possible …
• Pulsar is self-testable, it was possible to do it fast
June 2003: CDF Ops ordered us to “jump”, we asked “how high?”

CDF Ops office: discussion in June 03 about L2 Pulsar muon Path for RunIIA

Pulsar RunIIA
Muon path:

From concept to error free path takes ~ 3 months
RunIIa L2 Muon path commissioning: Pulsar methodology at work

- Fully self-tested before put in the running exp. up to 1 Billions events in self-test mode.
- The FULL chain test with beam worked on the first try (error free)

We didn’t waste one second of beam time!
Successful application prototype & pre-production boards
Primary Application

CDF Level2 Trigger Upgrade
Level 2 Upgrade System configuration

Pulsar pre-processors

L1 Muon
L1 Tracks
L1 Trigger decision

L2 CALO (Cluster/ IsoCluster)
Energy Sums

SLINK

Muon

Cluster

Merger

SVT

Electron

LV2toTS

Linux PC

Trigger Supervisor

Phase I: single PC configuration
Phase II: dedicated PC for each L2 buffer

Strategy: Commission parasitically
→ need to split all input signals (fiber + LVDS)
A Parallel Universe for the Pulsar

- Tracks
- SVT
- 1/3 RECES
- CList
- ISOList
- L2 Muons
- SVT
- Muon
- Reces
- Cluster
- Legacy Level 2 Decision Crate
- α - Processor
- Optical LVDS Splitters

Fiber Splitter Lab
- Hotlink Rx
- Hotlink Tx
- Taxi Tx
- Taxi Rx
- Power meter
- splitters

LVDS Fanout board
New 32-bit SLINK to 64 bit PCI interface card: S32PCI64 → developed at CERN

• highly autonomous data reception
• 32-bit SLINK, 64-bit PCI bus
• 33MHz and 66 MHz PCI clock speed
• up to 520MByte/s raw bandwidth

ATLAS SLINK data format

- Beginning of Block control word
  - Start of Header Marker
  - Header Size
  - Format Version No.
  - Source Identifier
  - Level 1 ID
  - Bunch Crossing ID
  - Level 1 Trigger Type
  - Detector Event Type

- Data or Status elements
- Status or Data elements
- Number of status elements
- Number of data elements
- Data/Status First Flag
- End of Block control word

http://hsi.web.cern.ch/HSI/s-link/devices/s32pci64/
L2 Decision Processing Time Measurements

PC with 2.4GHz AMD Opteron (64bit) Processor fed by SLINK from Pulsar system

Level 2 Trigger algorithms run on real data in Run IIa system compared to Run IIb PC

Complete time including loading over S-Link/PCI and returning result <10µs
Test data taking with a subset of Triggers (using Muon, Track and displaced Vertex)

1) Legacy L2 making the decision
   Pulsar system running parasitically

2) Pulsar making the decision

Perfect match of trigger decisions
Of both systems before and after prescales
PULSAR System Timing Measurements

Pulsar pre-processors

L1 Muon
L1 Tracks
L1 Trigger decision
L2 CALO (Cluster/IsoCluster)
Energy Sums

Muon
Cluster
SVT
Electron

Merger
Merger inputs
SVT input

SVT L2toTS
L2toTS

Handshake with TSI & L1A→L2A/R

buffer specific counters on L1A
- current event
- previous event (unbiased)

Linux PC

Trigger Supervisor
System timing measurements

Overall L1A to L2 Decision latency

New system (not optimized) already as fast as CDF Legacy Level2

More detailed timing measurements
Provide guideline for optimization.

Pulsar upgrade <42 µs>

L2 Legacy <44 µs>

Tail due to Silicon Vertex Trigger processing time

Silicon Vertex Trigger
Silicon Vertex Trigger Upgrade

Goal: reduce SVT processing time
- reduce number of tracks to fit \(\rightarrow\) narrow roads
- reduce time spent on track fitting

- new road pattern memory boards
- replace 3 custom boards by Pulsar boards with memory mezzanine cards

Aim: complete upgrade by end of next year

First part, eliminating redundant tracks already implemented
Summary: CDF Level 2 Trigger Upgrade
The Pulsar Project

• **Uniform & modular & flexible**
  Lego-style, general purpose design, backward & forward compatible.
  Many applications within & outside CDF:
  Plan to replace/upgrade > 10 different types of CDF trigger board
  Compatible with S-LINK standard → commodity processors …

• **Design & verification methodology**
  simulation & simulation: single/multi-board/trace & cross talk analysis …
  → no single design or layout error (blue wire) on all prototypes

• **Testability & commissioning strategy**
  Board & system level self-testability fully integrated in the design,
  Suitable to develop and tune an upgrade system in stand-alone mode
  Minimize impact on running experiment during commissioning phase

• **Application of S-LINK at Hadron Collider**
  experience gained transferable to and from LHC community…

For more information see:
http://hep.uchicago.edu/~thliu/projects/Pulsar/