University of BRISTOL

CMS L1 Triggering at the SLHC

- What?
  - What is the SLHC?
  - What constraints?
- How?
  - Architecture
  - Technology

What are we talking about?

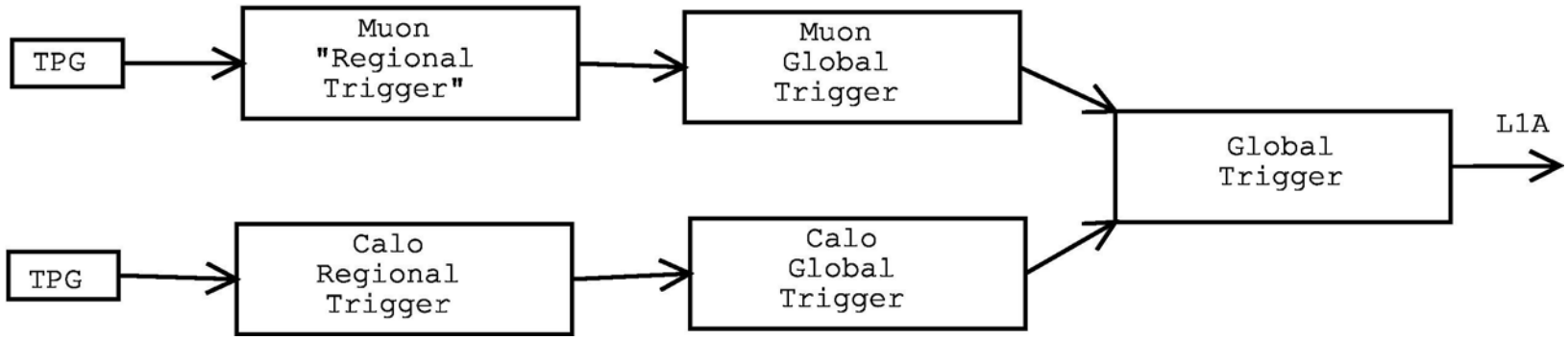
- Assume SLHC means:
  - $L = 10^{35} cm^{-2} s^{-1}$
  - 25ns BX
  - (~ 200 vertices per BX)
- Physics aims:
  - Discovery: e.g high p_t objects, large missing-E_t
  - Electroweak physics
    - Looking for W,Z,H products – sets thresholds

What constraints?

- Detector:
  - Tracker: complete redesign
  - Calorimeter: Detector and front-end unchanged
  - Muons: Minimum change on detector
- Latency (from BX to L1A at front end) 5μs max.
- L1A rate ~ 200kHz max (limited by ECAL VFE)

What does L1 do at the moment?

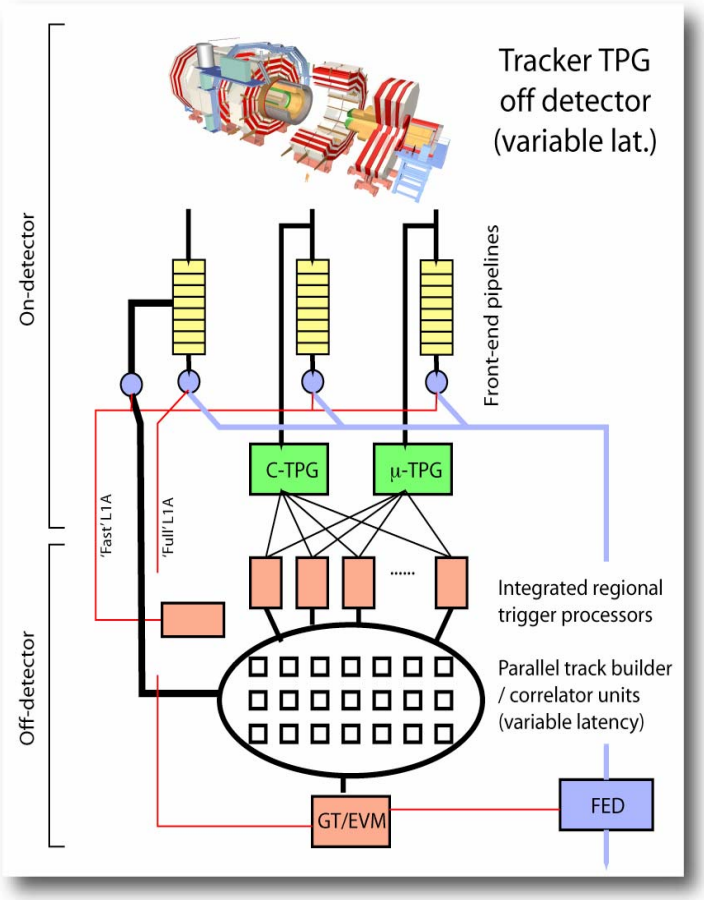
- CMS level-1 trigger system forms “trigger primitives” from Calorimeter and muon data.
- Muon/Calo trigger objects processed separately
- No tracking information.



What trigger approach?

- Want to match tracker and calo & muon information at "Level-1"
  - Electrons:
    - Single electrons: improve π^0 rejection
    - Di-electrons: identifying vertex gives x20 reduction in rate at SLHC (generator level)
  - Muons: BCID, p_t refinement
  - Jets/MET: Pile-up rejection from vertexing

How? (TPG off detector)



- Form a L1 decision from calo and muon. Run at 200kHz L1
  - Transfer data from latency buffers to event buffers on L1A
  - Readout a subset of tracker data on L1A
- Tracker 'TPG' off detector
- Correlate calo/muon/tracker to form "L1.5"
- Readout full tracker on L1.5A

How? (Fixed vs. variable latency)

- Once the data are transferred from latency buffers to event buffers requirement for a fixed latency trigger (and in-order L1A) is removed
- The processing needed to veto an event from the tracking data will vary from event to event.
- Minimize total processing power needed by having out of order L1.5 accepts.
- c.f. LHCb L1 track trigger (LHCB 2004-049-DAQ)

How? (Tracker TPG on detector)

- A more radical approach would be to form the tracker "trigger primitives" on the detector.
- Use free-space optics to pass data from layer to layer (?)
  - Can fan-out to neighbouring sensors
  - Different wavelength tx/rx to separate channels
- Less flexible than off-detector TPG
- More difficult to develop (?)
- Aim for fixed (low) latency. Include in L1 rather than create a L1.5 then ~200kHz limit no problem)

How? (Power Consumption)

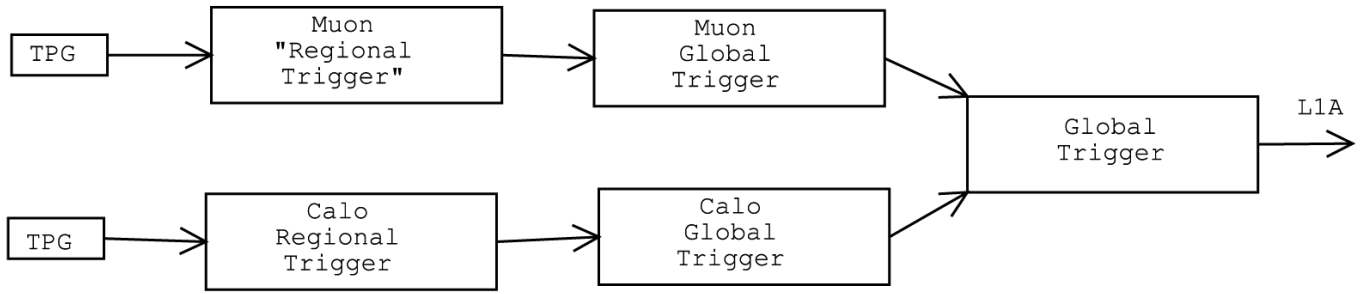
- A tracker with substantial processing is likely to dissipate substantial heat.
- Even shipping the data for every BX will burn power:
  - 3 charged tracks/cm^2 at r=10cm into 1cm-square pixel sensors (~ 4 Gbit /s)
  - gives ~ 75Tbit/s for 3 pixel layers.
  - Current gigabit serializers ~ 100mW/Gbit.s^{-1}
  - 7.5kW from serializers alone (cf. ~ 3kW from current pixel detector)

How? (simulation needed)

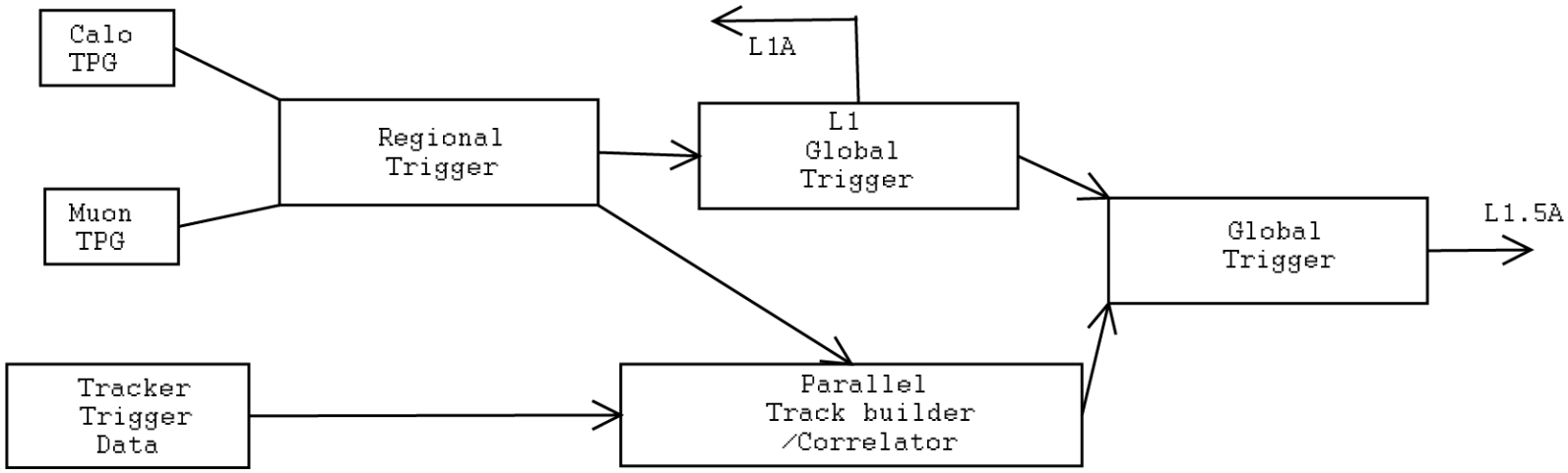
- Simulation work needed to determine the minimum volume of data required from tracker at L1 to correlate tracker to calo/muon information.
  - Have made a start at Bristol, but nothing that can be reported.

How? (Generic Trigger Modules)

- The concept of using a generic, reconfigurable processing module successful in GCT.
- Use common module for whole L1 trigger?

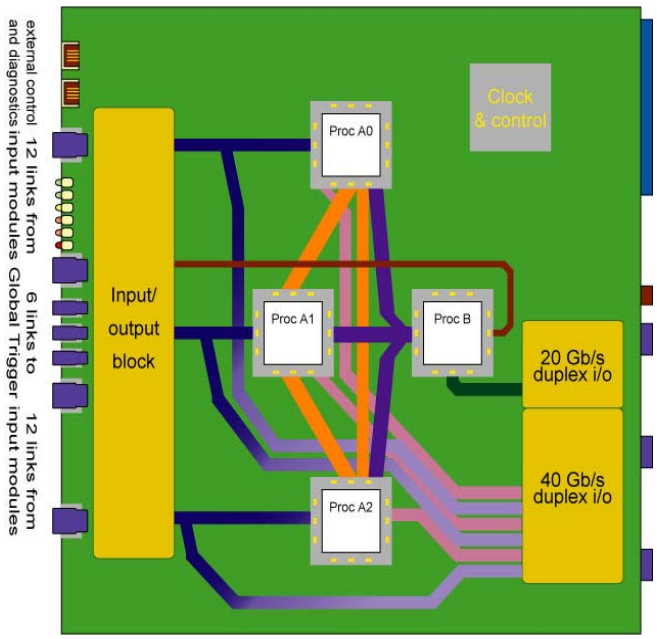


How? (Generic Trigger Modules)



- Have common regional trigger for Calo & Muons.
- Use same boards in global trigger (and track builder?)

How? (Extrapolate GCT TPM)

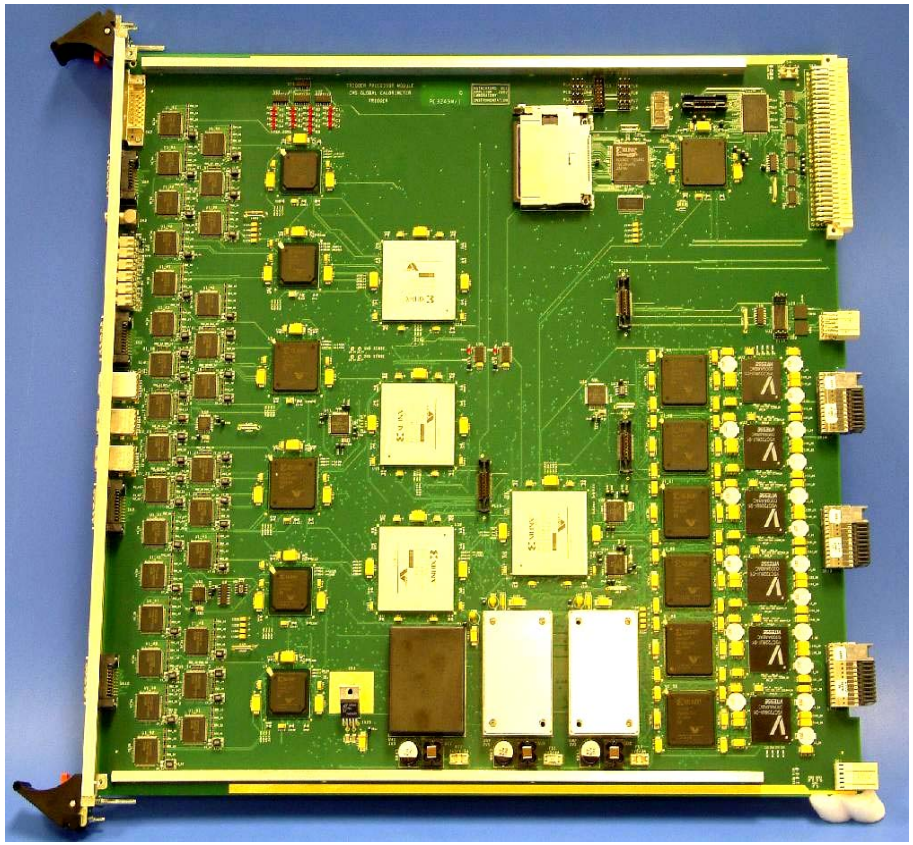


- Based on commercial components for processing and data transfer
- Four processing FPGAs, 3M gates, 14k logic cells
  - Pipelined logic and data transfers clocked at 160 MHz
- 1.44Gbit/s Front-panel I/O
  - 30 Gbit/s input data on 24 links
  - 7.5 Gbit/s output
- 3.2Gbit/s backplane
  - 60 Gbit/s in & out on 24+24 backplane links

Can we extend to a generic trigger processor for SLHC?

TPM design challenges

- Processing technology
  - Xilinx Virtex-II has been very successful
- High-speed data links
  - Serdes choice
  - Connectors and cables
  - Synchronisation
- System issues
  - Configuration
  - Control
  - Power distribution
- Firmware development and management



System Architecture

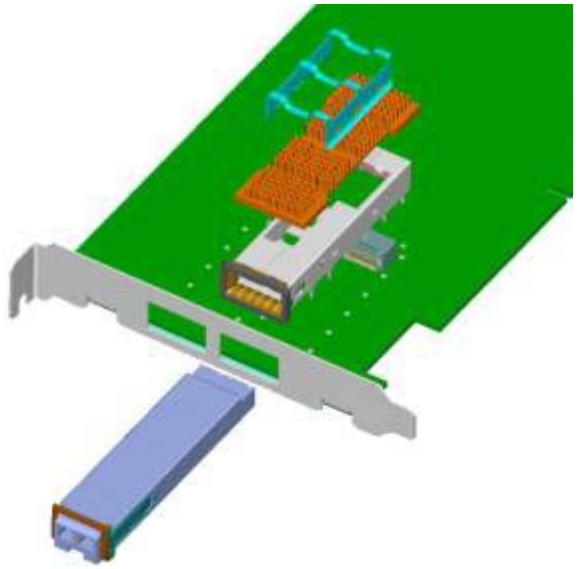
- GCT used a VME 9U based system:
  - Custom power
  - Custom J2/J3
- Move to a telecoms standard? E.g. Advanced TCA?
  - 8U boards
  - 6HP board pitch
  - Defined Gbit/s backplanes.

FPGA processing extrapolation

- Feature size
  - 150→90 nm
- Gate count
  - ×(150/90)²=2-3?
- I/O density
  - ×2-4 switching speed
  - Internal 10Gbit/s serdes (existing family has up to 20 per device)
  - 9.8Tbit/s with standard ATCA backplane.
- Optional embedded processors or DSP blocks.

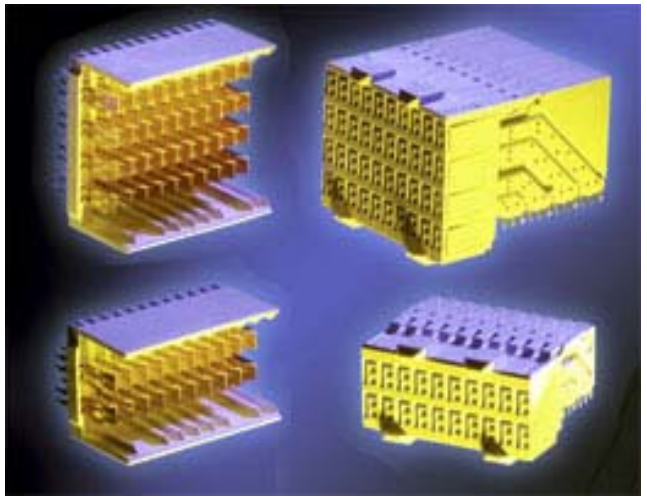
Front-Panel I/0 Extrapolation

- Use serdes inside processing devices
  - Increase density w.r.t discrete serdes
- Current TPM uses 1.44GBit/s per pair over Infiniband connectors.
- Use a pluggable system like XFP?
  - 10Gbit/s in 25mm front-panel space. (Can double sided)
  - Standard fitting on board
    - plug in copper module for up to 1.5m
    - Fibre for inter-crate.
    - Up to 120 Gbit/s on front-panel (240Gbit/s double-sided)



Backplane I/O Extrapolation

- Currently 3.2Gbit/s per pair over Teradyne VHDM-HSD connectors. (Probably good to ~ 6Gbit/s)
- 10Gbit/s per pair over backplane with Tyco ZPack HM-ZD connectors. Up to 2Tbit/s per board
  - (c.f. Xilinx demo at SuperComm '04)
  - 9.8 Tbit/s on standard backplane. 16Tbit/s possible with custom backplane



TPM Summary

- System Platform: VME -> AdvancedTCA
- Serial I/O: 1.44GBit/s / 3.2Gbit/s -> 10Gbit/s
  - I/O per board: 9Gbit/s -> 2TBit/s
- Bus speed: 160Mbit/s.line -> 640Mbit/s.line
  - Number of high-speed lines – try not to increase to much (already 3000)
  - Clocking: system-synchronous -> source-synchronous?

Design Methodology?

- It would be **much** more efficient to have a few, related, designs for trigger processing modules than many custom designs.
  - Reduces cost of manufacture
  - Reduces problems of maintenance & spares
- Need to find a way to work collaboratively on a single module?
  - Increase effort available for thinking / design / prototyping / testing
  - More likely to get a module that works for everybody.
  - Maintain distributed design expertise rather than concentrate at "the centre".

Summary

- Have presented a "straw man" L1 trigger for the SLHC
  - Focus on architecture and off detector implementation.
- Tracker on-detector electronics is a substantial challenge.
  - Dead material (e.g. fibres)
  - Power consumption
- Need careful examination of architecture choices
  - Tracker "TPG" on or off detector?
  - Smallest subset useful for triggering?
- A tracking-trigger couples design of tracker & trigger
- Suggest constructing trigger from generic processing modules.