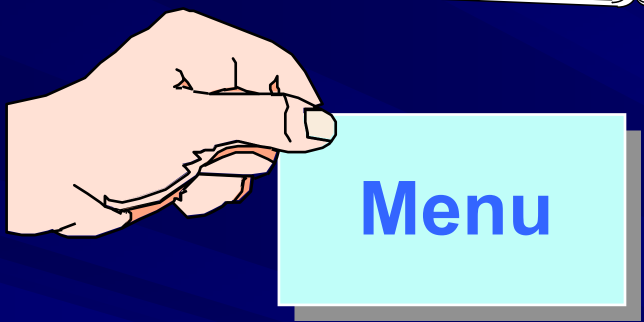
# Electronics Issues & challenges for future linear colliders




*By P. Le Dû*

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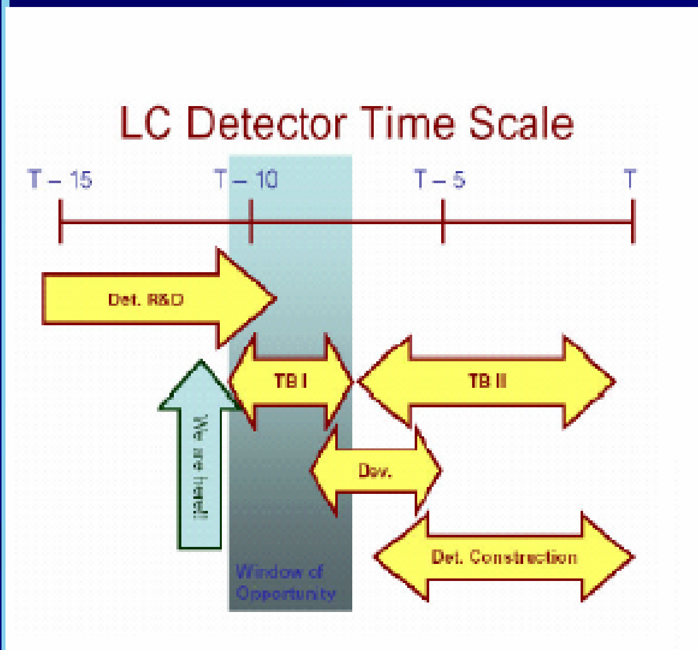
- Basic parameters and constraints
- Detector concepts
- Front end electronics and read out issues
- Data collection architecture model
- Software trigger

# Goals of this presentation

- Brief overview of the Read-out issues and directions for the next HEP facility : the ILC → International Linear Collider

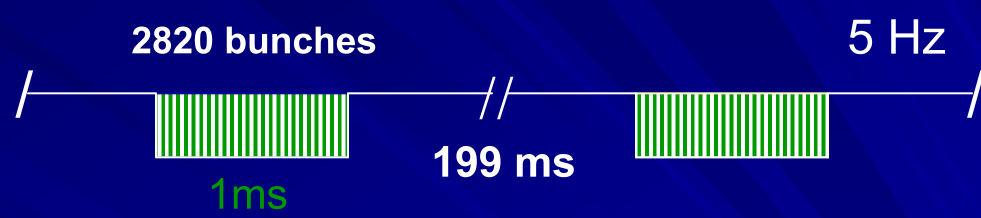




- 2005 → R&D
- 2007 → technology choice
- 2009 → begin construction
- 2015 → detector ready

# Conditions

***Recent International decision: « cold » machine ' à la Tesla'***




*Machine parameters*

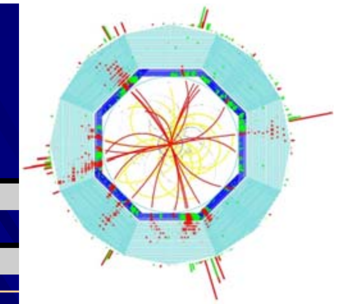
*The LC is a pulsed machine*

- 2 x 16 km superconducting Linear independant accelerators
- 2 interaction points
→ 2 detectors
- Energy
  - nominale : 500 Gev
  - maximum : 1 Tev
- IP beam size ~ 1 µm

| | |
|---|---|
| repetition rate | 5 |
| bunches per train | 2820 |
| bunch separation | 337 ns |
| train length | 950 ns |
| train separation | 199 ms |

*-> long time between trains*
*(short between pulses)*

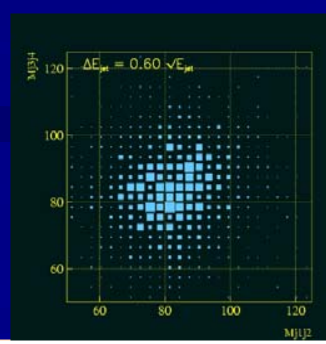
# ILC vs LEP/SLD



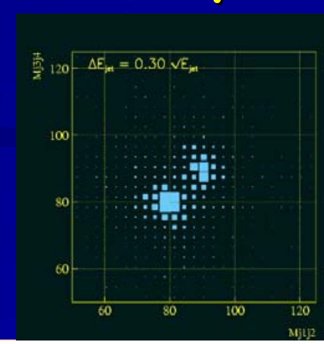
- Jets & leptons are the fundamental quanta at theILC. They must be identified & measured well enough to discriminate between Z's, W's, H's, Top, and new states. **This requires improving jet resolution by a factor of two. Not trivial!**
- Charged Particle tracking must precisely measure 500 GeV/c (5 x LEP!) leptons for Higgs recoil studies. …. **This requires 10 x better momentum resolution than LEP/SLC detectors and 1/3 better on the Impact Paramater of SLD!**
- To catch multi-jet final states (e.g. t tbar H has 8 jets), need real 4π solid angle coverage with full detector capability. **Never been done such hermiticity & granularity!**

*LEP-like resolution*

$60\%\sqrt{E}$



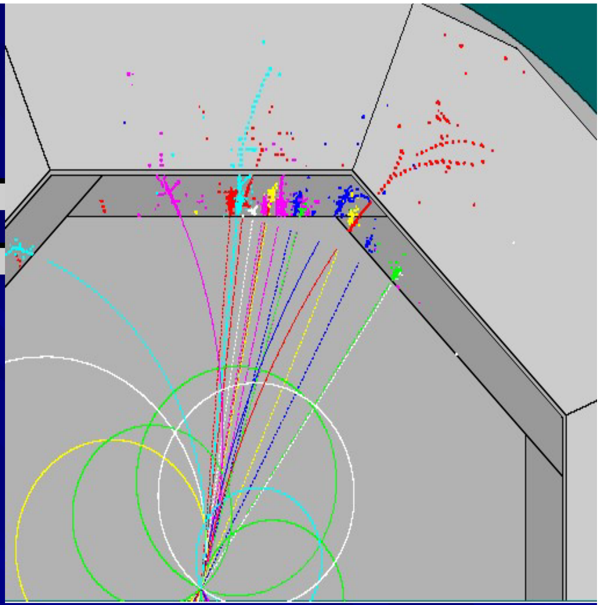

**2 Jets separation**




*ILC goal*

$30\%\sqrt{E}$

# ILC vs LHC

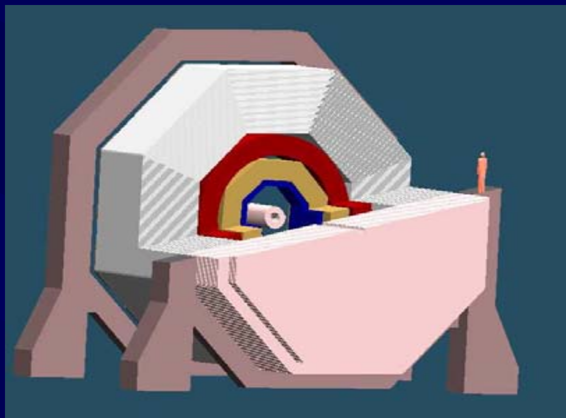


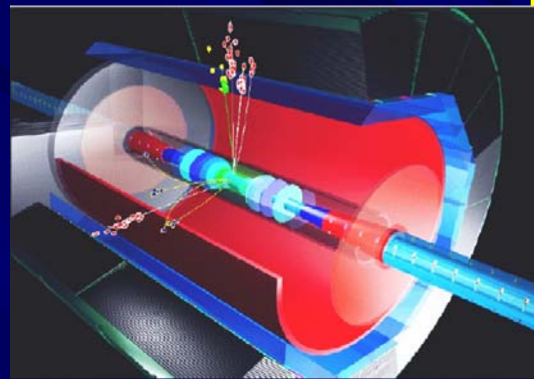
- **Less demanding …..**
  LC Detector doesn't have to cope with multiple minimum bias events per crossing,
  high rate triggering for needles in haystacks,
  radiation hardness…
  → hence many more technologies available, better performance is possible.

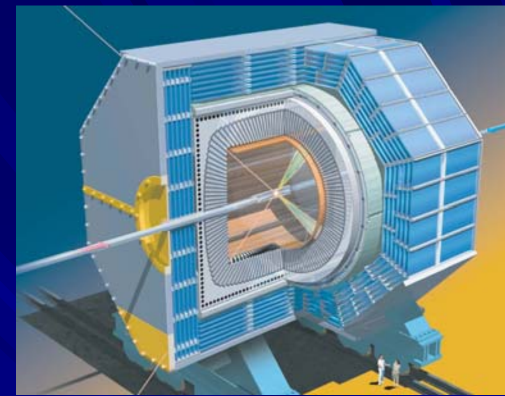
- **BUT →** LC Detector does have to cover full solid angle, record all the available CM energy, measure jets and charged tracks with unparalleled precision, measure beam energy and energy spread, differential luminosity, and polarization, and tag all vertices,…
  → hence better performance needed, more technology development needed.

- **Complementarity with LHC → discovery vs precison**
  The 'Particle flow' paradigm in calorimeters !
  → LC should strive to do physics with *all* final states.
  Charged particles in jets more precisely measured in tracker
  Good separation of charged and neutral

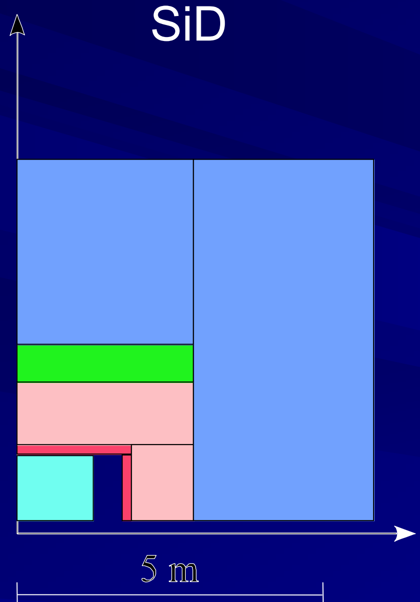
# Detector concepts



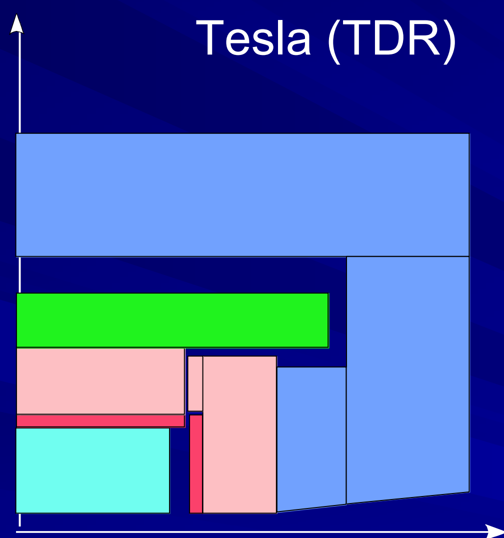




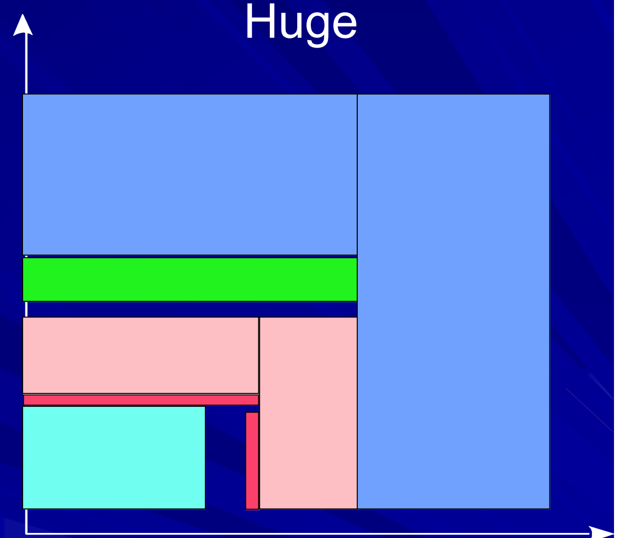
SiD




Tesla (TDR)



Huge




- Si Strips
- SiW EM
- 5 Tesla

- Large gaseous central tracking device (TPC)
- High granularity calorimeters
- High precision microvertex
- All inside 4T magnetic field

- Large Gazeous Tracker → JET,TPC
- W/Scint EM calor.
- 3 Teslas solenoid

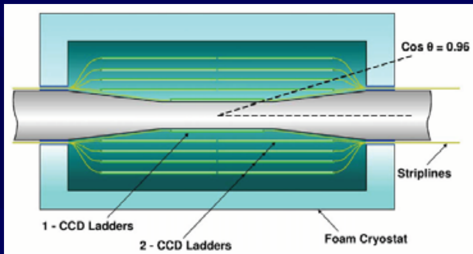
# Evolution of basic parameters

| Exp. *Year* | Collision rate | Channel count | L1A rate | Event building | Processing. Power | Sociology |
|---|---|---|---|---|---|---|
| UA's *1980* | 3 μsec | - | - | - | 5-10 MIPS | 150-200 |
| LEP *1989* | 10-20 μsec | 250 - 500K | - | 10 Mbit/sec | 100 MIPS | 300-500 |
| BaBar *1999* | 4 ns | 150K | 2 KHz | 400 Mbit/s | 1000 MIPS | 400 |
| Tevatron *2002* | 396 ns | ~ 800 K | 10 - 50 KHz | 4-10 Gbit/sec | $5.10^4$ MIPS | 500 |
| LHC *2007* | 25 ns | 200 M* | 100 KHz | 20-500 Gbit/s | $>10^6$ MIPS | 2000 |
| ILC *2015 ?* | 330 ns | 900 M* | 3 KHz | 10 Gbit/s | $\sim10^5$ MIPS | > 2000 ? |

** including pixels*

| Sub-Detector | LHC | ILC |
|---|---|---|
| Pixel | 150 M | 800 M |
| Microstrips | ~ 10 M | 30 M |
| Fine grain trackers | ~ 400 K | 1,5 M |
| Calorimeters | 200 K | 30 M |
| Muon | ~1 M | |

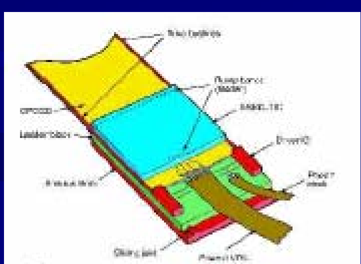
# Vertex technologies




## CCD

*(C. Dammerell & al.)*

- SLD/VXD3 experience, but needs faster readout and rad hard design.
- Column-parallel CCD with low noise, very low driving Voltage and 50 MHz ASIC.
- Read Out 20 time per BunchTrain (50 µs)
- RO Full detector → 2 x 1GByte fiber

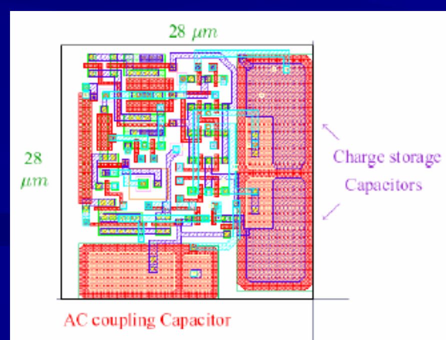


## CMOS

**(Monolhitic Active Pixel Sensor)**

*(IRES Strasbourg)*

- Concept from visible light imagers
- fast readout and on-chip integration of functionalities 20x20 µm cell CMOS sensor
- neutron fluxes 100 times larger than expected at LC,
- gives 2 µm resolution in beam tests
- thinned down to 120 µm.
- Adopted for STAR VTX upgrade at RHIC




Mimosa 6

## DEPFET …..etc

*(Bonn,MPI)*

- FET-Transistor integrated in every pixel (first amplification)
- No charge transfer
- Very limited power consumption (~ 5W for the full VD)
- Low noise allows 50 µm thinned down sensors

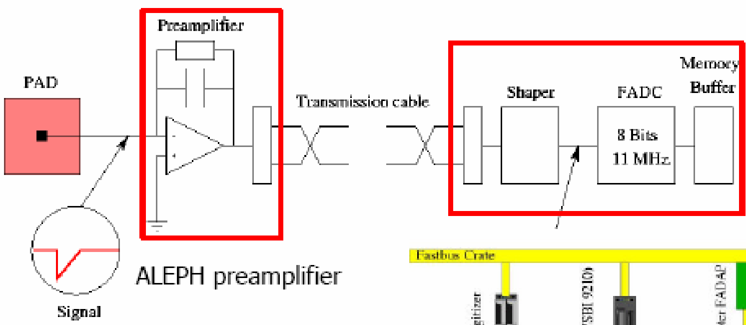
## Common Challenges

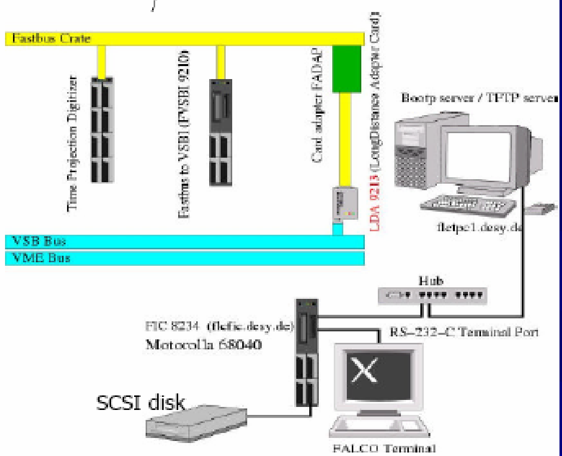
- Everything ON detector
- Collumn RO & sparcification
- Power cycling
- Read-out during Bunch Train
  → Influence of RF pick-up?

# TPC Read Out

From present (Aleph)

**TPC : a typical readout à la ALEPH**




**ALEPH TPC Electronics:**

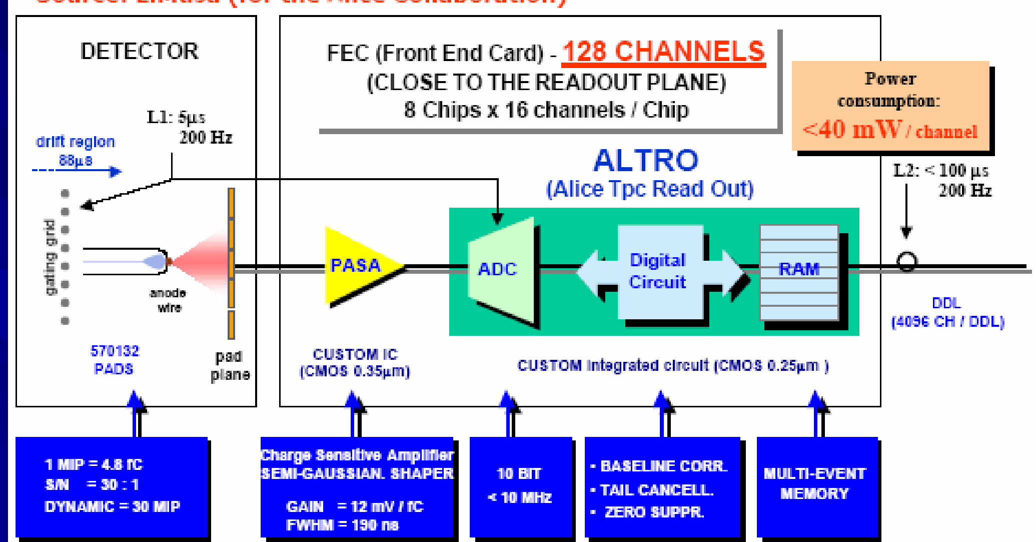
- Fastbus modules,
- TPD (4 x 16 ADC channels),
- FVSBI 9210 from CES,
- VME FIC 8234 from CES,
- readout sampling at 11 MHz.

- Software from ALEPH is used.

To future
(investigate Alice RO model?)

**The ALICE TPC Front End Electronics**

Source: L.Musa (for the Alice Collaboration)




**A single readout channel is comprised of:**

- a charge sensitive amplifier / shaper
- a 10-bit low power ADC
- a digital circuit for the tail cancellation, zero suppression, etc...
- a multi-event buffer (up to 8 event data streams)

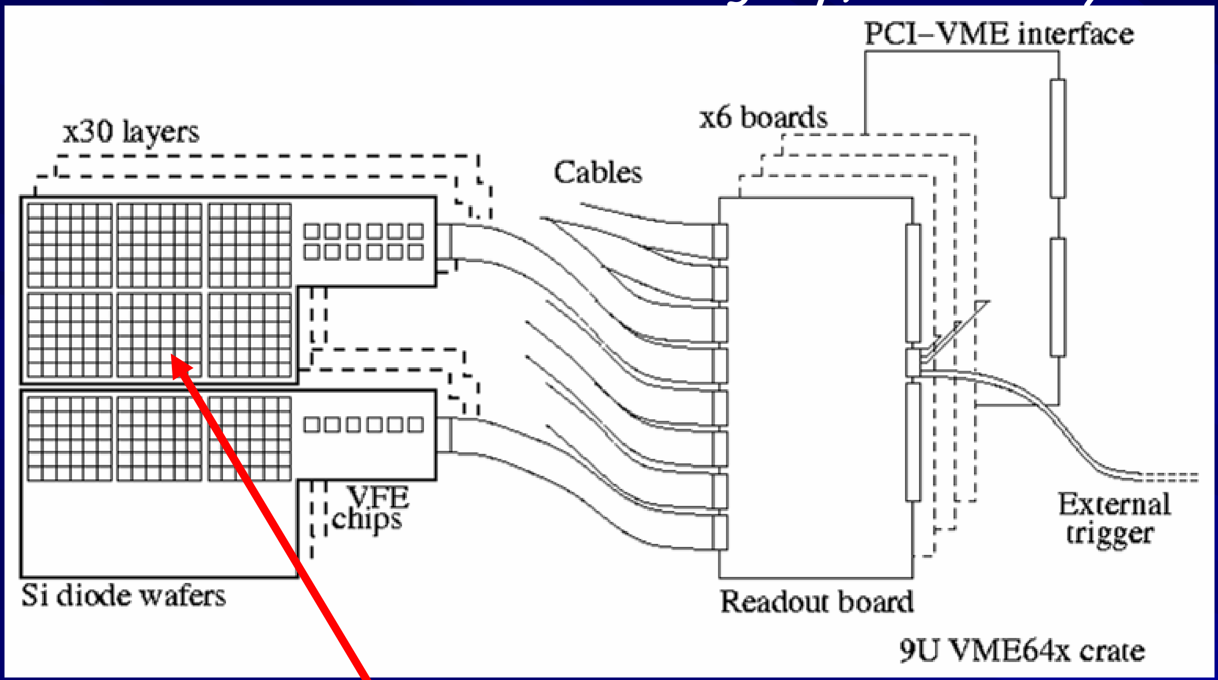
## Main Features

- VFE: GEM/Micromegas,Digital (Medipix)
- No active gating
- Continuous Read Out during the full bunch train (1ms)
- Minimize RO material in the end cap !

# Calorimeters Read Out

Today

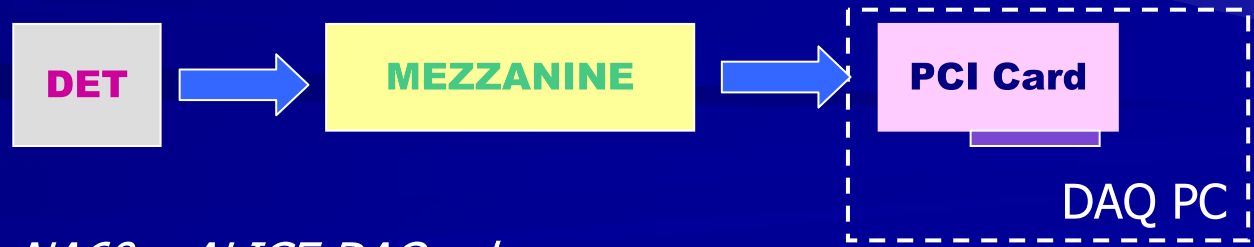
*CALICE UK group, P. Dauncey*




- RO every Xing (300ns)
- Uniform : EM,Hcal,Tail
- ~ 30 Million channels (SiW)
- Local Sparcification/buffer
- ASIC with 1024 channels
- Power cycling .....

*APD fibre masks or*
*flat-band connector to Si-PM cassette RO printed circuit*

Tomorrow investigation




*NA60 – ALICE DAQ scheme*

# Technology forecast (2005-2015)

- **FPGA for signal processing and buffering**
  - Integrates receiver links, PPC, DSPs and memory ....
- **Processors and memories**
  - Continuous increasing of the computing power
    - More's law still true until 2010! Expect x 64 by 2015!
- Memory size quasi illimited !
    - Today : 256 MB
    - 2010 : > 1 GB ... then ?
- **Links & Networks:**
  - Commercial telecom/computer standards
  - 10 -30- 100 GBEthernet !

***Systematic use of COTS products***

***→ make decision at T0 -3 years***

*Data Flow*

# Software trigger concept → No hardware trigger !

Detector Front End

Read-Out Buffer

Network

Processor Farm(s)

Storage

*up to 1 ms active pipeline (full train)*

## Sub-Detectors FE Read-out

Signal processing – digitization, no trigger interrupt

Sparcification,cluster finding and/or data compression

Buffering – dead time free

1 ms

3000 Hz

## Data Collection is triggered by every train crossing

**Full event building of one bunch train**

**Trigger :Software Event Selection** *using full information of a complete train* (equivalent to L1-L2-L3 …) with off line algorithms

Select 'Bunch Of Interest'

200 ms

30Hz

1 MBytes Average event size

## On-line processing

**Event classification** according to physics, calibration & machine needs

Few sec

**Data streams**

S1 S2 S3 S4 Sn

# Advantages → all

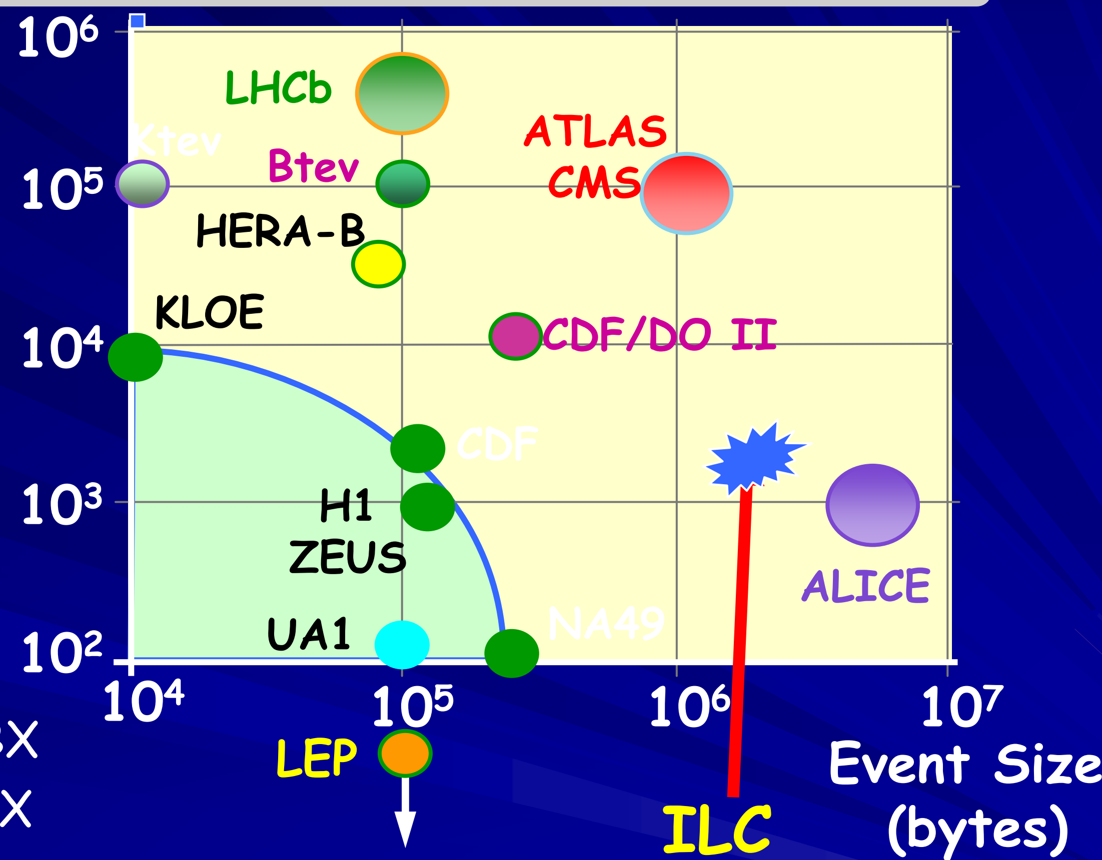
- Flexible
  - fully programmable
  - unforeseen backgrounds and physics rates easily accomodated
  - Machine people can adjust the beam using background events
- Easy maintenance and cost effective
  - Commodity products : Off the shelf technology (memory,switches, procsessors)
  - Commonly OS and high level languages
  - on-line computing ressources usable for « off-line »
- Scalable :
  - modular system

**Looks like the ' ultimate trigger '**

→ satisfy everybody : no loss and fully programmable

# Estimates Rates and data volume

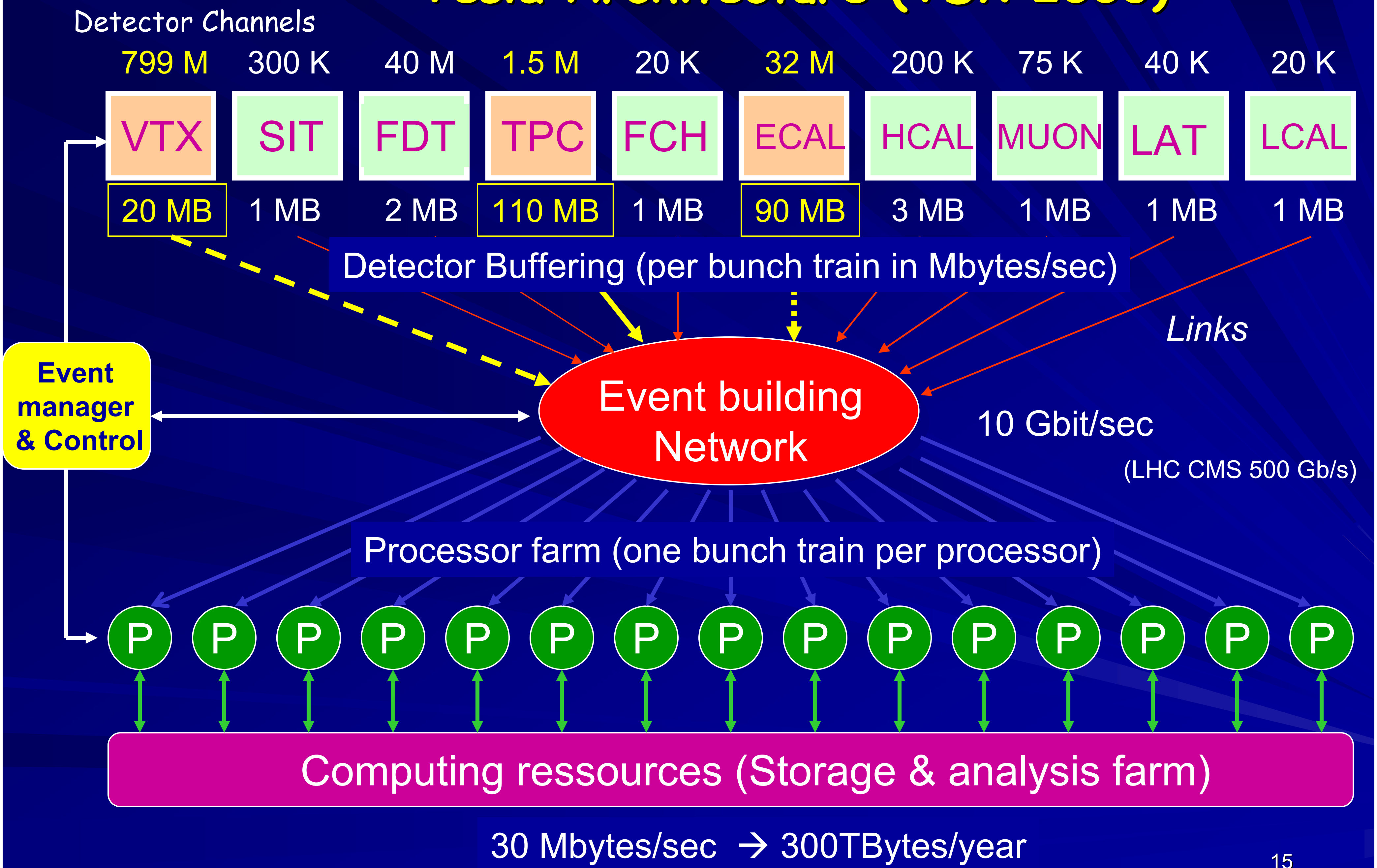
High Level-1 Trigger
(1 MHz)




- *Physics Rate :*
  - e+ e- → X  0.0002/BX
  - e+ e- → e+ e- X  0.7/BX
- *e+ e- pair background :*
  - VXD inner layer 1000 hits/BX
  - TPC 15tracks/BX

*-> Background is dominating the rates !*

# Tesla Architecture (TDR 2003)



# About systems boundaries …..moving due to !
# → evolution of technologies,sociology …..

NEW !

**Machine**
Synchronization
Detector feedback
Beam BT adjustment

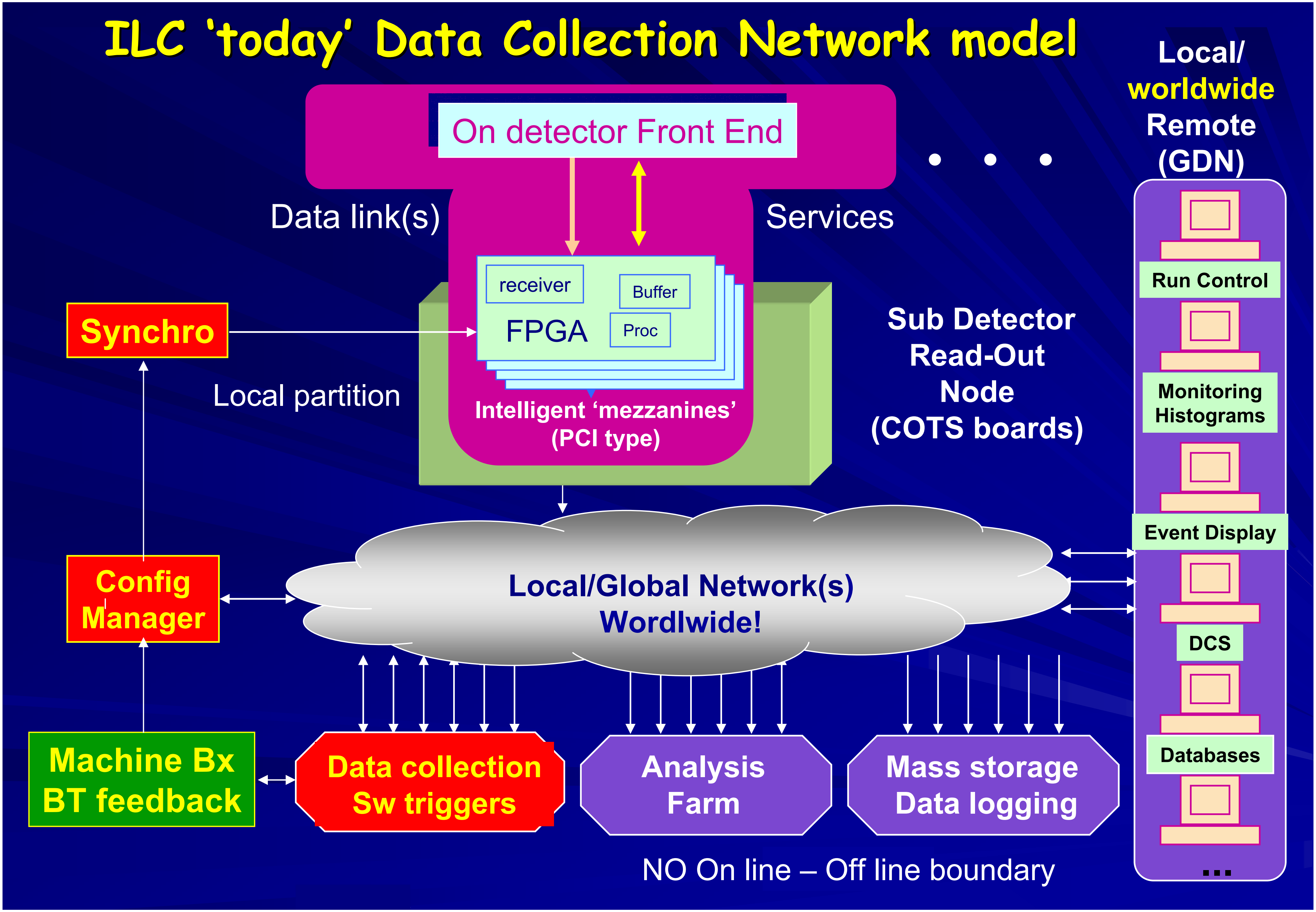
**Subdetectors Front End**
RO chain
Calibration
monitoring
Alignment …
FE Buffer

**Global Detector Nerwork (worlwide)**
- Detector Integration
- Remote Control Rooms (3)
  - Running modes
    - Local stand alone
    - Test
    - Global RUN
  - Remote shifts
    - Slow control
    - Detector Monitoring
- Physics & data analysis
(ex On- Off line)
  - Farms
  - GRID …
- Final Data storage

Full Integration of Machine DAQ In the data collection system

Uniform interface
Global synchronisation
Partitionning
(physical and logical)

**Data Collection (ex T/DAQ)**
Bunch Train Buffer RO
Event Building
Control - supervisor
On line Processing Procesors
SW trigger & algorithms
global calibration ,monitoring and physics
Local (temporary) Data logging (Disks)


ILC 'today' Data Collection Network model
Local/
worldwide
Remote
(GDN)
On detector Front End
Data link(s)
Services
receiver
Buffer
FPGA
Proc
Intelligent 'mezzanines'
(PCI type)
Synchro
Local partition
Sub Detector
Read-Out
Node
(COTS boards)
Run Control
Monitoring
Histograms
Event Display
DCS
Databases
...
Config
Manager
Local/Global Network(s)
Wordlwide!
Machine Bx
BT feedback
Data collection
Sw triggers
Analysis
Farm
Mass storage
Data logging
NO On line – Off line boundary

# Summary

The ILC environment poses new challenges & opportunities which will need new technical advances in VFE and RO electronics → NOT LEP/SLD, NOT LHC !

- Basic scheme: The FEE integrates everything
  - →From signal processing & digitizer to the RO BUFFER
- Very large number of channels to manage (Trakers & EM)
  - →should exploit power pulsing to cut power usage during interburst
- New System aspects (boundaries ..→ GDN !)
- Interface between detector and machine is fundamental
  - →optimize the luminosity → consequence on the DAQ
- Burst mode allows a fully software trigger
  - →Looks like the Ultimate Trigger: Take EVERYTHING & sort later !

→ GREAT! A sociological simplification!