Front-end electronics dedicated to the next generation of linear collider calorimeter

CALICE COLLABORATION

LPC Clermont

Samuel MANEN
Gérard BOHNER
Jacques LECOQ

LAL Orsay

Julien FLEURY
Christophe de la TAILLE
Gisèle MARTIN

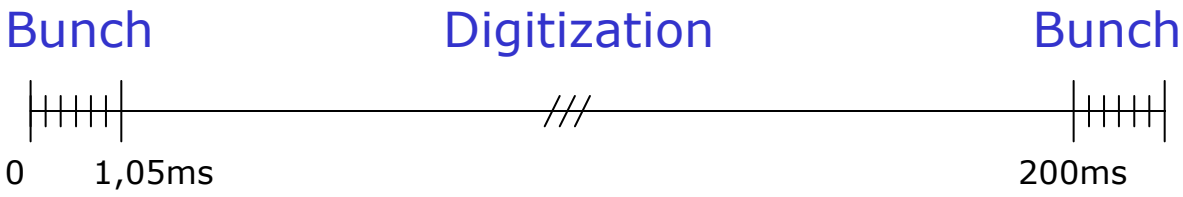
OUTLINE

- Requirements for ECAL
- Electronics synoptic
- Low noise preamplifier
- Shaper
- Pipeline analog to digital converter
  - Gain 2 amplifier.
  - The comparator.
- Conclusion and schedule.

Requirements for ECAL

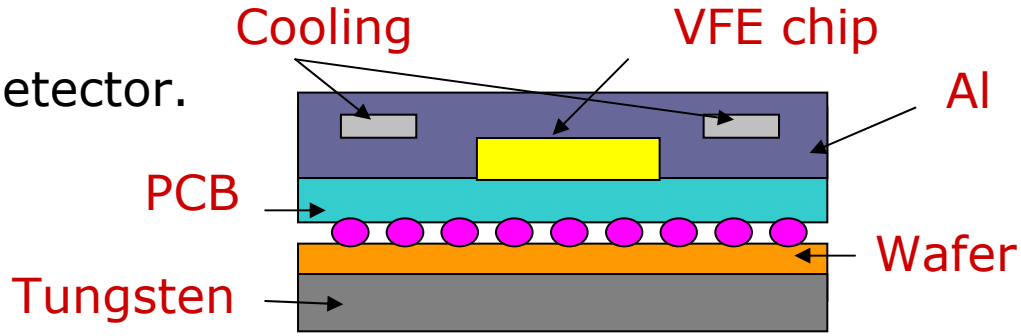
- ECAL : Barrel with sandwich silicon-tungsten structure composed of 40 layers of reading with diodes of 1cm².
- 34 Millions channels very low consumption
  - Pulsed power supply.
- Large dynamic range typically 14-15 bits and accuracy about 8bits.
  - Multi-gain system.
- Train = 3000 Bunch-crossing every 200ms.

  BX = between 150ns-300ns.
  - Slow system.



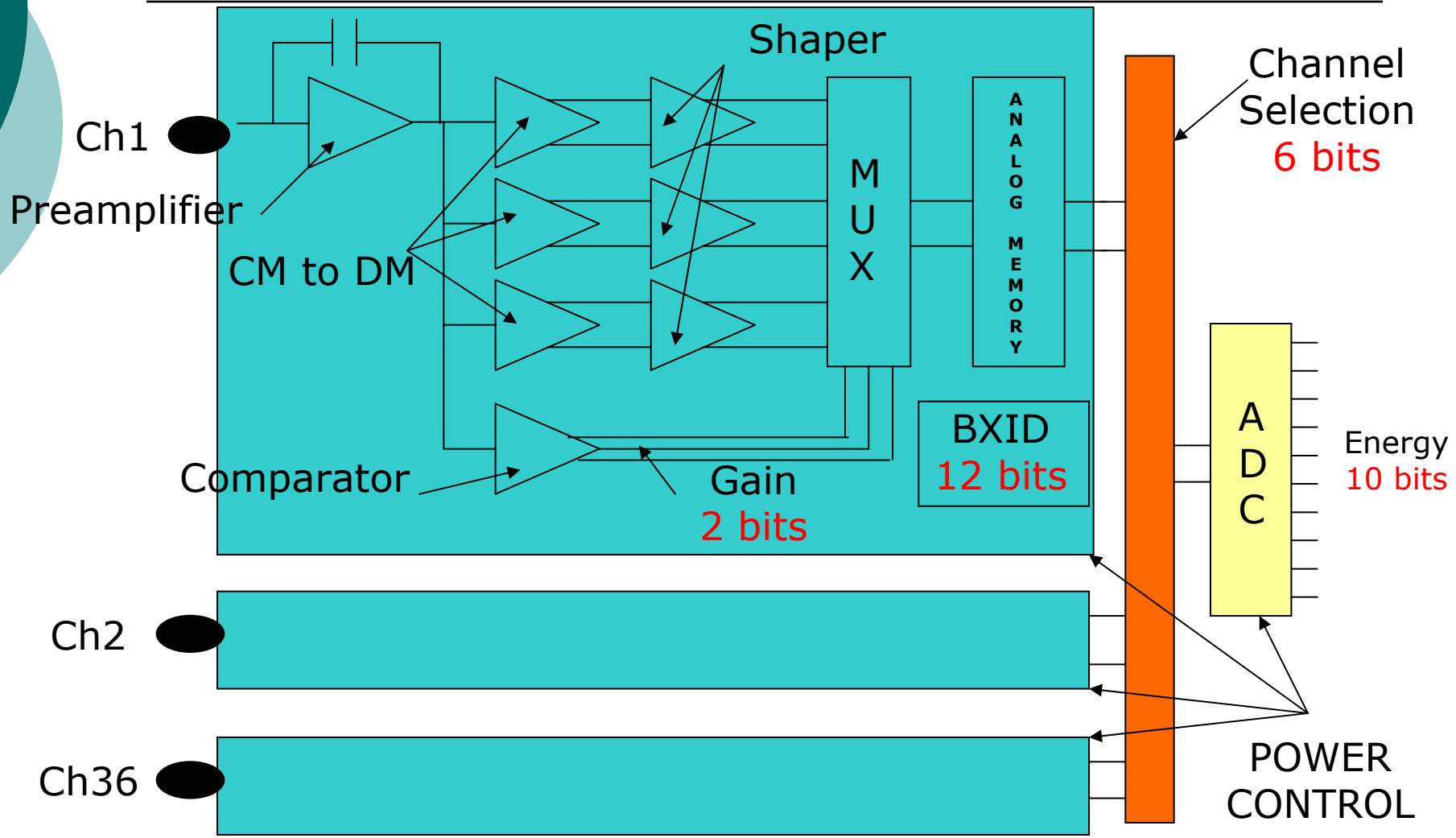
Electronics integration

- Chip embedded in detector.



  - Reduce line capacitance → reduce preamplifier consumption to obtain a noise less than 1/10 MIP (MIP= 40,000 e-).
  - Reduce crosstalk.
  - Electromagnetic shower on chip???
  - Cooling issues.
- Sensor (diode) is a wafer 6cm*6cm so 1 chip for 36 channels.
  - 34 Millions channels → 950,000 chips.
  - 34 Millions channels → 3,400 m² silicon.

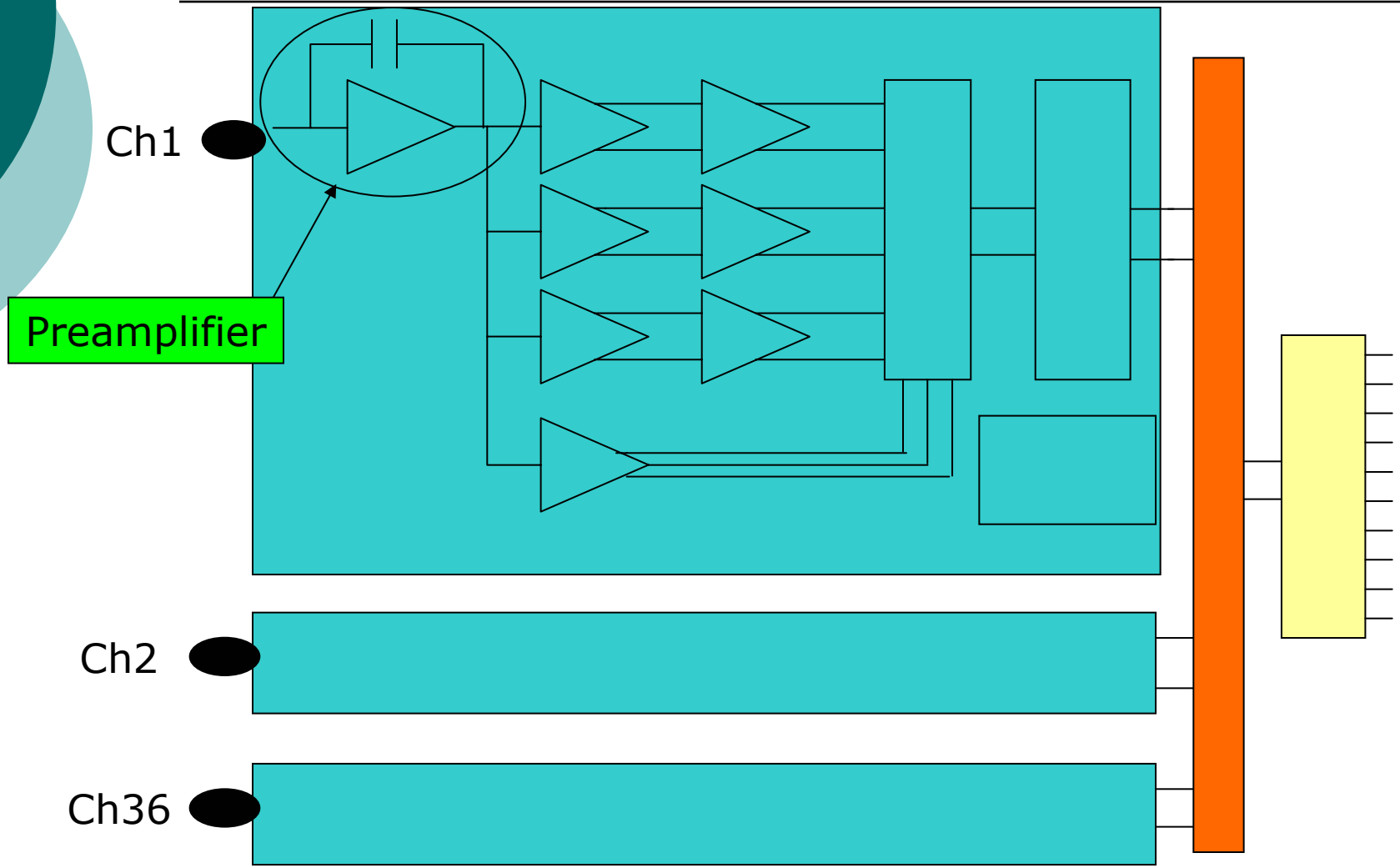
Electronics synoptic



Technology choice for R&D

- The electronics for front-end will be mixed
  - Need good digital performance.
  - Need good analog performance.
  - As cheap as possible.
- Our choice AMS 0.35µm CMOS (c35b4)
  - Perennity because used by car industry.
  - Two transistors type.
    - Transistor 3.3V for digital block.
    - Transistor 5V for analog block.

THE PREAMPLIFIER



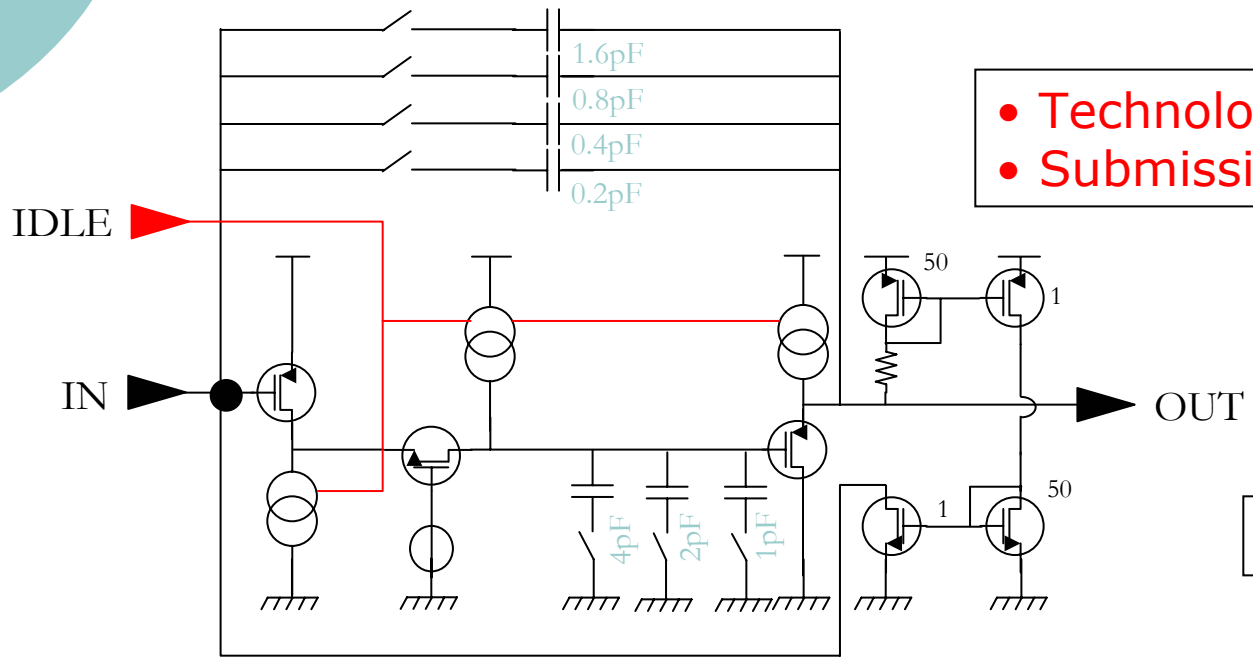
Low noise preamplifier

- MIP is fixed by silicon wafer depth: 500µm so 40,000e-
- Noise is defined as MIP/10 so 4000e-.
  - Two types of noise :
    - Serial noise : $$e_n^2 = \frac{8 \times k \times T}{3 \times g_m} + \frac{A_f}{f}$$

      The noise 1/f is neglected because we have a transistor Pmos in input.
    - Parallel noise : $$i_n^2 = 2 \times q \times Ig + \frac{4 \times k \times T}{Rf}$$
- Use a big transistor Pmos to have important g_m.
  - Large W 2000µm.
  - Small L 0,5µm.
  - Need current I_{ds}=200µA (power limited 1mW for preamplifier).

Schematic of the preamplifier

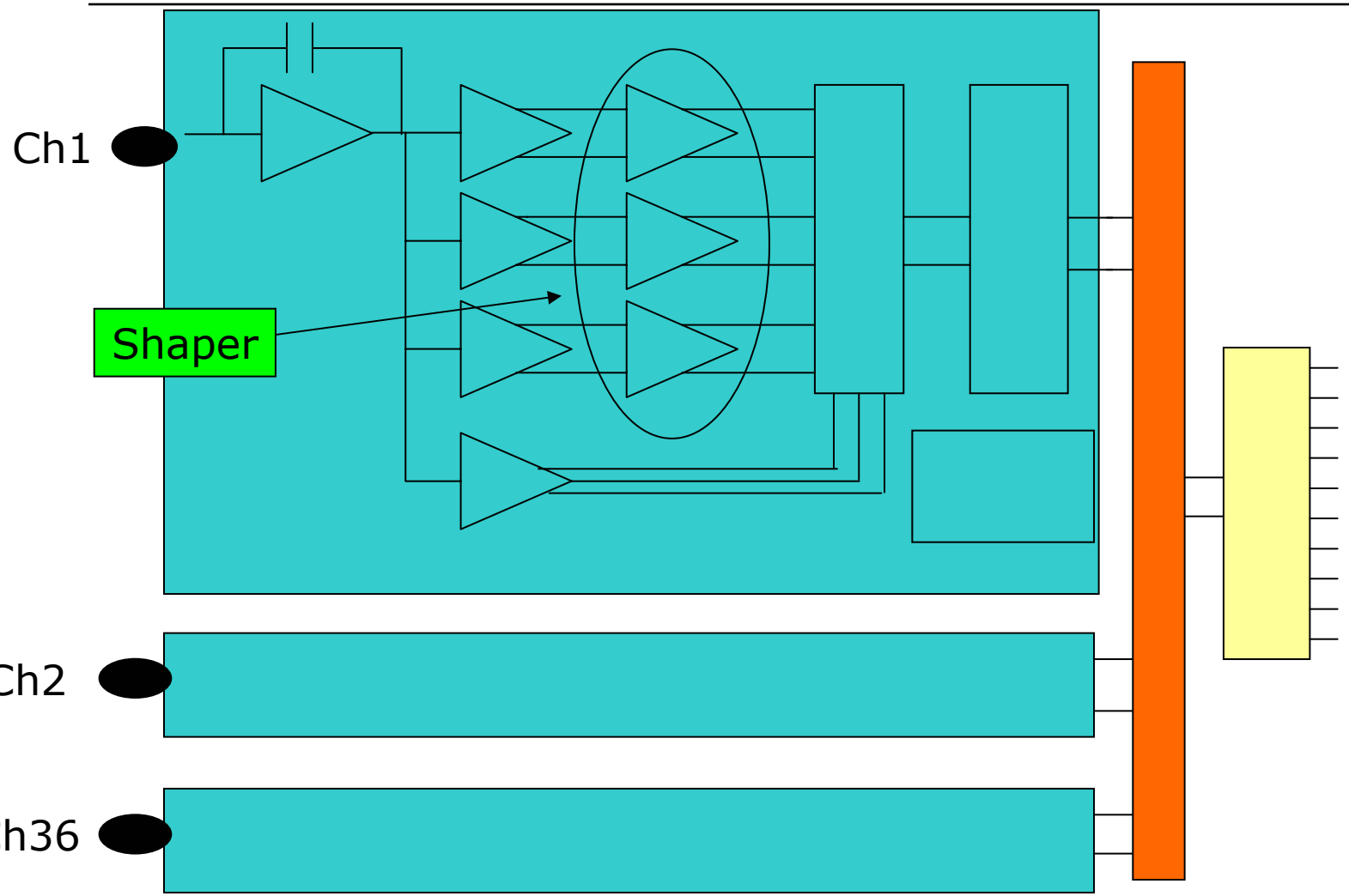
- Standard charge preamplifier
- Low consumption: below 1mW
- Low noise: about 1nV/√Hz



- Technology: AMS CMOS 0.35µm
- Submission: April 19th 2004

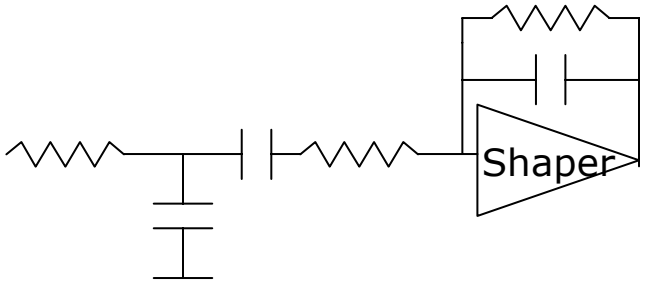
LAL Orsay (J.Fleury)

Electronics synoptic



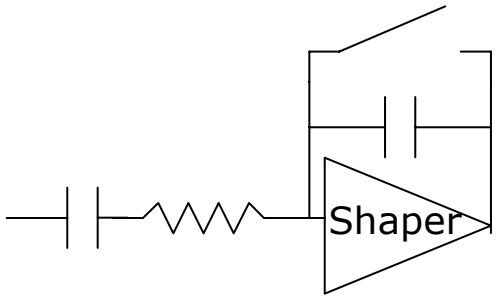
Two alternatives of filtering

- Shaper CRRC²
  - g_m=10mA/V→e_n=1.1nV/√Hz
  - I_g=30nA →i_n=100fA/ √Hz



  - ENC=1,430e-
  - Advantage:
    - System well known
  - Inconvenient:
    - Takes a large place with resistances
    - Slow reset, probably pile-up.

- Switched integrator
  - Same conditions

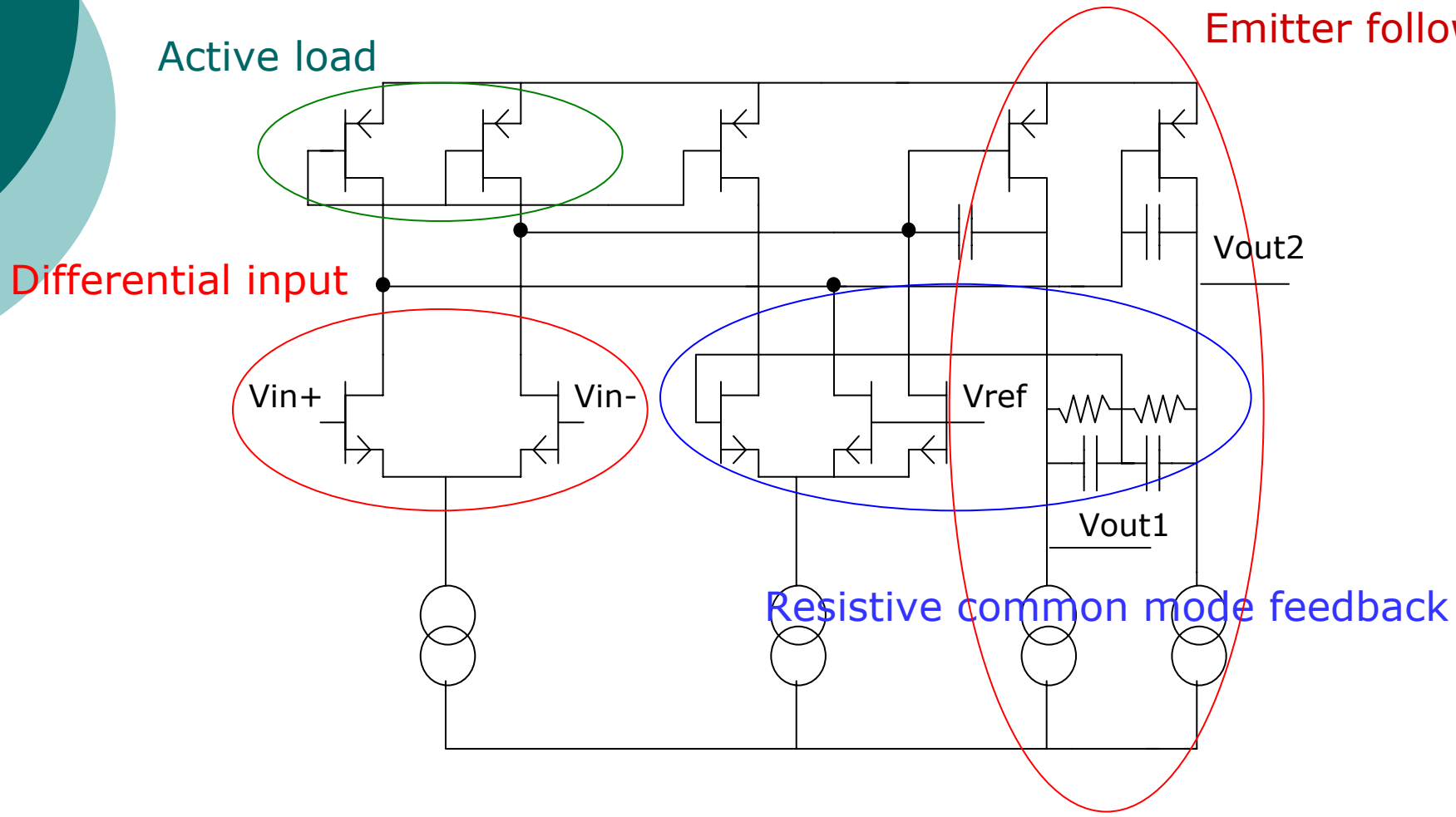


  - ENC=1,660e-
  - Advantage:
    - Good integration of switch
    - No pile-up
  - Note:
    - Need a command signal

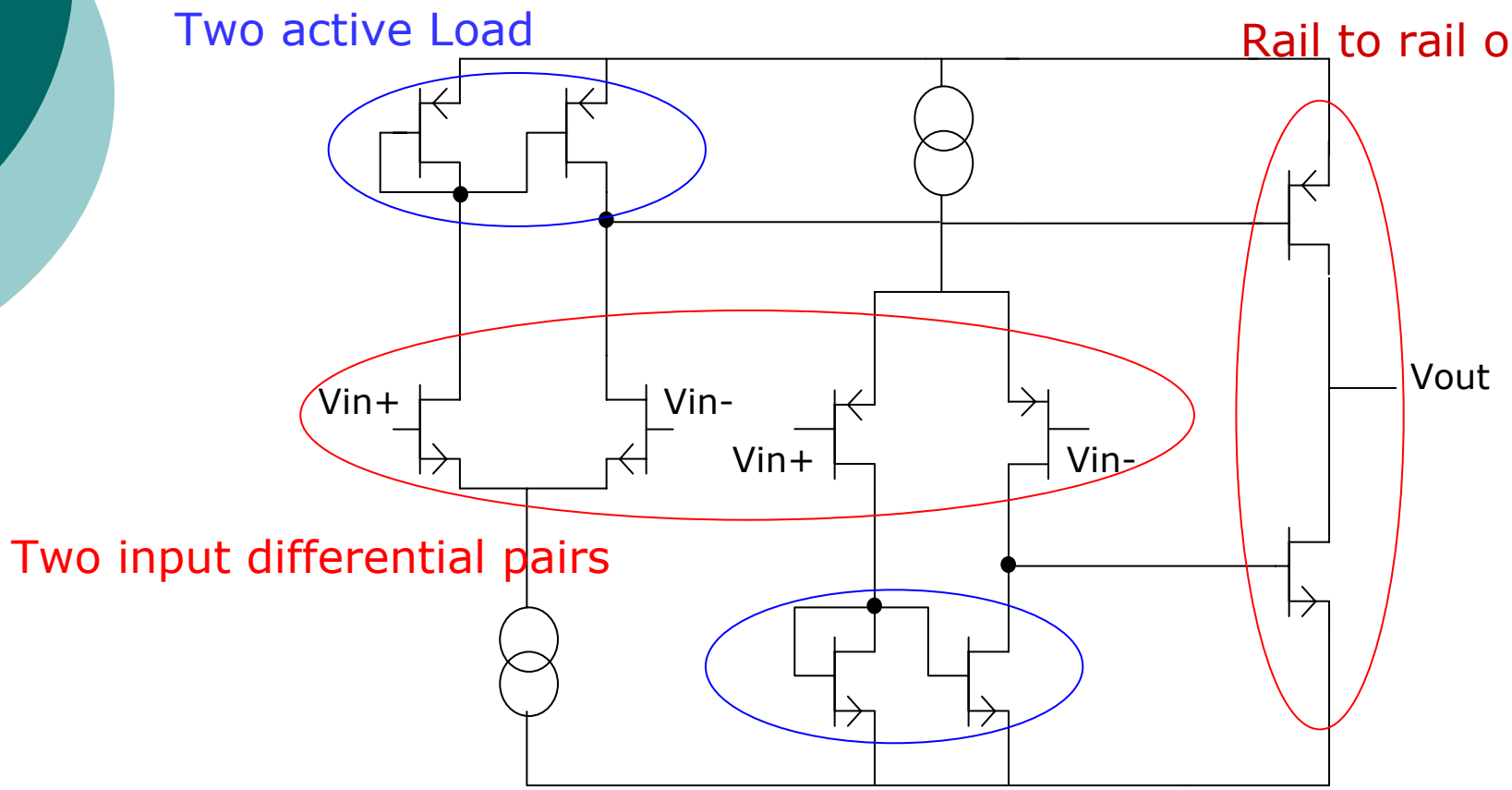
Amplifier of the shaper

- Development of an amplifier in two technologies :
  - Shaper is built with an amplifier used as integrator in 0.8µm BiCMOS.
  - Gain 100 amplifier in 0.35µm CMOS to define offset.
- Mixing of two schematics
  - An amplifier with resistive common mode feedback.
  - A differential amplifier with input and output rail to rail.

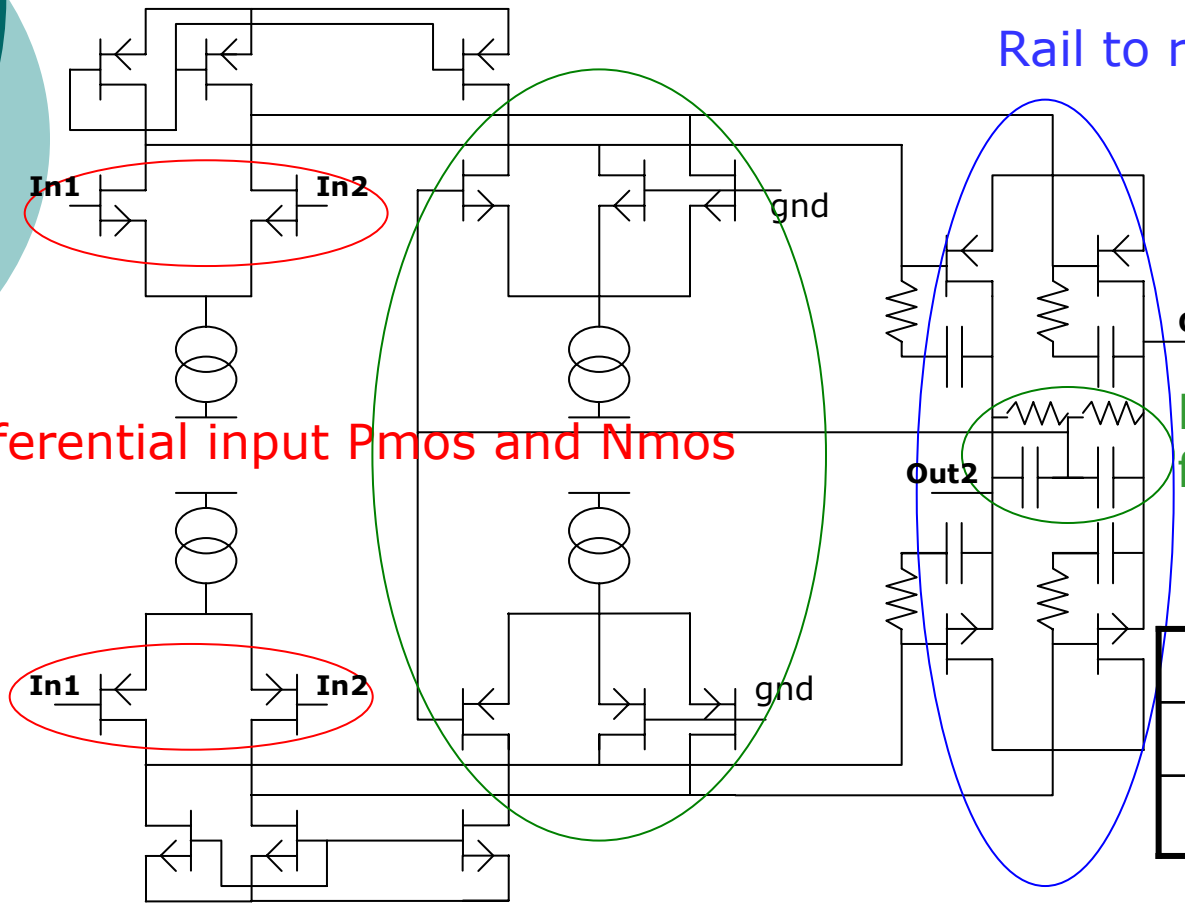
Differential amplifier with resistive common mode feedback



Differential amplifier with rail to rail input output



Amplifier CMOS



Rail to rail differential output

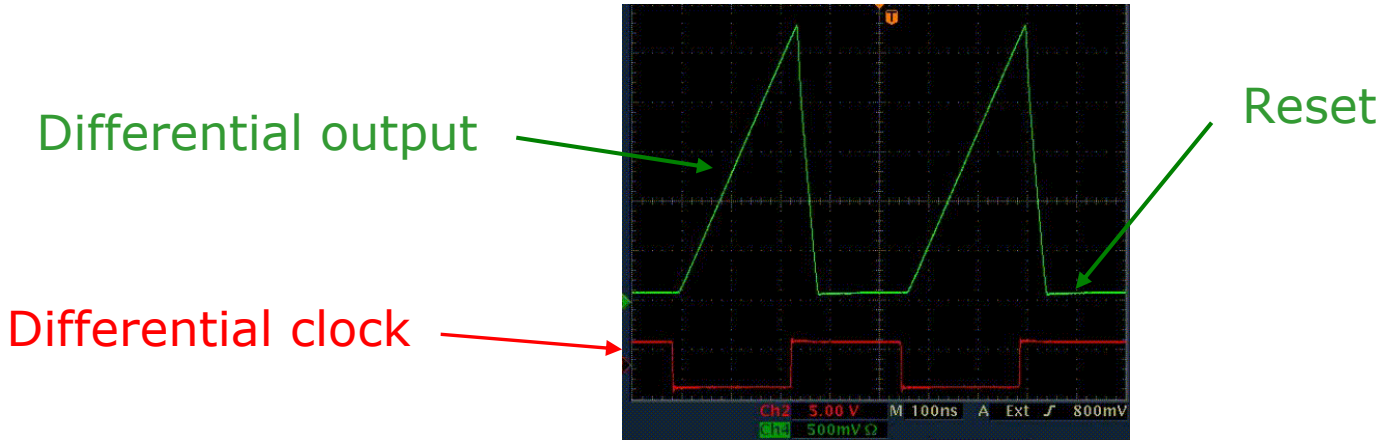
Differential input Pmos and Nmos

Resistive common mode feedback

Power Supply	±2,5V
Consumption	300µA
Gain-bandwidth	50M

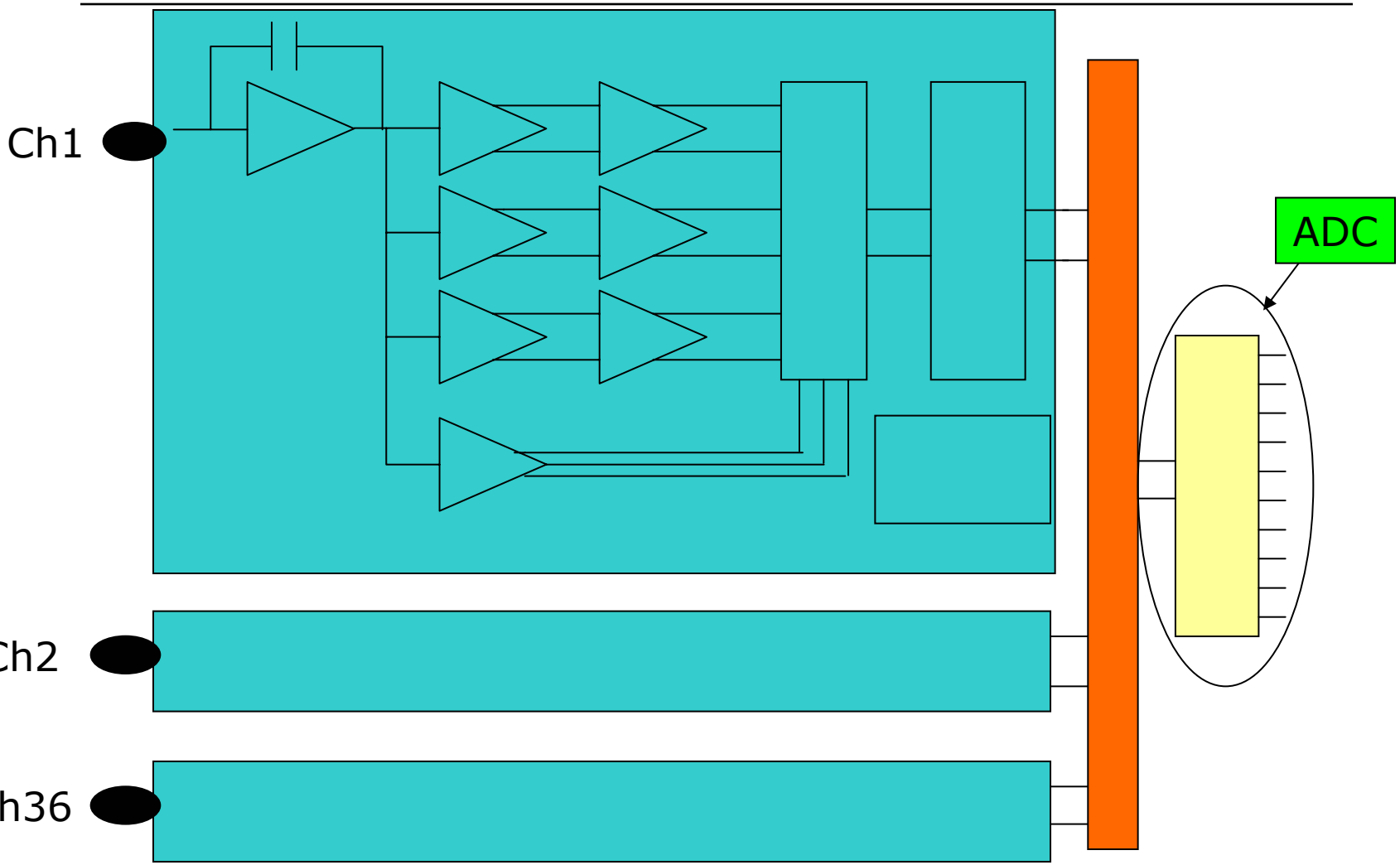
Amplifier: some tests results

- Two versions of amplifier
  - One in 0.8µm with the amplifier in integrator. OK.



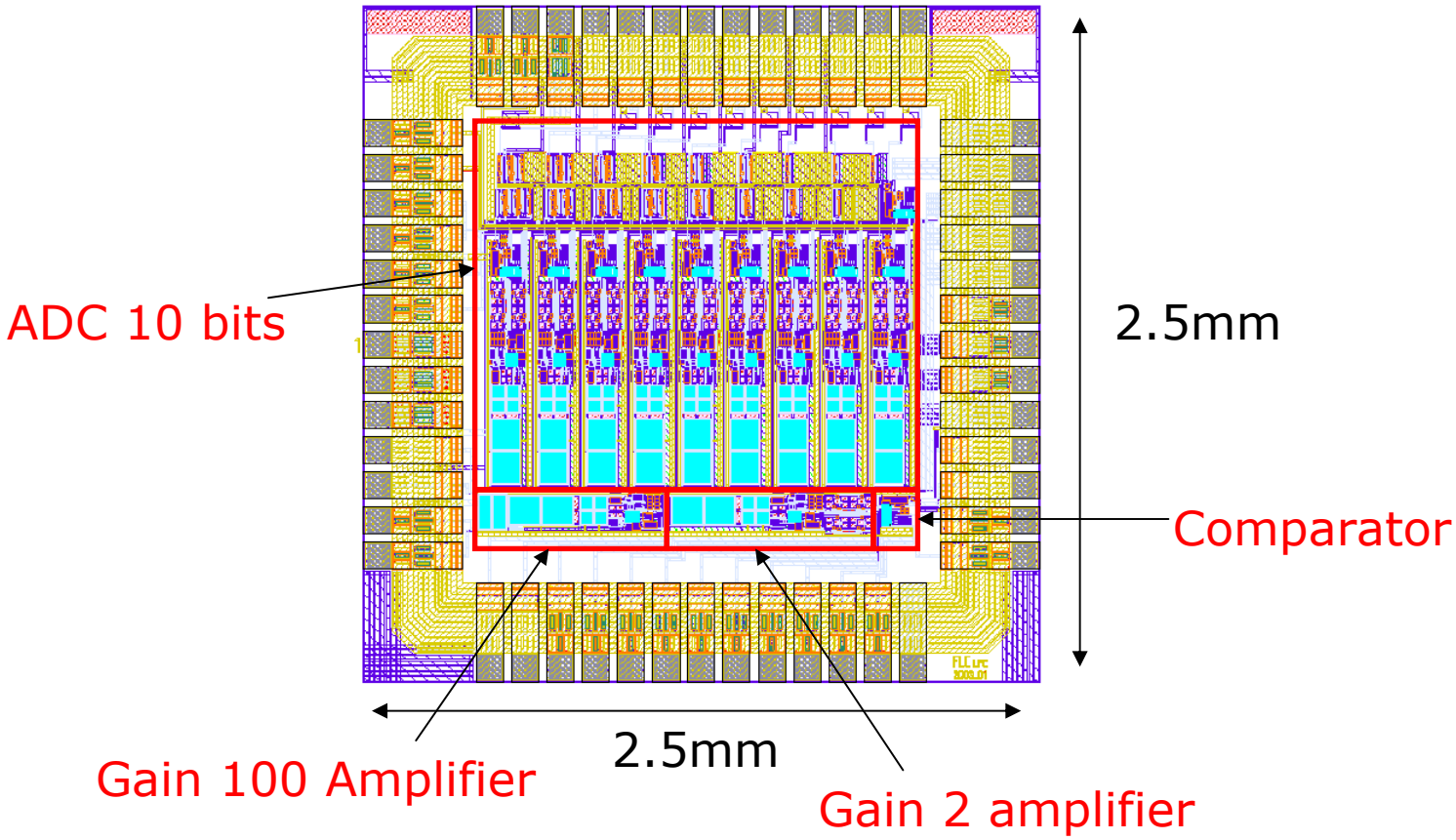
  - One in 0.35µm with the gain 100 amplifier :
    - Offset measured=1mV, so good matching.

Electronics synoptic

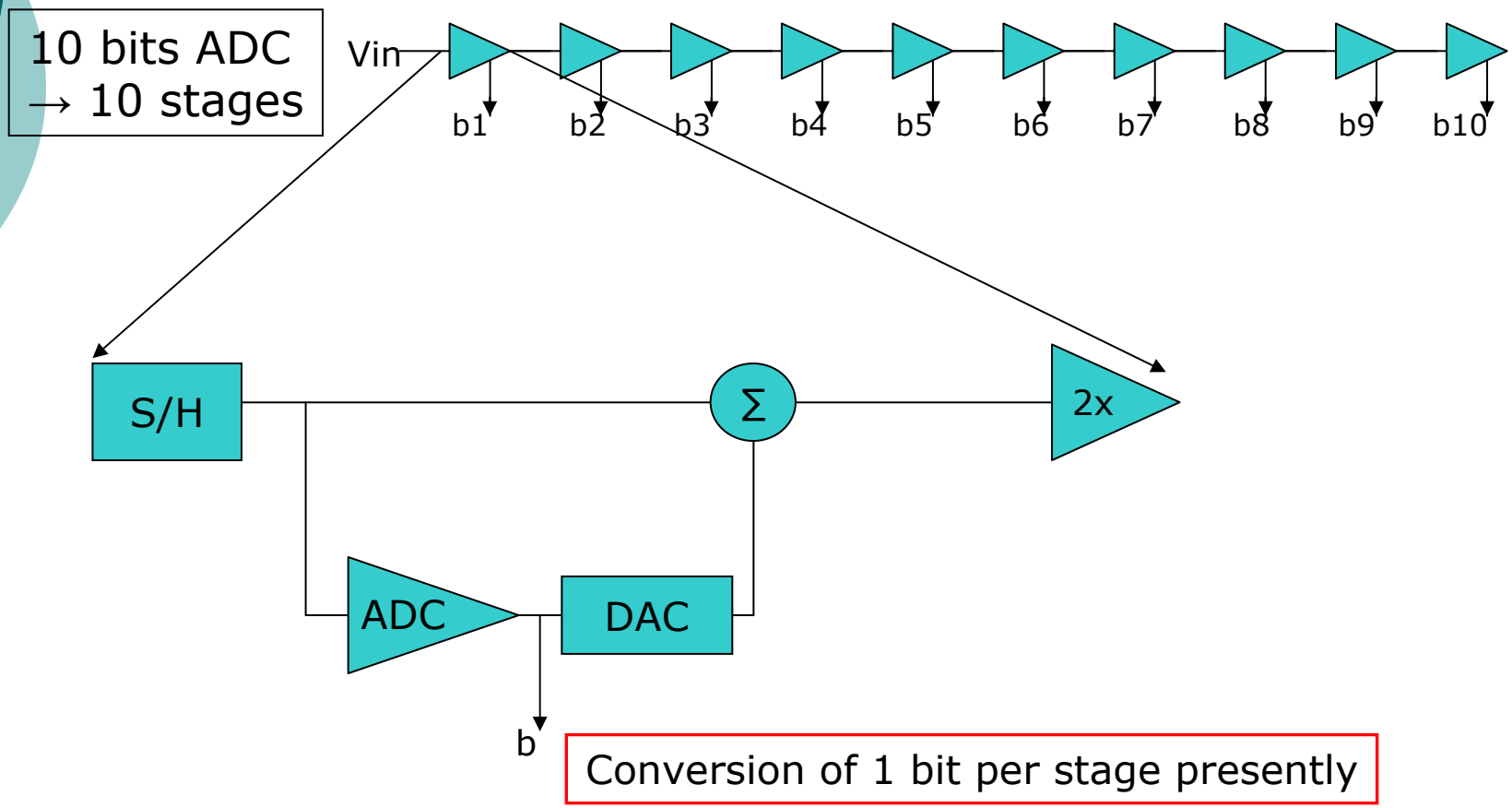


The chip in technology 0.35µm CSI

Chip developed and tested in 2003. Area 6.25 mm².



ADC pipeline schematic principle



ADC equivalent scheme

Two cases :

- If Vin > Vref

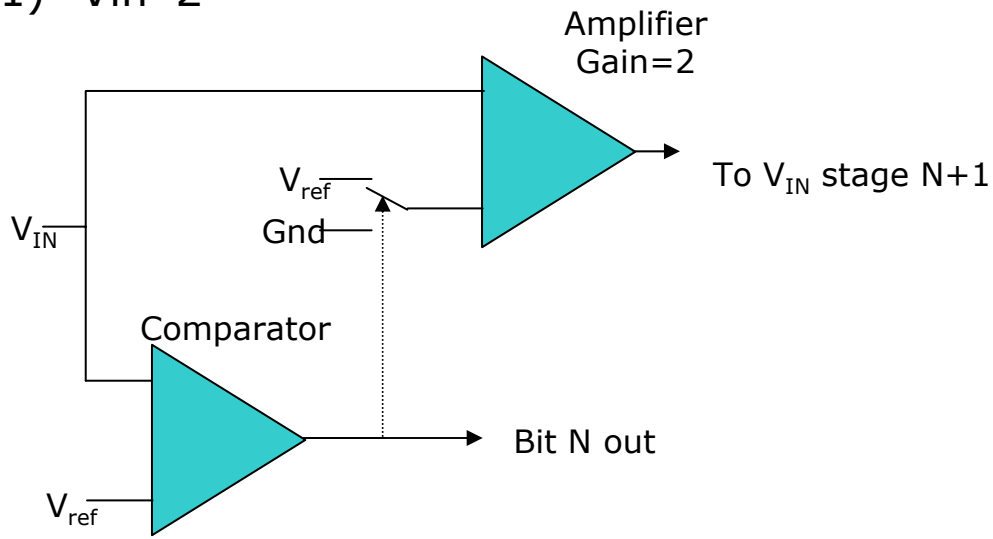
→ Bit N out =1 and Vin(N+1)=(Vin-Vref)*2

- If Vin < Vref

→ Bit N out =0 and Vin(N+1)=Vin*2

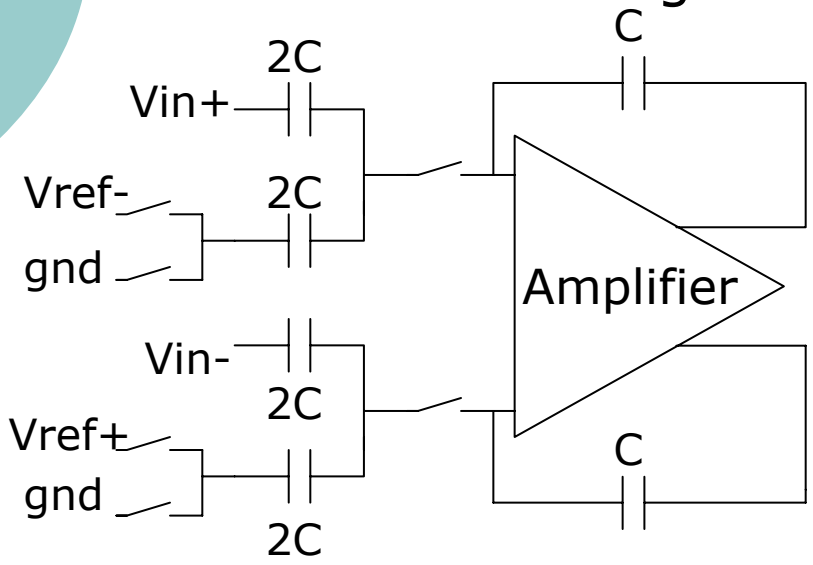
What we need:

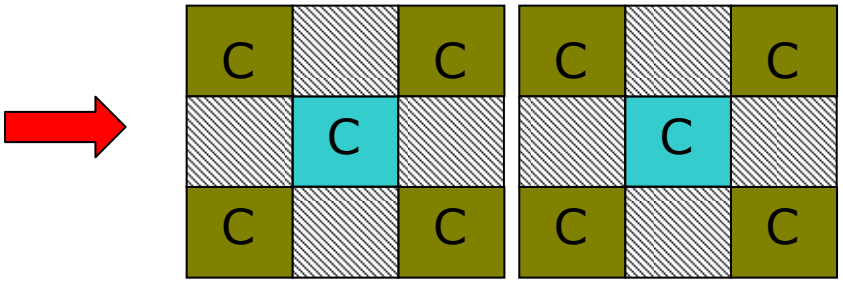
- An amplifier in gain 2.
- A comparator.



Gain 2 amplifier

- Gain 2 amplifier is identical to the shaper one.
- Hard to do a gain 2 to obtain 10 bits.



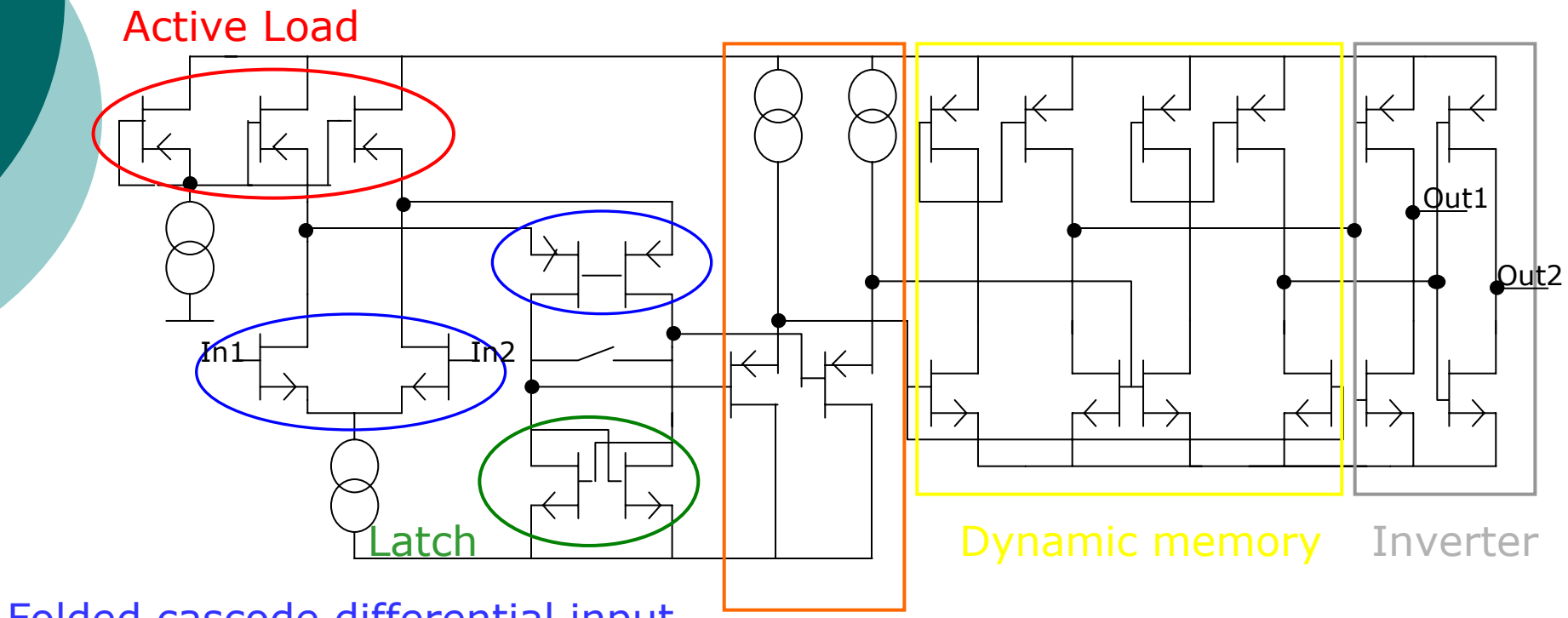


Layout capacitance with C=300fF (18.5*18.5µm)

Tests results:

- ❑ Average gain=2.01±0.02
- ❑ Average offset=-4±4mV

Comparator CMOS



Comparator is used in other IN2P3 laboratories.

Comparator tests and simulation results

Power Supply	±2,5V
Consumption	100µA
Clock frequency	5MHz
Sensitivity	300nV
Offset	9mV

Simulation parasitic results

Noise

Sensitivity	300µV
Offset average	11mV

Tests results

CONCLUSIONS:

- Very good modelisation.
- Must improve offset due to parasitic capacitance.
- Sensitivity in test correspond to the noise of system.

Simulations and tests results for ADC

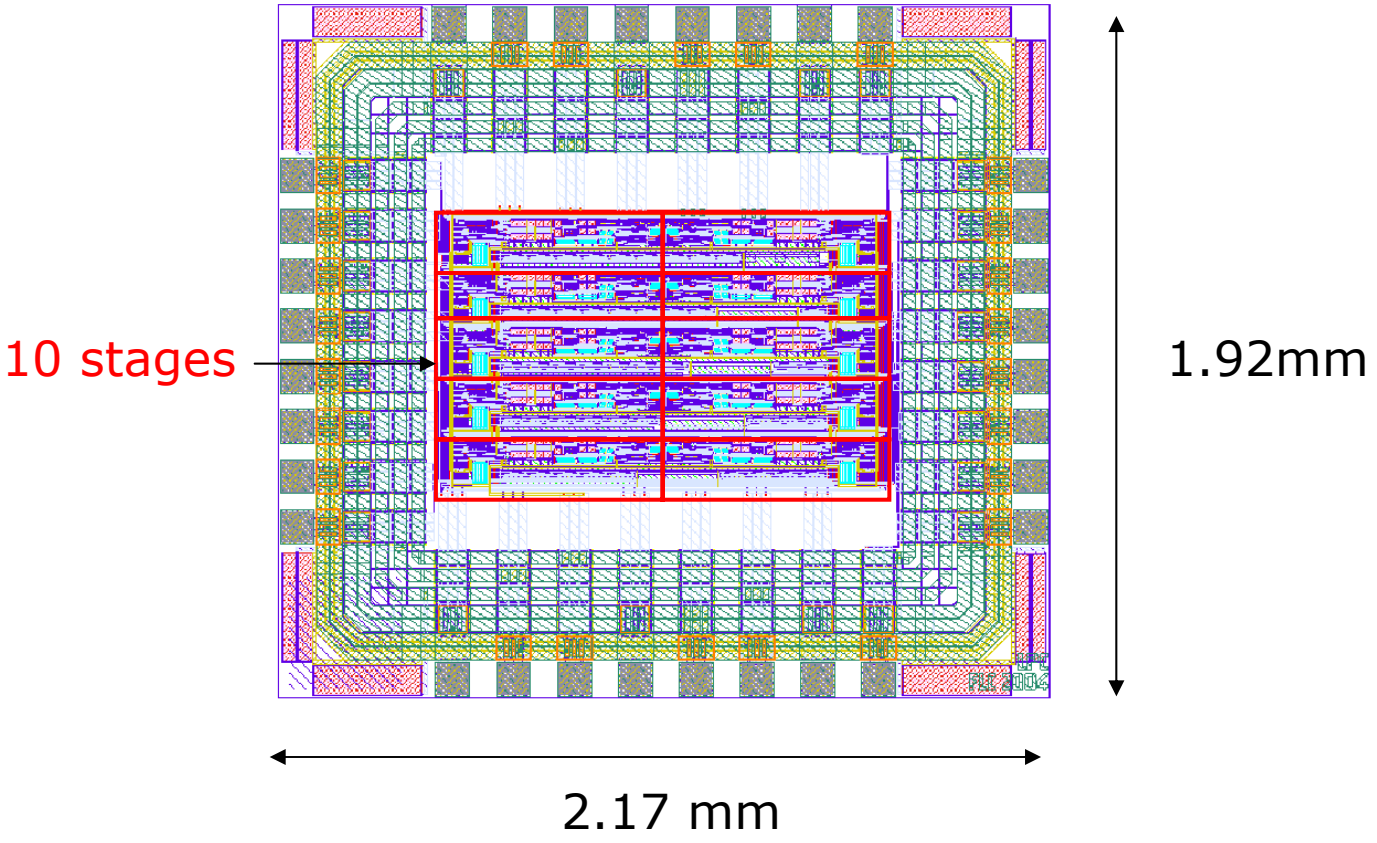
- First simulation results successful but in fact this simulation was done without parasitic capacitance…!!!
- TESTS:
  - Functionality verified.
  - 5 first bits are obtained.

Power supply	± 2,5V
Dissipation	20mW
Input	±1V
Clock	5MHz

- SIMULATION with parasitic:
  - Problems of stability with amplifier.
  - Very important error on output code.

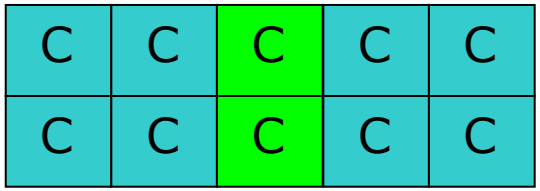
New ADC pipeline 10 bits in 0.35µm C35B4

Chip send in July 2004. Area 4.17 mm².



Improvements done for ADC

- Polysilicium high resistivity permits to draw big resistance
  - Occupy less place on silicon.
- AMPLIFIER:
  - Amplifier stabilization with higher RC on rail to rail output.
  - New layout for gain 2: more compact to obtain better matching.



- COMPARATOR:
  - Offset improvement.
- More important power supply decoupling.
- Simulation results with parasitic this time
  - 10 bits obtained, wait and see for tests in October 2004.

Conclusion

- One possible global scheme of the FE electronic exists.
- Two possibilities of filtering OK.
  - Shaper CRRC²
  - Switched integrator
- Charge preamplifier, a shaper and a comparator CMOS exist.

Schedule

- News improvements for ADC:
  - 1.5 bit per stage for consumption.
  - Not exactly the same block for 10 stages.
  - To reduce consumption only one master current for all amplifiers and comparators.
  - Perhaps, need digital correction. Not realized for the moment.
  - Offset correction for amplifier?...