# ATLAS Local Trigger Processor

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# Level-1 Trigger Overview

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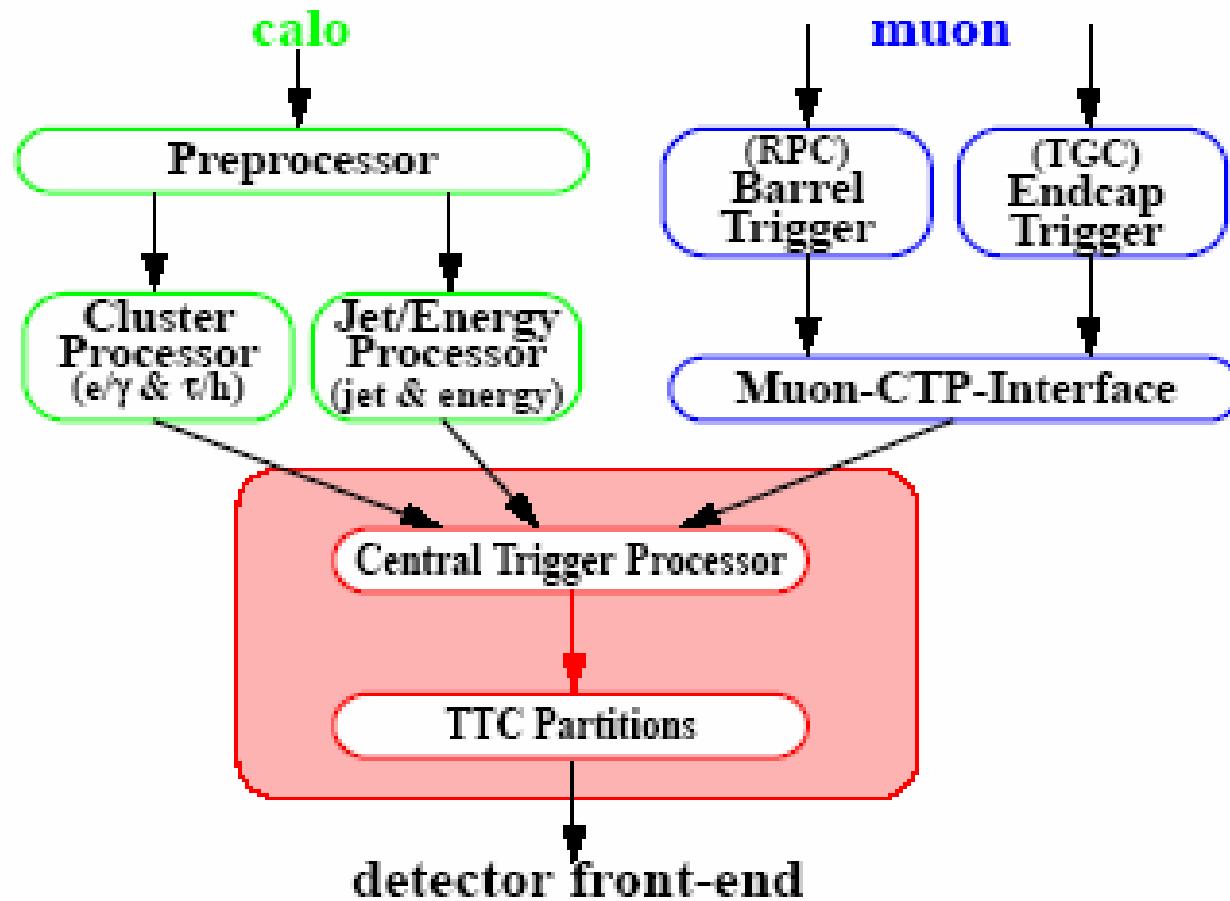
# Why a Local Trigger Processor module?

- **Need for an interface between the Central Trigger Processor and the TTC partitions**
  - TTC signals transmission
  - Dead-time (BUSY) handling
  - Calibration requests capability
- **Need for stand-alone operation of partitions**
  - Including capability for running several partitions
  - Dealing with dead-time

→*LTP module and CTP-Link*

# TTC Partition Root

- 4 modules
  - LTP
  - TTCvi
  - TTCxx (vx, ex or tx)
  - ROD-BUSY module
- LTP receives the CTP-Link from the CTP and allows to run in stand alone mode
  - i.e without the CTP

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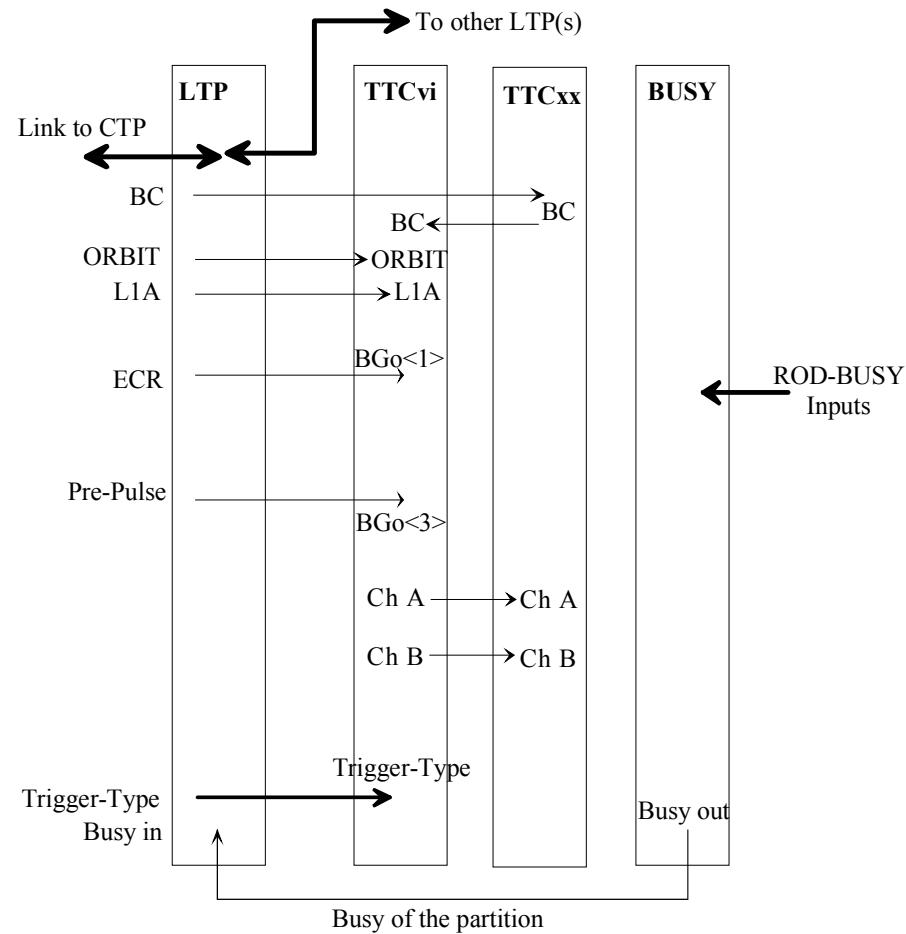
# CTP Link

- It contains →

- One link per sub-detector
  - Several LTPs daisy chained on this link
  - Up to 20 links delivered by the CTP

- LVDS signals

| BC | LHC clock |
|----|-----------|
| ORBIT | LHC ORBIT signal |
| L1A | L1 Accept signal |
| Trigger-Type | 8-bit trigger-type word issued by the CTP with each L1A |
| ECR | Event Counter Reset signal |
| Pre-Pulse | A signal issued by the CTP indicating that in N BC a L1A will be issued. |
| BUSY | The BUSY signal generated by the RODs of the sub-detector |
| Calibration | 3-bit word issued by the sub-detector and used by the CTP to generate calibration triggers |

**CTP**

LTP   LTP   LTP   LTP

CTP Link    CTP Link continuation
            BUSY signal
            is daisy-chained

**LTPs of one sub-detector**
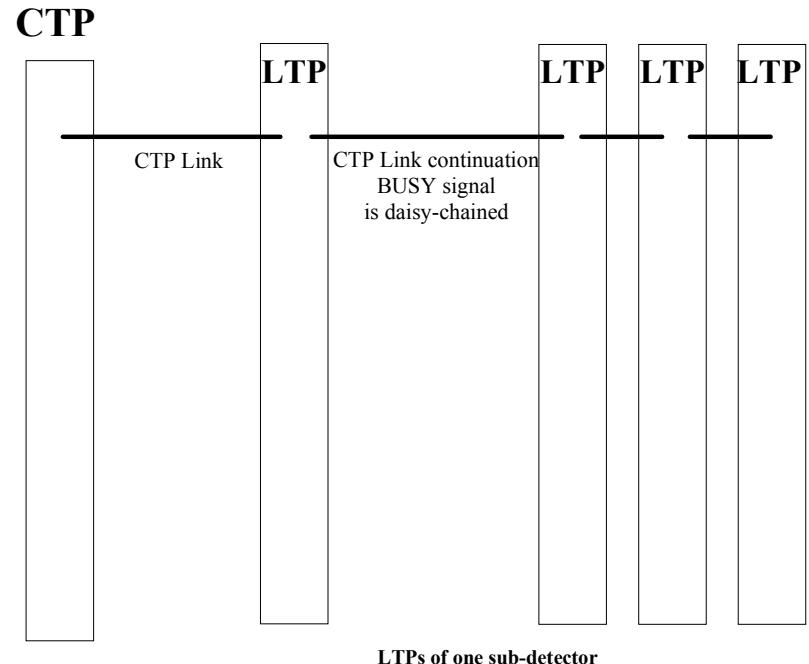
# LTP Basics

- Contains the interface to CTP functionality
  - Connection to the CTP with possibility to daisy chain
    - Output link
  - Connection to the TTCvi and TTCxx (TTCex or mx or vx)
- Contains all the tools to generate local triggers, local commands (B-Go), trigger-type
- Handles the dead-time when in local mode
- Is able to act as a master on the output link
  - Allows to easily drive several TTC partitions from one LTP
    - Assuming they are on the same link
    - Mainly for TTC partitions from the same sub-detectors

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# LTP in global mode

- Get all the timing and trigger signals from the CTP
  - BC, Orbit, ECR, Pre-Pulse, L1A

- Send the Busy signal and the calibration requests to the CTP
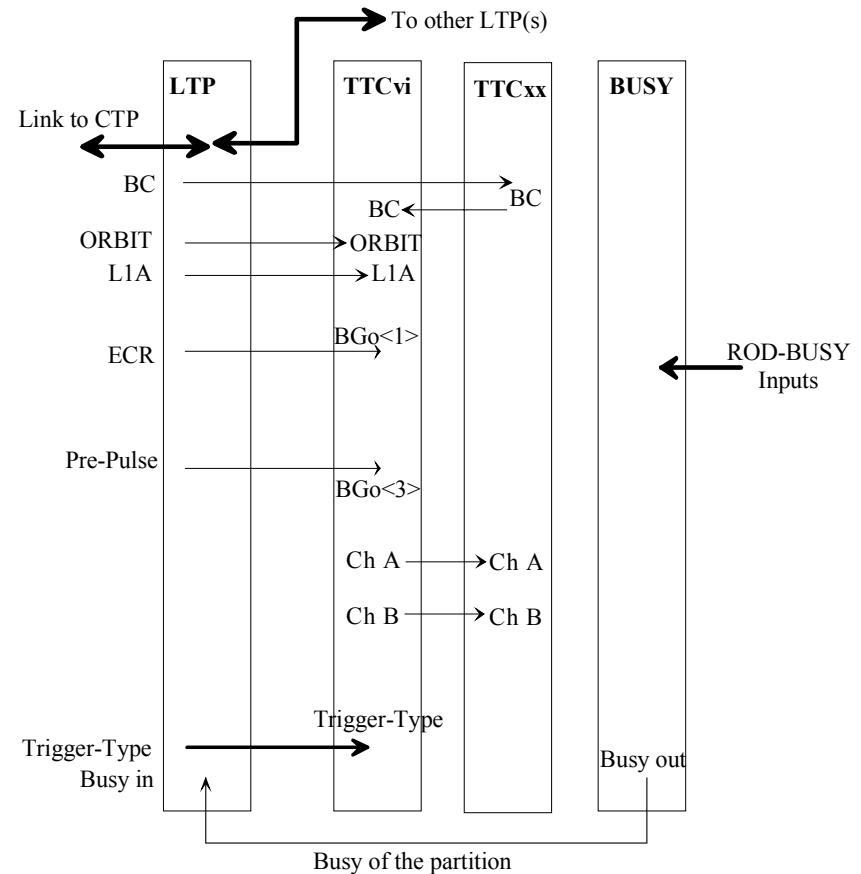
# Calibration requests

- Input to CTP:
    - Each <u>sub-detector</u>: 3-bit calibration trigger
    - 16 sub-detectors and other sources of calibration triggers defined
    - CTP contains 4-bit LHC turn counter: each turn is assigned to one sub-detector
- Generate L1A when:
    - Calibration trigger input has value ≡ 1 .. 7
    - Current LHC turn is allocated to the sub-detector
    - Current BCID is in BCID group for calibration: e.g. empty bunches, large gap
    - No dead-time generated by CTP, no external BUSY
- Identify calibration trigger:
    - Trigger type word
- Timing to be set-up by sub-system
    - e.g when should a pulser fire to get data in phase with L1A

# Role of the LTP in Stand-alone Mode

- Generates local trigger and handles locally the dead-time

- Generates "Trigger_type", synchronisation signals, ... for some special calibration runs

- Must allow to have several separate partitions from several sub-detectors running together
  - e.g Calorimeter(s) with Level-1 calorimeter

# LTP in stand-alone mode

- Use local triggers and local commands
  - May still use BC and Orbit from the CTP
- Handle the Busy to introduce local deadtime
- May drive its output CTP Link towards other LTPs and receive Busy signals from these other LTPs
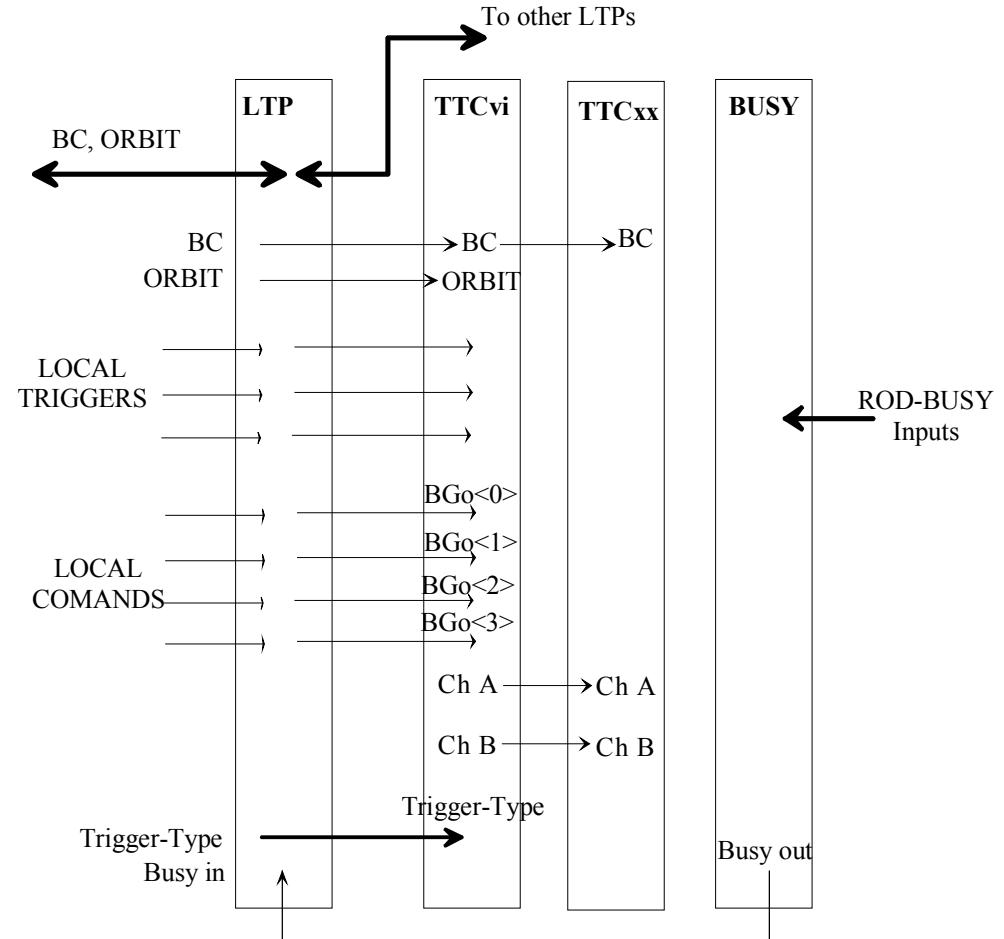


¹ **TTCtx, TTCex, or TTCvx**

# Block Diagram

CTP link input

CTP link output

**Local inputs
BC,
Local Triggers,
Local Commands,
Busy,
Calibration Req.**

Programmable
Switch
+
Pattern Generator
+
Logic

**Local outputs
BC, L1A,
Local Triggers
Commands,
Busy,
BGo<i>**
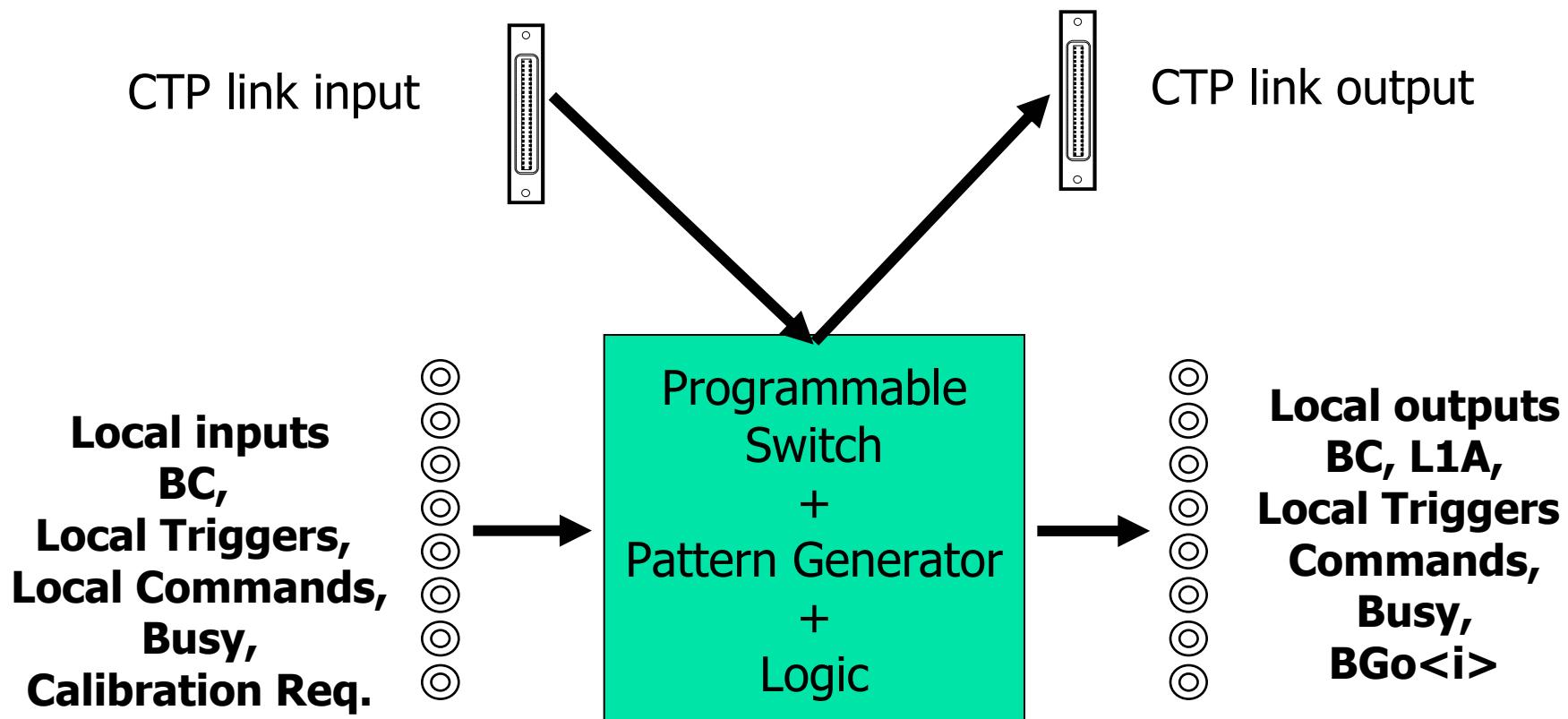
# Internal Pattern Generator

- An internal sequencer allows to generate any signal at any given time within a LHC turn
- Can be used in global mode to send to the CTP the 3-bit calibration request
- Can be used in stand-alone mode for generating any signal
  - Triggers, BGo<i>, …
- 1 MWord RAM
  - Read-out with BC → 26 ms time coverage
  - One shot or continuous mode
  - Can be started by ORBIT or Pre-Pulse or a VME access

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# L1A Path

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# Test Triggers path

14

# BUSY path

Global mode

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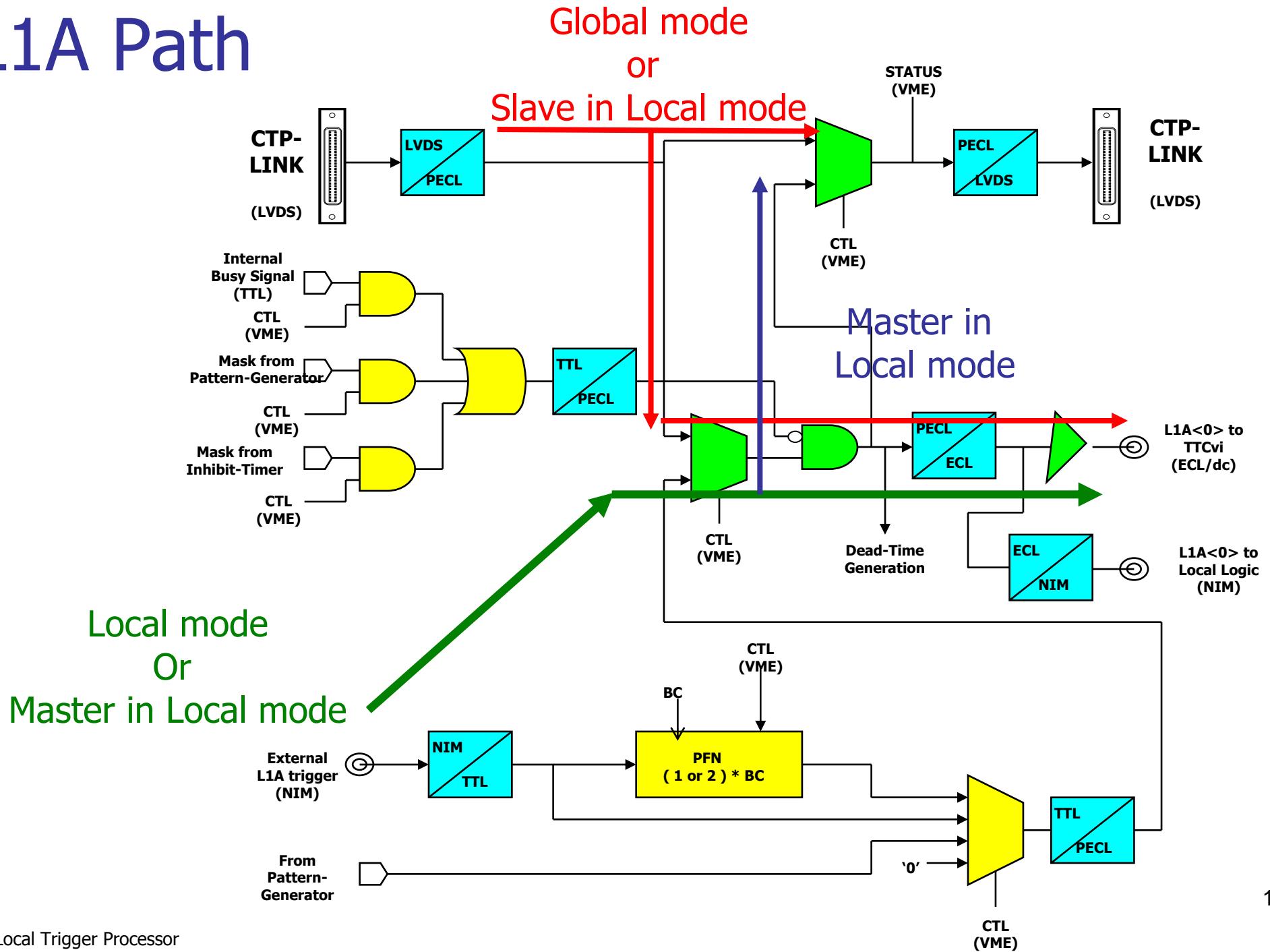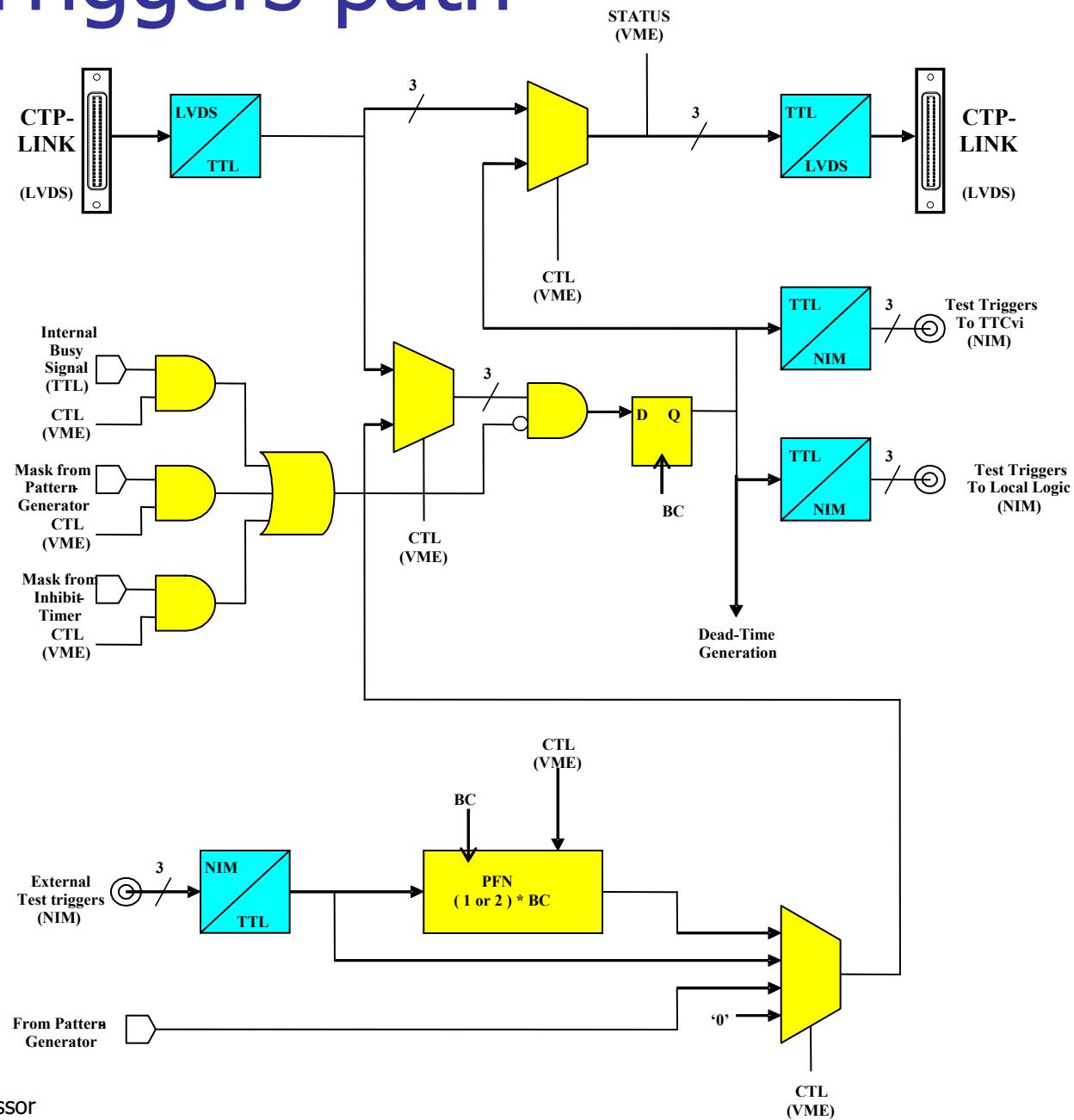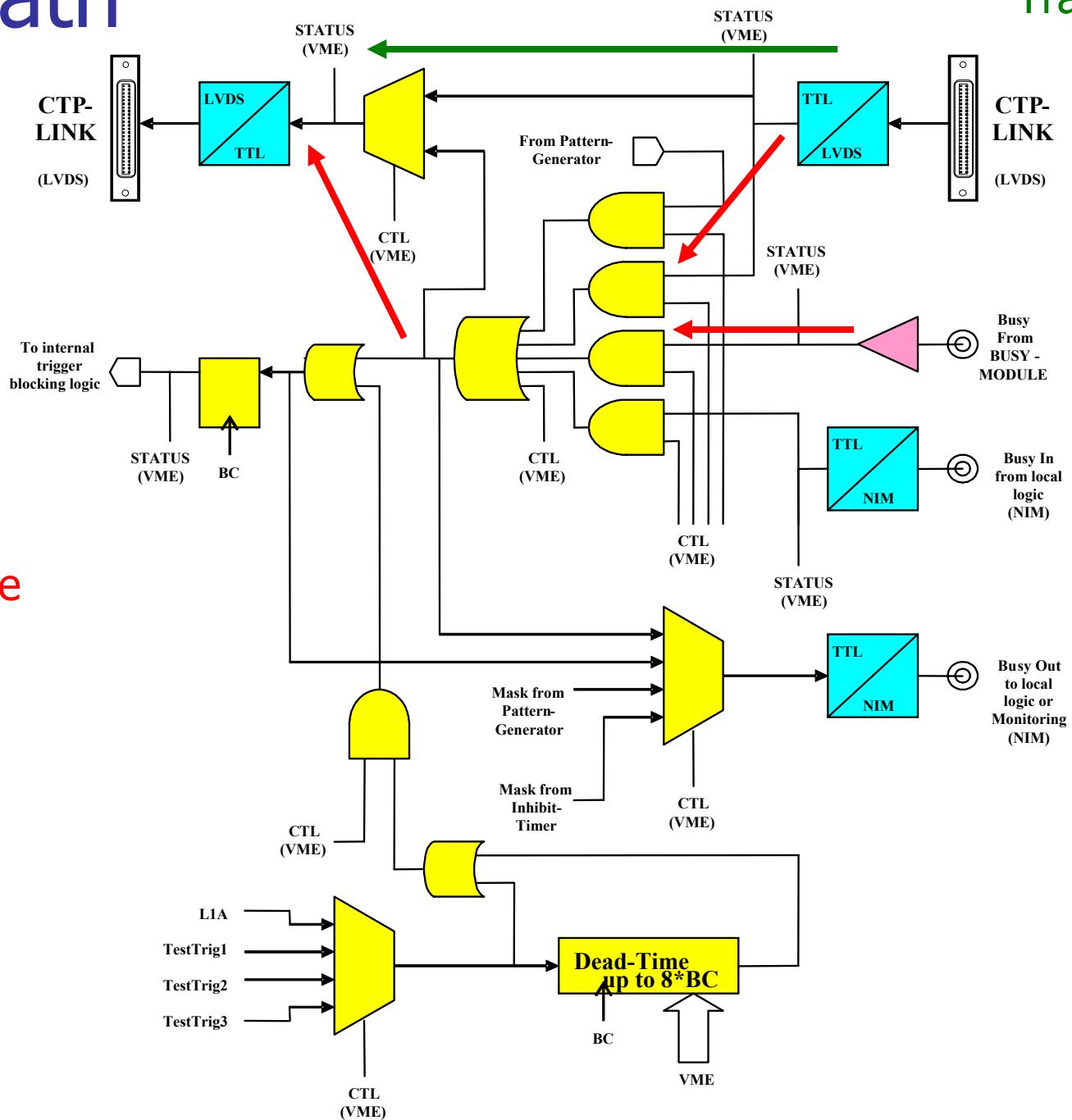
# Pattern Generator Block Diagram

SRAM
ADDR
Counter

SRAM
1 Mword x 16-bit
12 ns

BC Clock

Pattern SRAM
Data Port

SRAM
RD / WR / RUN
SEQUENCER
STATE MACHINE

ADDR CNT
Shadow reg.

CS*WR*ACR

CS*WR*SRAM

CSR

Read
VME
Data

CS*RD*<addr>

CS*WR*CSR

MODE
(CSR)

Output Pipeline
Register

RD Pipe-
Line Reg.

Predefined
Values

Pattern
Generator
Output

VME
Data
Bus

BC Clock

Fixed Value Reg

CS*WR*<addr">

16
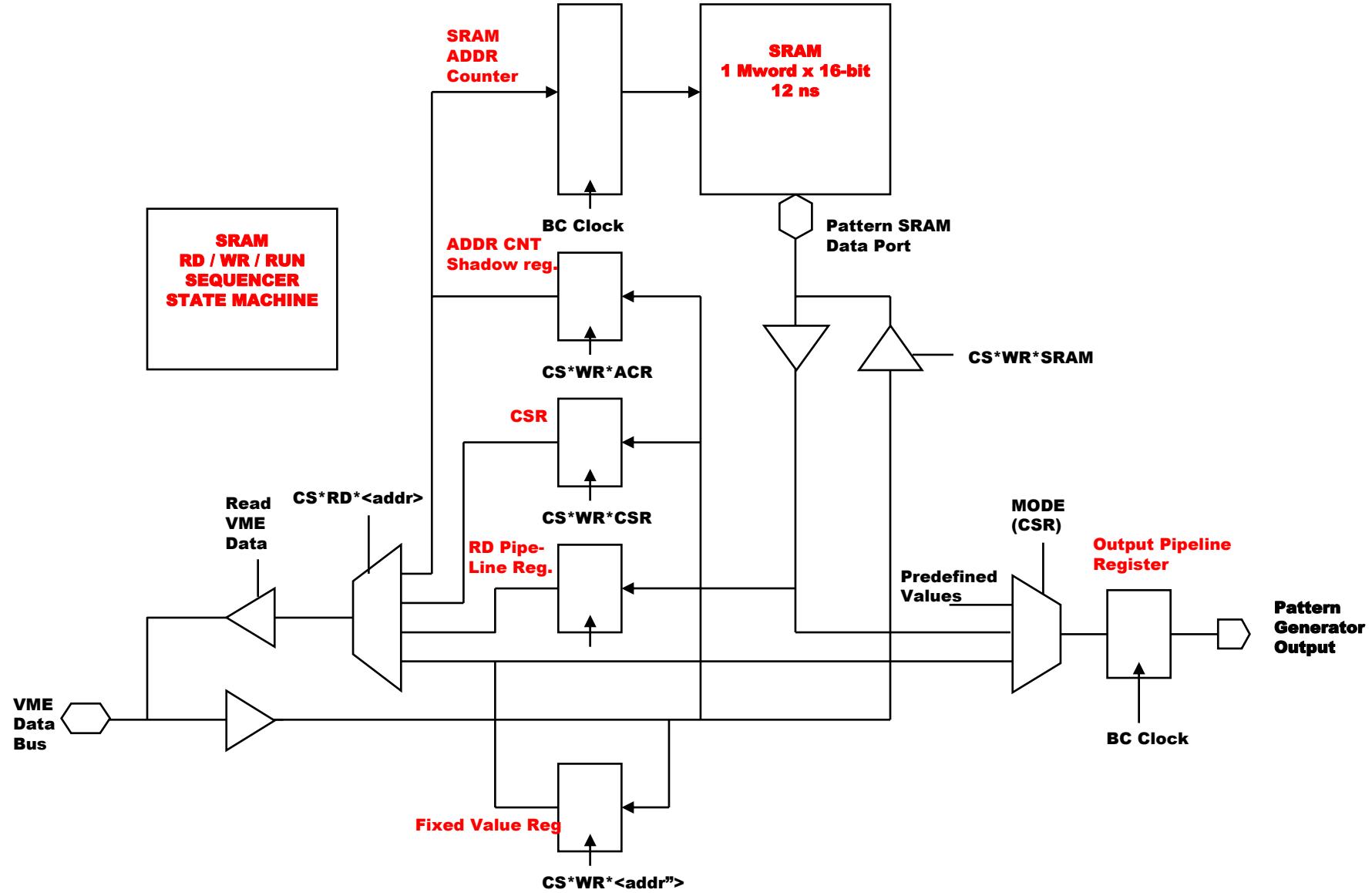
# Orbit path

**Global mode or Slave in Local mode**



CTP-LINK IN
(LVDS)

LVDS / PECL

**Master in Local mode**

CTL (VME)

STATUS (VME)

PECL / LVDS

CTP-LINK OUT
(LVDS)

TTL / PECL

ORBIT to TTCvi ECL/dc

PECL / ECL

CTL (VME)

TTL / PECL

CTL (VME)

PECL / NIM

ORBIT or TURN to Local Logic (NIM)

CTL (VME)

'0'

PECL / TTL

TTL / NIM

Divide by 3564

ORBIT 4 bit Counter/ "TURN" generator

RST by ECR

Start Timer

External Orbit (NIM)

System Clock (BC)

From Pattern-Generator/Sequencer

TURN number from VME

BC

Trigger/BGo Inhibit 12 bit Timer and Shadow register

Trigger/BGo Inhibit (4*BC wide)

Inhibit window position from VME

**Local mode or Master in Local mode**

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# Trigger Type path

# Technology

- LVDS on the CTP LINK
- Internal logic in PECL for BC, ORBIT and L1A
- 5V TTL remaining logic
- NIM and ECL for external connections to the TTCvi and local equipment
- CPLD's by ALTERA (ISP)

# Cable & Connectors

- CTP LINK Cable: 25 twisted pairs screened, max length 30 m
- Cable skew tests has been done – will wait for test-beam results – before deciding on final selection of cable brand
  - See EDMS document: ***ATL-DA-TN-0001***
- Local (short) cables, linking LTP's together, can be flat cables
- 50 pin 3M Micro Delta Ribbon connectors are used

# Logic implementation

## Firmware in 8 CPLD's

1. Pattern Generator Control and FSM
2. Pattern Generator Memory Address Counter
3. BC & ORBIT paths' CSR's, BC divider, Inhibit Timer, Event Counter
4. Trigger Selector MUX and CSR's for L1A and Test Triggers
5. Trig-Type Register File, CSR, Diagnostic FIFO ctl
6. B-Go[3..0] source selector and associated CSR's
7. BUSY and Dead-Time logic & selector, CSR, Calibration path, TURN counter
8. VMEbus Interface and Interrupter

# Status

- 6 LTP modules assembled
- Tested and debugged
- All functions works
- In system tests during October 2004 25 ns test-beam run
- Documentation in progress and partly entered in the EDMS
- EDMS Description: **_Atlas_LTP_** / EDMS Id: **_EDA-00508 v.0_**

# LTP Pictures

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