The OTIS TDC Chip

The OTIS is a 32 channel TDC chip developed at the University of Heidelberg. It will be used for the readout of the Outer Tracker Detector in the LHCb experiment. It features radiation hard layout techniques and is implemented in commercial CMOS 0.25 µm technology. The latest version OTIS 1.2 has been submitted for manufacturing in May 2004.

The TDC is based on a clock driven architecture and uses a DLL for time reference. Each channel's drift time data is written to a ring buffer to cover the trigger latency. After which the data is either transferred to the derandomiser buffer or overwritten. The buffer management as well as the trigger handling, data formatting and transmission to the subsequent DAQ stage is accomplished by a control circuit. Measurement results for the OTIS 1.1 are presented and together with the enhancements leading to OTIS 1.2.

The TDC Core

The TDC core, consisting of 64 stages DLU used as a time reference, the hit register and the decoder circuit, performs the drift time measurement. Therefore the DLL consists of a chain of voltage controlled delay elements through which the LHC clock signal is propagated clockwise.

The phase detector of the DLL then compares the original LHC clock and propagated clock. Depending on the phase between these two clock signals, a charge pump adjusts the delay of the DLL to exactly 1 clock cycle such that the LHC clock signal is propagated and clocked in-phase. In this state, clocked state, the hit reference signals for the drift time measurement can be obtained from the 64 delay elements providing a intrinsic resolution of 390ps. These reference signals are then used to latch the discriminated hit signals into the corresponding hit registers, forming the clocked driven architecture of the TDC. The hit register holds an image of the detector signal and through a subsequent decoder converts the hit position to a 6bit binary representation. The pre-pattern register is the interface to the following pipeline memory. In addition to the hit time it stores some status information and is further used to lead the subsequent stages with programmable test data. It also provides the test patterns for the self-test of the pipeline memory.

The DLU is a 256 bit wide shift register that stores the data for each channel. The DLL output is a clock signal with an intrinsic resolution of 75ps. If the hit reference signal is detected, the DLL is reset, the hit register is filled, and the DLU is clocked until the next hit or test data is available.

Pipeline memory and derandomiser buffer

Pipeline and derandomizing buffer are realized as arrays of dual port RAM cells. Their dimensions are 16x320bit wide and 48x240bit depth each, packed into the 32 channels. After powering the chip, it performs a power up reset. In addition it provides the 50ns and 75ns measurement hard layout techniques and is implemented in commercial CMOS 0.25 µm technology. The latest version OTIS 1.2 has been submitted for manufacturing in May 2004.

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The control algorithm performs the memory access required for trigger handling and data retrieval for readout. In addition it provides the 50ns and 75ns measurement hard layout techniques and is implemented in commercial CMOS 0.25 µm technology. The latest version OTIS 1.2 has been submitted for manufacturing in May 2004.

The OTIS 1.1 (Fig.3) is the latest full scale prototype chip and is available since February 2004. On a die size of 8mm x 8mm it implements all planned readout modes and modifications to fit LHCb specifications. Depending on the number of hit information) is followed by 32byte representing drift times of 48x240bit is large enough to hold the data of 16 triggers per bunch crossing of the hit. Obviously only the first hit of the 32 channels. While the lower 6bits are the measured fixed 900ns readout time required by the bunch crossing of the hit. The measured drift times are expected to follow the measured slightly off linear relation between hit position and drift time.

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