ALICE Trigger System

Features
Overall layout
Central Trigger Processor
Local Trigger Unit
Software
Current status

Features

• **3 decision levels**: L0: 1.2 μs, L1: 6.5 μs, L2: 88 μs
• **Parallel decisions** at each level – different groups of detectors (clusters) are reading out different events at the same time
• All the readout detectors (max. 24) are partitioned in up to 6 dynamically partitioned independent detector clusters
• **4 past/future** protection circuits for each decision level shared among all detectors, which protects the system against pile-up
• **50 trigger classes** (combination of input signals and trigger vetos) for each level
  • 24 L0 trigger inputs
  • 20 L1 trigger inputs
  • 6 L2 trigger inputs
Recall input

**BUSY signals**
Calibration requests

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**CENTRAL TRIGGER PROCESSOR**

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**DAQ (RORC)**
List of CTP events
Interaction record

**RoIP**
L1 data

**LTU/TTC**
Trigger outputs

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**ECS**
Control

**READOUT SUB-DETECTORS**

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**Trigger inputs**

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**Trigger outputs**
LTU/TTC

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**Trigger sub-detectors**

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**Trigger inputs**
Connections

CTP-LTU, LVDS

BC clock, coax. cable

RoI connections
CTP logic

- 50 programmable trigger classes for each level (AND of trigger inputs)
- Past/future protection circuits shared among all classes
- BUSY veto replaced by delayed decision from previous level on L1, L2 boards
- On the output, classes are combined (OR) to detector clusters
**CTP partitioning**

- 11 6U VME boards connected by special backplane
- 6 passive fan-in boards of 6U VME size (not shown on the picture) for:
  - L0 inputs (2)
  - L1 inputs (2)
  - BUSY inputs (2)
Context diagram of LTU

- Up to 4 TTC partitions configured by 1 SBC in 1 crate

- TTC partition controlled by LTU through its VME master interface and I/O connections

- GLOBAL (DAQ) mode: LTU is controlled by CTP

- STANDALONE mode: LTU is controlled by on-board CTP emulator

- The same front-end interface in both modes (L0, BUSY, FO)
LTU board
LTU block diagram
CTP emulation

• Together with selector, it allows **STANDALONE** mode operation, presenting the same FE interface as in **GLOBAL** mode
• 7 legal sequences
• Programs of max. 32 sequences are prepared in emulator memory. L1 and L2 data are fully programmable
• Sequence execution triggered by **Start signal** derived from BC scaled down, random generator, external pulser or software request
• **Error prone flag** enables programmable random or ‘on demand’ errors with chosen sequences in order to allow the FE electronics testing for error recovery
LTU sequences

Possible sequences:
L0
L0 - L1 - L2a  (DAQ)
L0 - L1 – L2r
PP
PP – L0
PP – L0 – L1 – L2a
PP – L0 – L1 – L2r

Errorneous sequences:
L0 - L2a
PP – L0 – L2a
PP – L0 – L2r

(a) Single pass
(b) Continuous loop
(c) Extended continuous loop
(d) Extended loop variation
LTU testing, just completed

• I/O tests – front panel connectors, backplane connector - I2C bus and Roll connections
• Functional tests with CTP emulator, the TTCvi was replaced by VME board with large sequential memory where data sent to B-channel of TTC were caught
**LTU software**

The control software for the LTU is ready. It is a subset of the software prepared during LTU development and testing. It is written in **Python/Tkinter** and **Tcl/Tk (GUI)** and **C (VME interface)**.

Platforms:
- VME SBC CCTVP110, **Linux/VMERCC or CCT driver**
- VME SBC Motorola, **AIX**
- PC + NI VME MXI cards with **Windows/VISA possible**

In addition to LTU control, SW supplies GUI for limited TTCvi control.

The same SW framework will be used with CTP boards.
Testbeam setup

Simplified block-diagram of LTU

- RoI output signals are used for feeding of the next LTU
- 2 BUSY inputs of 1 LTU can be used to combine BUSY from 2 detectors (common BUSY)
Testbeam setup

• Thanks to programmability of busy logic and LTU Mode, any LTU can become Master (CTP emulator) by simple reprogramming of LTUs

• If trigger is connected to all the LTUs, the exclusion of any detector is possible without recabling

• Advantage: all the three LTUs operate together, without additional hardware.
Current status

• 53 LTUs manufactured and tested, prepared to be used for tests with front-end electronics
• 3 LTUs are going to be used together in October combined Inner Tracking Subsystem test
• The ALICE CTP is being developed, first set of boards expected at the beginning of next year