Experience with Trigger Electronics for the CSC System of CMS


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CMS Detector Layout

CMS Endcap Muon System
Cathode Strip Chambers
Cathode Strip Chambers (CSC)

- 6-layer chambers
- Radial, trapezoidal cathode strips
- Azimuthal anode wires
- Induced charges on strips - precise $\phi$ coordinate
- Closely spaced wires - fast timing
- Wires ganged in groups of 5-16 for $r$ coordinate
Front-end Electronics
Requirements

Acquire data for muon hits

- **Cathode strips**: precise $\phi$-coordinate determination by interpolation of induced strip charges.
  - $\Delta Q/Q_{\text{total}} = 0.01$ per CSC layer
- **Anode wire groups**: precise timing for bunch crossing tagging and radial position determination.
  - 2 ns discriminator slewing

Generate primitives for Level-1 Trigger

- **Identify Local Charged Track (LCT) segments using cathode and anode signals**
CSC Trigger Elements

• **On-chamber:**
  - **AFEB** (Anode Front-End Board) discriminates anode hits.
  - **ALCT** (Anode Local Charged Track) receives anode hits, forms anode muon stubs, and sends trigger information to TMB.
  - **CFEB** (Cathode Front-End Board) contains cathode amplifiers and trigger comparator ASICs that discriminate and find cluster positions to $\frac{1}{2}$-strip accuracy.

• **Peripheral crate:**
  - **TMB** (Trigger MotherBoard) receives anode stubs and cathode hits, forms cathode muon stubs, correlates in time with anode stubs, and sends matched muon stubs to MPC. One TMB per chamber.
  - **MPC** (Muon Port Card) receives muon stubs from 9 TMBs, send the 3 highest-quality stubs to the SRSP on optical links.

• **Counting house:**
  - **SRSP** (Sector Receiver/Sector Processor) receives matched muon stubs from up to 4 stations, looks for tracks, and assigns muon track position and momentum.
Summer 2003 Beam Test Goals

1. Multi-chamber system test using preproduction versions of off-chamber electronics.

2. Re-verify triggering with high spatial resolution and bunch ID efficiency.

3. Check the high-rate system capability.
May-Sept. 2003 CSC Beam Test Setup at CERN X5A

- **Track Finder Crate**: TRIDAS
- **Peripheral Crate**: 2 DMB, 2 TMB, 1 CCB, 1 MPC
- **TTC crate**: DAQ Data
- **FED crate**: 1 DDU
- **PC**:

2 CSC’s, all on-chamber boards

Up to 80K events read out in 2.6s spill
Comparator ASICs

- Compare pulse heights from adjacent strips to find cluster to \( \frac{1}{2} \)-strip
- 15000 16-channel ASICS on CFEB boards (OSU)
- Production complete

ALCT Boards

- Finds tracks among anode hits, stores data for readout
- XCV600 and XCV1000s used for main FPGA
- 468+spares boards of 3 types (288-, 384-, 672-channel)
- Production complete (making more spares)
Peripheral Crate: Trigger Motherboard

- Generates Cathode LCT and matches ALCT with CLCT
- 9U x 400 mm form factor
- Uses XC2V4000 for main FPGA
- 32 pre-production boards have been built (CMS uses 468)
Track Finder Crate: SP2002 (Main Board)

12 Used in CMS System

Receiver:

- Optical Transceivers
  - 16 x 1.6 Gbit/s Links
- TLK2501 Transceiver

Data conversion:

- Phi Global LUT
- Eta Global LUT
- Phi Local LUT
- Front FPGA

VME/CCB FPGA

To/from custom GTLP back-plane
Muon Event Display
(2 chambers, CSC1 tilted)
• 6 layers * up to 112 wire groups per layer (672 channels)
• Hits delayed in 2ns steps to optimum phase for timing, then recorded every 25 ns bunch crossing (BX).
• In each anode pattern, pre-trigger when e.g. 2 layers receive hits.
• Confirm pre-trigger with e.g. 4 or more layers with hits within a pattern.

<table>
<thead>
<tr>
<th>Anode Collision Muon Pattern</th>
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<tr>
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<td><em>xx</em>_</td>
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• ALCT board outputs up to 2 ALCTs per chamber/BX. Choose those having maximum number of layers.
• Logic is fully programmable: plenty of adjustments are allowed.
2003 Synchronous Beam Structure

48 bunches
25 ns bunch spacing
bunch width 3-5 ns

1.2 \mu s

23 \mu s

SPS orbit period

Structure repeats during 2.6 s spill length
Structured Beam Bunch Structure and ALCT Delay Tuning

Expect muons in 48 out of 924 bx verified by CLCT BXN from data

BX efficiency vs. ALCT delay setting 0-31 ns
BX Distributions With Optimal Anode Delays

Note logarithmic scale

Cathodes:
- Data mostly in 3 BX (no fine time adjustment possible)

Anodes:
- Data 98.7% in 1 BX
### Trigger Primitive Algorithms: Cathodes

- **6 layers** * up to 80 wire groups per layer (480 channels)
- Form “di-strips” by OR’ing 4 adjacent ½-strip bits.
- In each cathode pattern, pre-trigger when 2 layers are hit, confirm pre-trigger when 4 layers are hit.
- Simultaneous ½-strip patterns for high-$P_T$ muons, di-strip patterns for low-$P_T$ muons:

<table>
<thead>
<tr>
<th>Pattern 1</th>
<th>Pattern 2</th>
<th>Pattern 3</th>
<th>Pattern 4</th>
<th>Pattern 5</th>
<th>Pattern 6</th>
<th>Pattern 7</th>
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**TMB Patterns**

<table>
<thead>
<tr>
<th>Layer 0</th>
<th>Layer 1</th>
<th>Layer 2</th>
<th>Layer 3</th>
<th>Layer 4</th>
<th>Layer 5</th>
</tr>
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<tbody>
<tr>
<td>x___    x__    x___    x__    x__    x__    x__    x__</td>
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- **CLCT board outputs up to 2 CLCTs per chamber/BX. Choose those having:**
  1. Maximum number of layers.
  2. ½-strip patterns preferred over di-strip patterns.
  3. Straightest pattern.
- **Logic is fully programmable: lots of adjustments are allowed.**
Comparator $\frac{1}{2}$-strip ID

- Particles tracked using precision charge readout on cathodes
- Position difference between center of $\frac{1}{2}$-strip and the fitted track:
Cathode Comparator Behavior

- Source of imperfect ½-strip resolution due to imperfect comparators
- Resolution ~5 ADC counts (2.9 fC)
- Offset ~8 ADC counts (4.6 fC)
• At low cluster charge, $\varepsilon$ drops due to too little charge for comparison
• At highest cluster charge, $\varepsilon$ drops due to slow saturation of amplifiers
CLCT Position Correlations

- Relative position of CLCTs from Chamber 2 vs. Chamber 1
- N.B. Chamber 1 is vertically higher than Chamber 2 (thus the offset in position).
Simultaneous searches for di-strip patterns (low-Pt) and half-strip patterns (high-Pt)

Simulate low-Pt by tilting the chamber (phi)
Quality = Layers-3

- HQ
- straight
- 1/2-strip

1/2-strip patterns

- HQ
- bent
- 1/2-strip

2-stripe patterns

- HQ
- bent
- 2-stripe

$\phi = 0^\circ$

$\phi = 5^\circ$

$\phi = 20^\circ$
Expected LCT rate at LHC is $97 \text{ KHz/chamber (ME1/1)}$ (CMS note 2002-007)
• TMB anode-cathode matching is done primarily by timing.
• If 2 ALCT and 1 CLCT or vice versa are found, two matched stubs are reported by copying the single stub view.
• If 2 ALCT and 2 CLCT are found, they are matched by the number of layers.
• Trigger hits and stub information are all read out to the DAQ system for 16 BX, starting 2 to 5 BX before the first hit.
Given an ALCT*CLCT matched stub in chamber 1, the efficiency for a matched stub in Chamber 2 can be found. Using a $\pm 5$ strip and $\pm 3$ wire-group tolerance:

- $\varepsilon=97.9\%$ in one BX
- $\varepsilon=98.9\%$ in two BX (correct BX or one after)
- $\varepsilon=99.1\%$ in three BX (correct BX $\pm 1$)

as determined from logged Track-Finder data
Conclusions

• This was the first time the CMS endcap muon group demonstrated a complete electronics chain from chamber to muon tracks using pre-production electronics.
• The CSC trigger (and DAQ) system performed extremely well at the 2003 test beam.
• A few hardware problems were found (e.g. optical link clocking) and have since been addressed.
• Further “system integration” tests are underway at 2004 test beams at CERN.