Realization of the ALICE SSD EndCap Modules

(For the ALICE Collaboration)

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Outline

• Introduction ALICE ITS.
• Introduction EndCap, Architecture.
• ASIC’s : ALCAPONE & ALABUF.
• Prototyping.
• Production tests of pcb’s & ASIC’s.
• Conclusion.
ALICE ITS SSD EndCap

- SSD: 2 layers of double sided Si detectors, total 72 detector ladders.
- Each ladder 2 EndCap’s.
- Each EndCap controls 11 to 14 detector modules.
- A module has 1 Si. Strip detector and 2 hybrides with 6 HAL25 front-end chips.
- Hybrides at different bias potentials.
EndCap Constraints

- Radiation Tolerant max. \( \sim 50 \text{krad} \) (+SEE prob.)
- Low Power : max. 10W per EndCap
- Small size : 7 x 7 x 5 cm
- Protect Front-end against Latch-up
- Control 11 to 14 double sided detector modules
- Provide good separation for detector bias potentials
- Connect to DAQ system @ GND potential.
EndCap Architecture

Interface Card (1x)
- Control ASIC's
- Interface buffers & control
- CMOS & LVDS
- N-side buffer & control
- ALCAPONE
- ALABUF
to 28 hybrids

Supply Card (7x)
- P-side supply & buffers (14x)
- ALCAPONE

DAQ & CONTROL
- all LVDS
- control
- Error & JTAG
- analogue data

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Control chip in 0.25µm CMOS

Functions:

- Shunt regulator for 2.5V
- Progr. Power regulator 2.1-2.8V with over current protection
- Progr. readout control
- Progr. JTAG slow control
- LVDS & CMOS signal buffering
- inputs are compatible for AC-coupling (JTAG & LVDS)
- 4 input, 8bit ADC. 1 current output for NTC.
AC coupling of analogue signals

- Specifications to check:
  - Position resolution
  - Amplitude distortion
  - Additional noise
- Check for different time constants and occupancies
- Monte Carlo simulation of detector signals
- Baseline fluctuations due to AC coupling converted to noise value.

Baseline fluctuation $\sigma_{bl} = 107e$, mean = 110e
Electronic noise $\sigma_{el} = 400e$, mean = 0

Conclusion:
C-couple 560nF
**ALABUF2**

**Analog buffer & Multiplexer Specifications:**

- 2 amplifier2 with 2 inputs
- Fixed differential gain 5.66
- Power: on: 91 mA  
  off: 10.4mA
- Maximum output: 1.85V  
  @ <1% non linearity error
- Settling time <20ns
- Noise: ~60 electrons @ input
- Vref output for front end chip: 1.2V ±5%
- All inputs are compatible for AC-coupling.
EndCap Control, JTAG & Power

Supply Card
- ALCAPONE 0
- ALCAPONE 1
- ALCAPONE 2
- ALCAPONE 3
- ALCAPONE 4
- ALCAPONE 5
- ALCAPONE 6
- HYBRID: 6xHAL25

Interface Card

Supply Card

next SupplyCard max. 7.

P side of detector modules
N side of detector modules

Power on
JTAG On

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**Module Readout**

- Serial readout; one ADC for each double sided detector.
- All detector modules are readout at the same time.

Readout clock @10MHz
EndCap Prototyping

1. Verify temperature behavior of construction with “dummies”.
2. Start ASIC design in 2000.
3. Calculate effect of AC coupling in analogue data path.
4. All test controls & stimuli programmed in one FPGA (ALTERA).
   ➢ Controllable & programmable via JTAG from PC with LabView.
   Very flexible.
5. Test board for one chip. All I/O’s to connectors, goal:
   ➢ Build full module out of ALCAPONE- and ALABUF test boards.
6. Test Functionality & performance of both ASIC’s.
7. Build EndCap and connect detector module; test Functionality.
8. Submission of final design of both chips.
9. Use proto EndCap module in beam-test and verify Performance of the whole EndCap. This is last step with packaged chips.
10. Start pre-production of real size (=small) EndCap pcb’s. Pre-series checked in a next beam-test (October 2004).
11. Production for 200 InterfaceCards & 1200 SupplyCards has started.

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Components:
- Cable Card (FR4); all cables are soldered.
- Interface Card; aluminum + kapton
- 7 Supply Cards; aluminium + kapton
- Connectors 0.5mm pitch
- Base plate (FR4)
- Stainless steel plate; soldered stainless steel tube (18ºC).
SupplyCard

4x ALCAPONE1 + ALABUF2

room temp. +4°C with expected load.
+10°C with ~3x exp. load.
PCB production tests

- **JTAG Boundary Scan Test** for connectivity of wire-bonds.
- Check other functions via JTAG bus and measure results via PC
- All wire-bonds are tested.
- All connector I/O’s are tested.
- Basic values are logged.

**DUT**: Supply Card

**Interconnect** (exchangeable)

**ALTERA pcb Test controller**

**Load pcb & measure**

**control & measure**

**PC**

**JTAG**
PCB production test setup
Chip & Wafer Test setup

- LabView controlled.
- Measurements via:
  - Oscilloscope,
  - Power supplies (load),
  - multi I/O PCI card.
- Test patterns from FPGA
- Software controlled Probe station, max. 3 retries / chip
- ~ 9 hours/ wafer (720 chips)
Wafertest: ALABUF2

**Test software:**
- All test Data saved by LabView in **XML** format.
- XML “filter” to select specific data.
- Post processing using MathCAD.
- First DC connectivity (3 retries).
- Complete performance test:
  - DC: power, offset, linearity, gain
  - AC: AC-coupled control inputs, noise, pulse response, supply range.
- **Yield over 6 wafers : 84.8%**.
- Optimal contact resistance ~2.6Ω.
- Lower gain measured after termination.
- Difficulty with 8” wafer: bad vacuum spread over chuck.
Conclusion

• Not possible without the use of ASIC’s
  • size, radiation tolerance, costs.
• Robust system based on AC coupled signals.
• The use of the JTAG bus for controls AND connectivity tests speeds up production test.
  Preparation of connectivity test is very time consuming.
Finished.
Irradiated ALABUF1

- Dose: 500 krad Co$^{60}$ source
- No significant degradation measured

![Diagram](image)

**Fig. 7. DC transfer characteristic AVout(AVin) before (red points) and after (blue points) the irradiation.**
## AC coupled LVDS receiver

<table>
<thead>
<tr>
<th>Specifications</th>
<th>Details</th>
</tr>
</thead>
<tbody>
<tr>
<td>Power consumption (simulation)</td>
<td>429uA 2.5V</td>
</tr>
<tr>
<td></td>
<td>=1.073mW</td>
</tr>
<tr>
<td>Nominal data rate</td>
<td>10MHz</td>
</tr>
<tr>
<td>Maximum data rate</td>
<td>50MHz</td>
</tr>
<tr>
<td>Common mode range of operation</td>
<td>1.25V±0.5V</td>
</tr>
<tr>
<td>Single power supply (VDD)</td>
<td>2.5V</td>
</tr>
<tr>
<td>Differential swing in DC-coupling mode.</td>
<td>&gt;100mV</td>
</tr>
<tr>
<td>DC-hysteresis</td>
<td>±25mV</td>
</tr>
<tr>
<td>Precision of the input voltage level setting in AC-coupling mode.</td>
<td>( V_H - V_L =350mV \pm 70mV )</td>
</tr>
<tr>
<td></td>
<td>( (V_H + V_L)/2 =1.25V ± 150mV )</td>
</tr>
<tr>
<td>Differential swing in AC-coupling mode.</td>
<td>&gt;220mV</td>
</tr>
<tr>
<td>Enable/disable functionality</td>
<td>yes</td>
</tr>
</tbody>
</table>
• 2 channel analogue buffer
• diff. gain 5.66
• power:
on-91mA
off-10.4mA
• max 1.85V
outp. <1% non lin.
• settling <20ns
• noise:
@ input 68µV