Readout Electronics of the ATLAS Muon Cathode Strip Chambers

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Abstract

The ATLAS muon spectrometer will employ cathode strip chambers (CSC) to measure high momentum muons in the extreme forward regions. Due to the severe radiation levels expected in this environment, the on-detector electronics are limited to amplifying and digitizing the signal while sparsification, event building, and other tasks are performed off-detector.

We report on the first tests of the complete readout chain from chamber to the off-detector readout driver (ROD).

I. INTRODUCTION

The CSC system is designed to measure high momentum muons in the extreme forward regions (pseudorapidity $2.1 < |\eta| < 2.7$) of the ATLAS detector [1]. Its principle of measurement is to determine the hit coordinates by interpolating charge deposited on adjacent strips. Multiple layers of strips allow for tracks to be formed from these hits.

In the initial configuration of ATLAS, a total of 32 chambers are arranged in two end-caps. A chamber has four identical layers, each providing a precision measurement in the (radial) bend direction and a coarser measurement of the transverse (azimuthal) coordinate. Each chamber has a total of 768 precision coordinate strips and 192 transverse coordinate strips. The precision strips have a readout pitch of 5.08 mm and a strip capacitance of 20–50 pF, depending on strip length which varies due to the chamber's trapezoidal shape. At an expected strip hit rate of up to 650 kHz a signal-to-noise ratio of 150:1 is required to obtain a single plane resolution of ~ 60 μm in the bending direction.

Because of the severe radiation levels anticipated for the CSC environment, a minimum of the electronics will be located on the detector. The on-detector electronics amplifies and shapes the cathode strip signals, and stores the pulse height information during the first-level trigger latency. When a trigger is received, four consecutive time samples are digitized and transmitted via fiber-optic links to the off-detector electronics. Sampling and digitization are performed on-detector but are controlled by the off-detector electronics. The ROD processes the samples in two stages. The sparsification stage suppresses hits below threshold and hits not associated with the current bunch crossing. The rejection stage identifies tracks and removes isolated background hits. The remaining data are formatted and sent to the ATLAS Trigger/DAQ System for further processing.

II. THE CSC READOUT ELECTRONICS

A. The on-detector electronics

The CSC on-detector electronics [2] consists of two layers of amplifier-storage module (ASM) boards. Each strip is connected to a preamplifier and shaper circuit, implemented as a radiation-tolerant custom ASIC, which forms a bipolar pulse with a 140 ns shaping time to mitigate pile-up effects. The shaped pulses are sampled every 50 ns, and the analog pulse height information is stored in a custom radiation tolerant CMOS switched capacitor array (SCA) for the duration of the level 1 trigger latency, which is estimated to reach 125 bunch crossings in the worst case sce-

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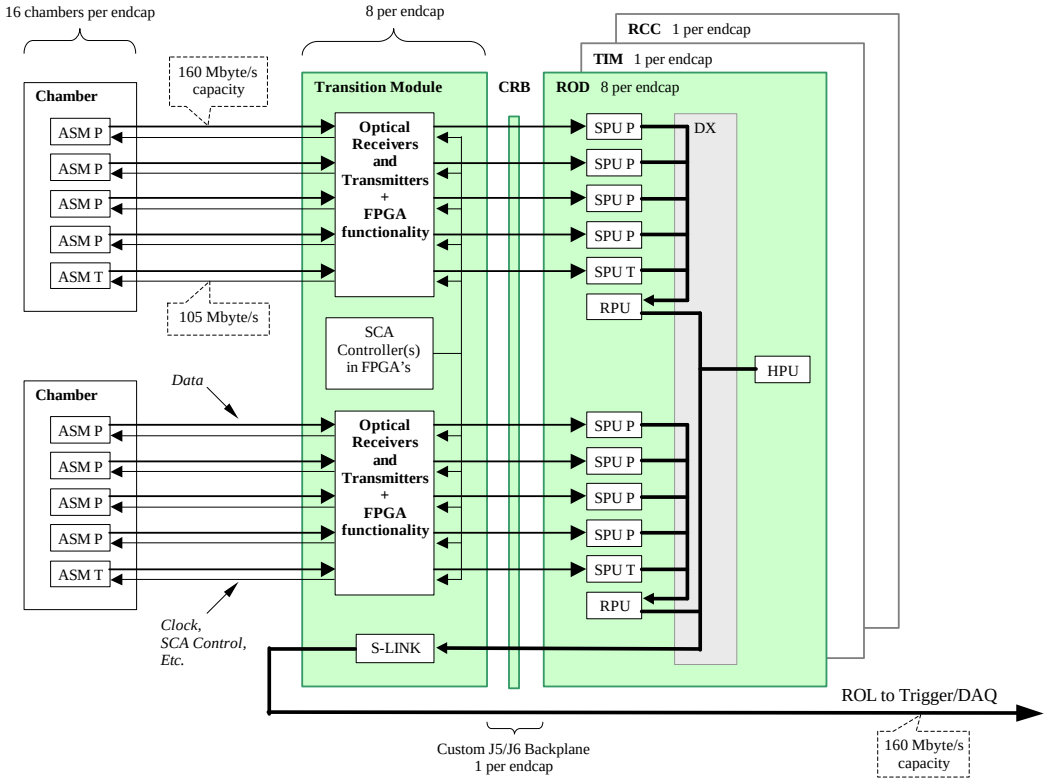

Figure 1: Schematic of the CSC ROD

nario. The SCA provides an effective pipeline depth of 288 bunch crossings. Following a trigger, all channels of the SCAs are time multiplexed and digitized using 12-bit Analog Devices AD9042 ADCs. Custom ASICs multiplex the data from 16 ADCs to two G-Link serializers configured to operate with 16-bit input words at 40 MHz single frame rate.

Eight preamplifier/shaper ICs supporting a total of 96 channels reside on a printed circuit board (ASM-I). Two ASM-I boards piggyback on one ASM-II which contains the 16 SCAs, ADCs, multiplexors serving 192 channels total, and two fiber optic G-Link transmitters. One HP-1024 fiber optic receiver handles incoming control signals from the ROD. A total of five such ASM-I/ASM-II combinations are needed to read out one chamber – four for the precision coordinate strips and one for the transverse coordinate strips from all four layers. Four ASM-I/ASM-II configurations are attached to the narrow edge of the chamber and share a common Faraday cage and cooling fixture. The transverse strip ASM-I/ASM-II package is attached to the broad side of the chamber.

B. The off-detector electronics

The off-detector electronics [3] consists of readout drivers (RODs) coupled with transition modules. Each ROD handles the incoming data of two chambers, i.e. from 10 ASM-II boards (Fig. 1). It also controls the ASM-II, in particular the readout of the SCA when a trigger has been received. In addition the ROD provides data monitoring functionality. The transition module contains all opto-electronics for readout and control of the ASM-II boards as well

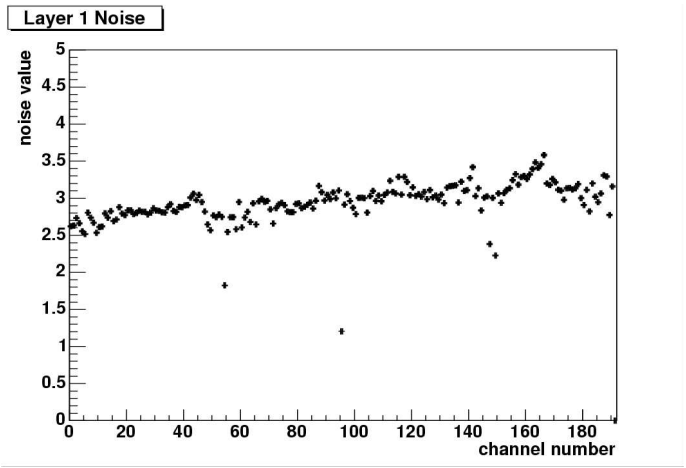

Figure 2: RMS noise, in ADC counts, for one CSC layer. The slope towards higher channel numbers is consistent with the increased strip capacitance which grows with radius.

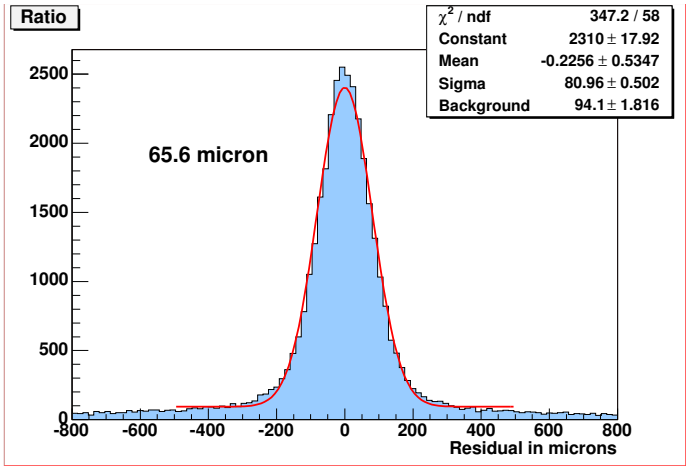

Figure 3: Single layer resolution determined from muon beam data taken with one chamber, using only precision coordinates.

as for sending the processed data to the data acquisition system. It connects to the ROD directly via a custom backplane.

The RODs are housed in a 9U VME crate. A timing interface module (TIM) in each VME Crate distributes clock and control signals to the RODs. The crate also contains a ROD crate controller (RCC), an off-the-shelf VME single-board computer which, by communicating with the ATLAS Trigger/DAQ System, is responsible for starting and stopping data acquisition and for sampling events from the CSC detector for monitoring purposes.

While most of the ROD's control functionality is implemented in field programmable gate arrays (FPGAs), processing of the 160 Mbyte/s data stream from the ASM-II is handled by digital signal processors (DSPs).

A 300 MHz Texas Instruments TMS320C6203 DSP with 2 MBytes off-chip memory supported by two Xilinx Spartan II FPGAs for interfacing are grouped together on a small plug-in module. The ROD has 13 such modules, 10 for sparsification, two for background rejection, and one host module (HPU) which supervises the others and communicates with the RCC via the VME bus.

The ten sparsification processing units (SPUs), one per ASM-II, reduce the raw data stream by suppressing strip signals below a threshold cut and by rejecting signals outside the timing window correlated with the trigger. The four consecutive time samples retrieved from each strip provide pulse shape information, i.e. charge and time. The SPU applies calibration constants to the data, organizes the hits into clusters and determines their peaking time.

The output of each SPU is sent to the rejection processing unit (RPU) via the data exchange subsystem (DX). The RPU receives data from all four layers of the chamber. It builds tracks from the clusters identified by the SPUs. Isolated clusters are rejected. The remaining data are transferred via the DX and the 160 Mbyte/s readout link to the readout buffers in the ATLAS Trigger/DAQ system, where the data is stored during subsequent level 2 trigger processing and event building.

III. Performance

The complete readout chain from chamber to ROD has been tested with cosmic rays, and with >100 GeV muons at CERN's X5/GIF beamline. High trigger rate readout was exercised using a pulser trigger.

For these tests one chamber was fully equipped with shielded and cooled ASM-I and ASM-II boards, read out via fiber optic links and a transition module to a ROD prototype. The latter was populated with four SPUs and one HPU. The SPUs reordered the data but did not sparsify, i.e. every channel was read out. Instead of transporting data via DX, the HPU was programmed to build the events and send them out to a standalone data acquisition system connected by means of a PCI-VME interface. In this mode, the event data was written into HPU memory, and later transferred to the VME bus. While this limited the number of events per run, it facilitated realistic performance tests of the system from cham-

ber to ROD.

Noise levels and single layer resolution were found to be close to expectations. The RMS noise was measured at $\sim$3 ADC counts, equivalent to $\sim$0.5 fC (Fig. 2). A track resolution of 66 μm was determined in the beam test with the chamber at nominal high voltage (Fig. 3). The system tests revealed no bandwidth bottlenecks. Simultaneous readout of four precision layers was achieved at trigger rates of up to 106 kHz without affecting noise or resolution.

IV. Conclusions

The CSC readout electronics have been tested in a near-final configuration with cosmic rays as well as a muon beam. Noise, chamber resolution, and overall performance at up to 100 kHz sustained trigger rate were all within expectations.

V. Acknowledgements

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VI. References

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