



A flexible stand-alone testbench for facilitating system tests of the CMS Preshower

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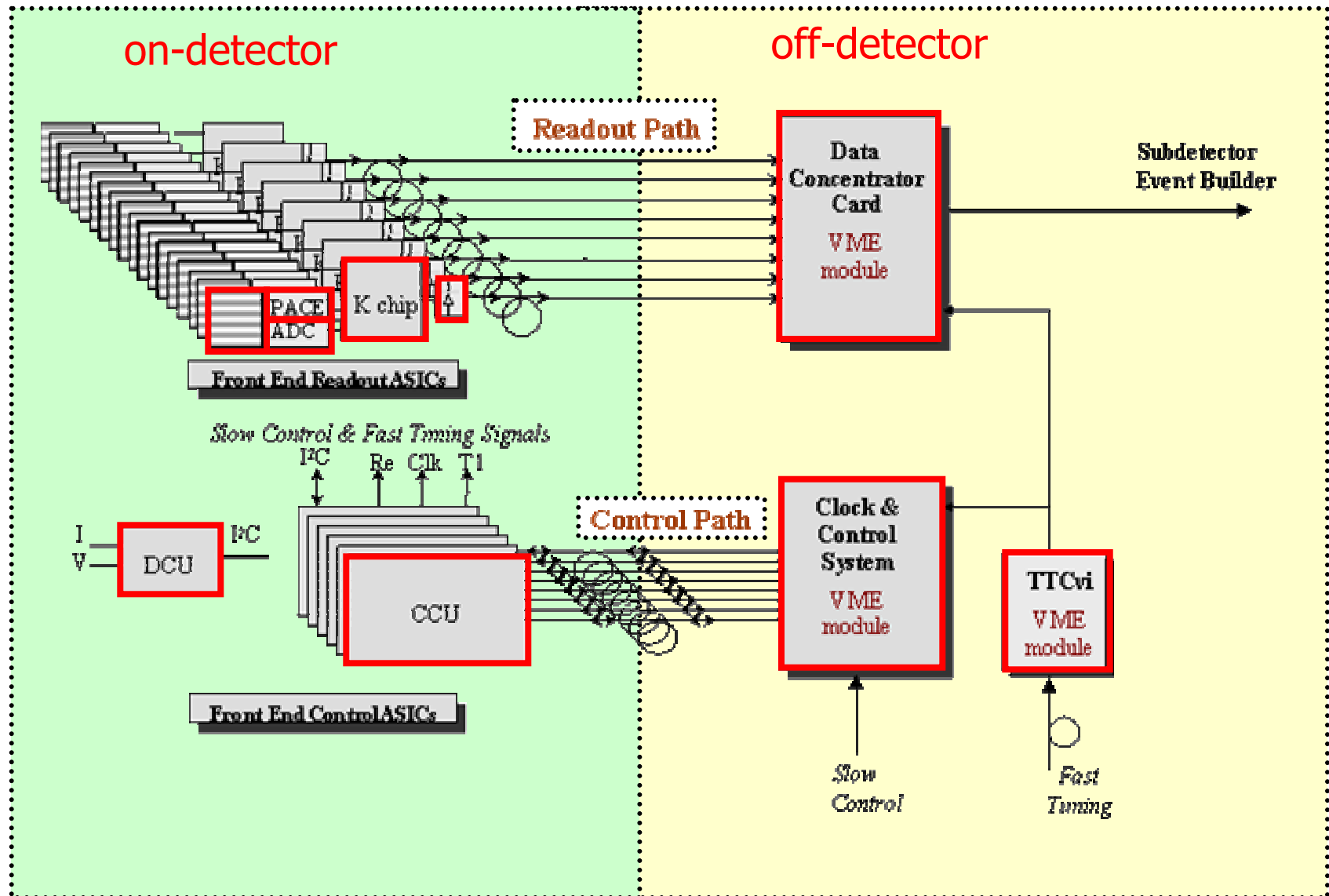
Presentation Overview



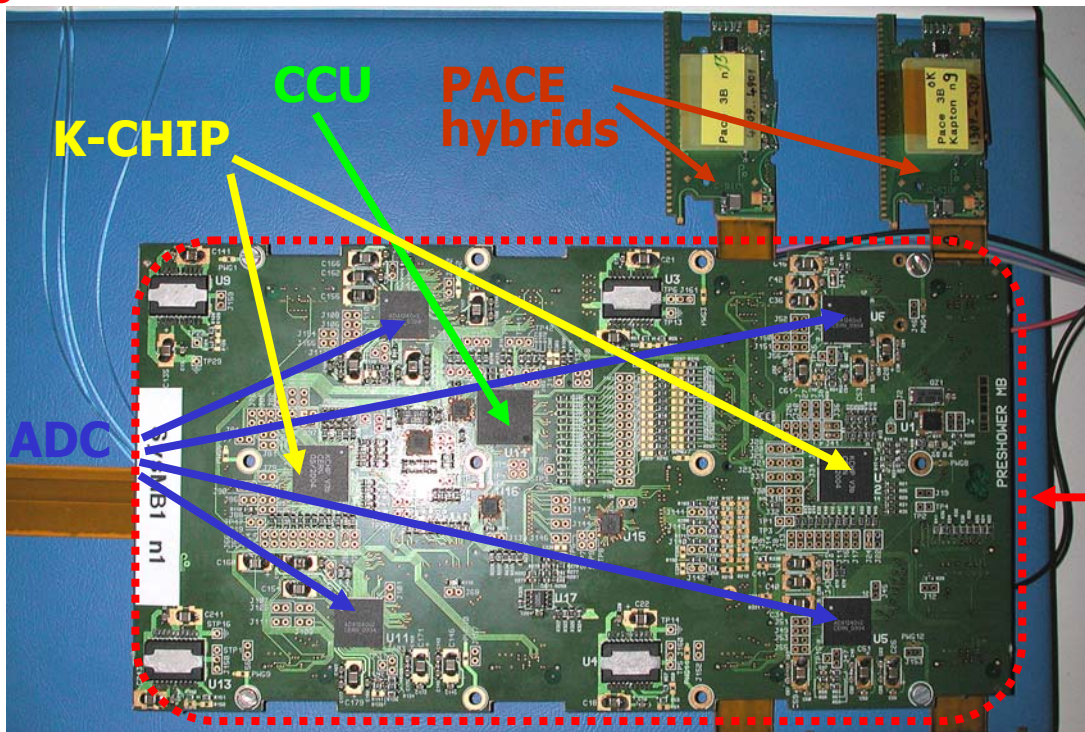
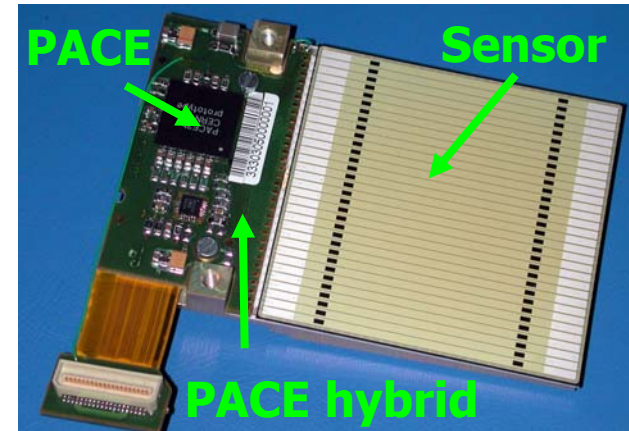
- Introduction
- Testbench
 - Motivation
 - Implementation
 - Features
 - Software
 - System Tests
 - Other Uses
- Summary/Conclusions



INTRODUCTION – Preshower Architecture



μ module \longrightarrow



System board



TESTBENCH - Motivation (1/2)



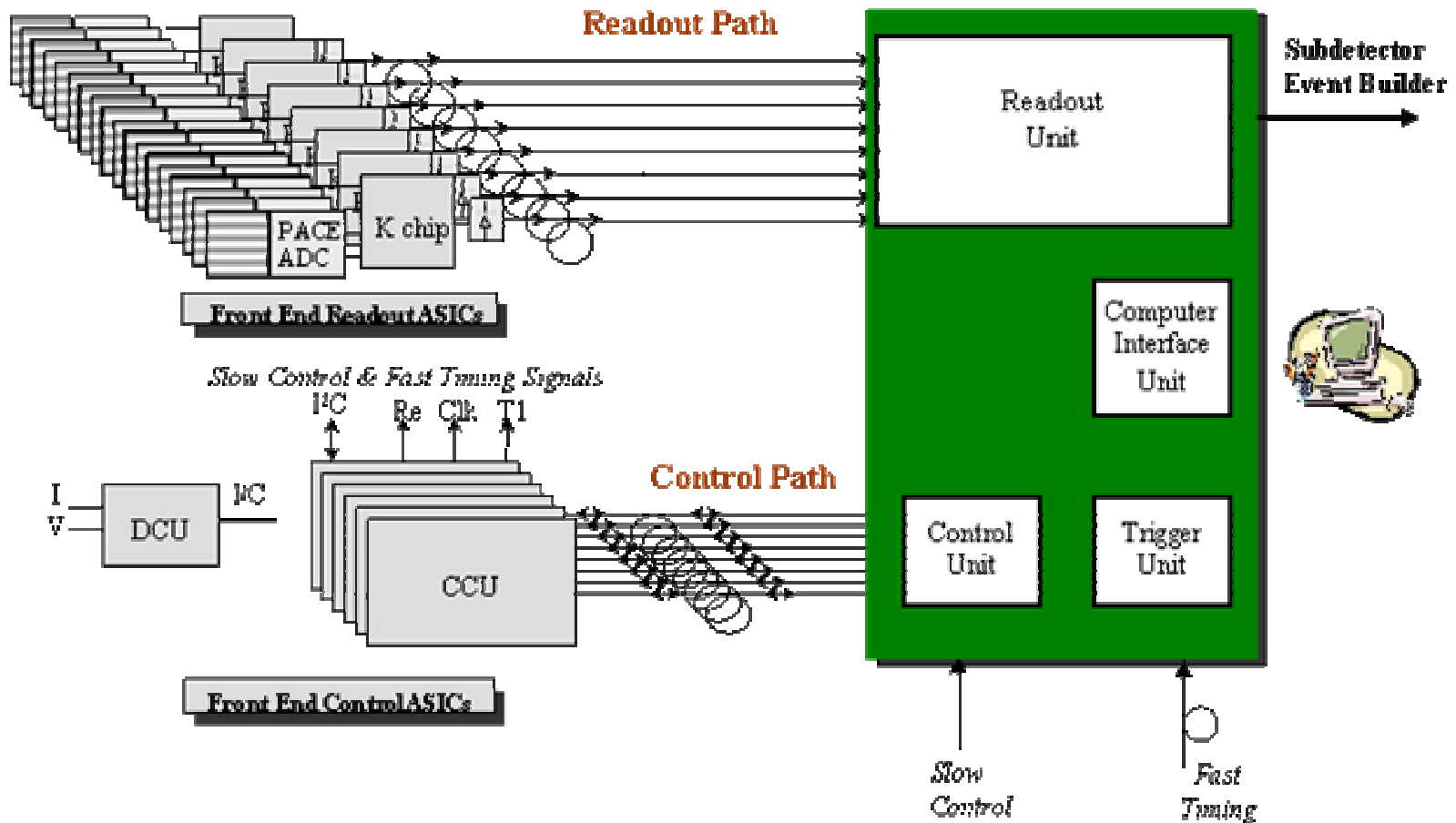
Main Purpose: Evaluation of system board

Requirements

- ☞ Clock & control system
- ☞ Flexible Trigger Generation system
- ☞ Readout system

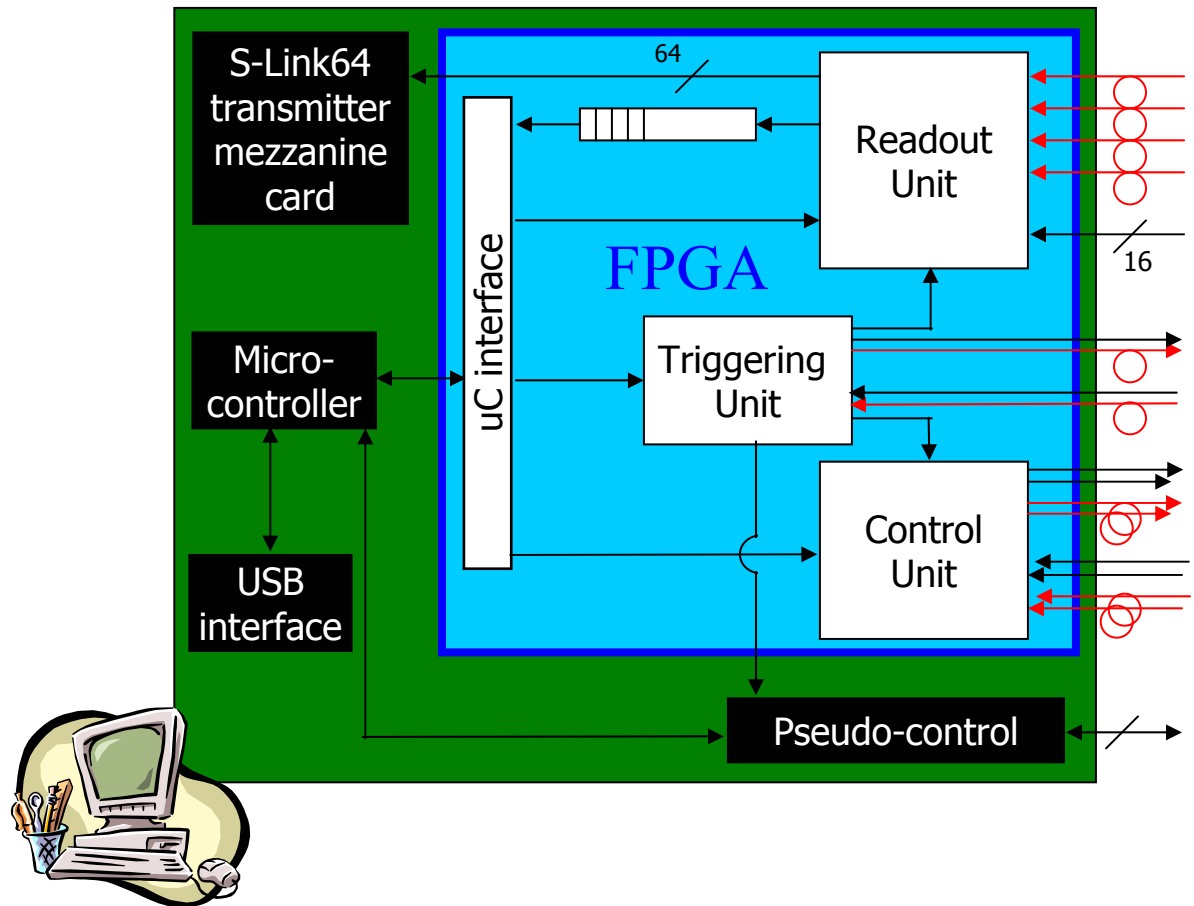
Availability (Q3 2003)

- ☑ FEC
- ☒
- ☒
- ☒





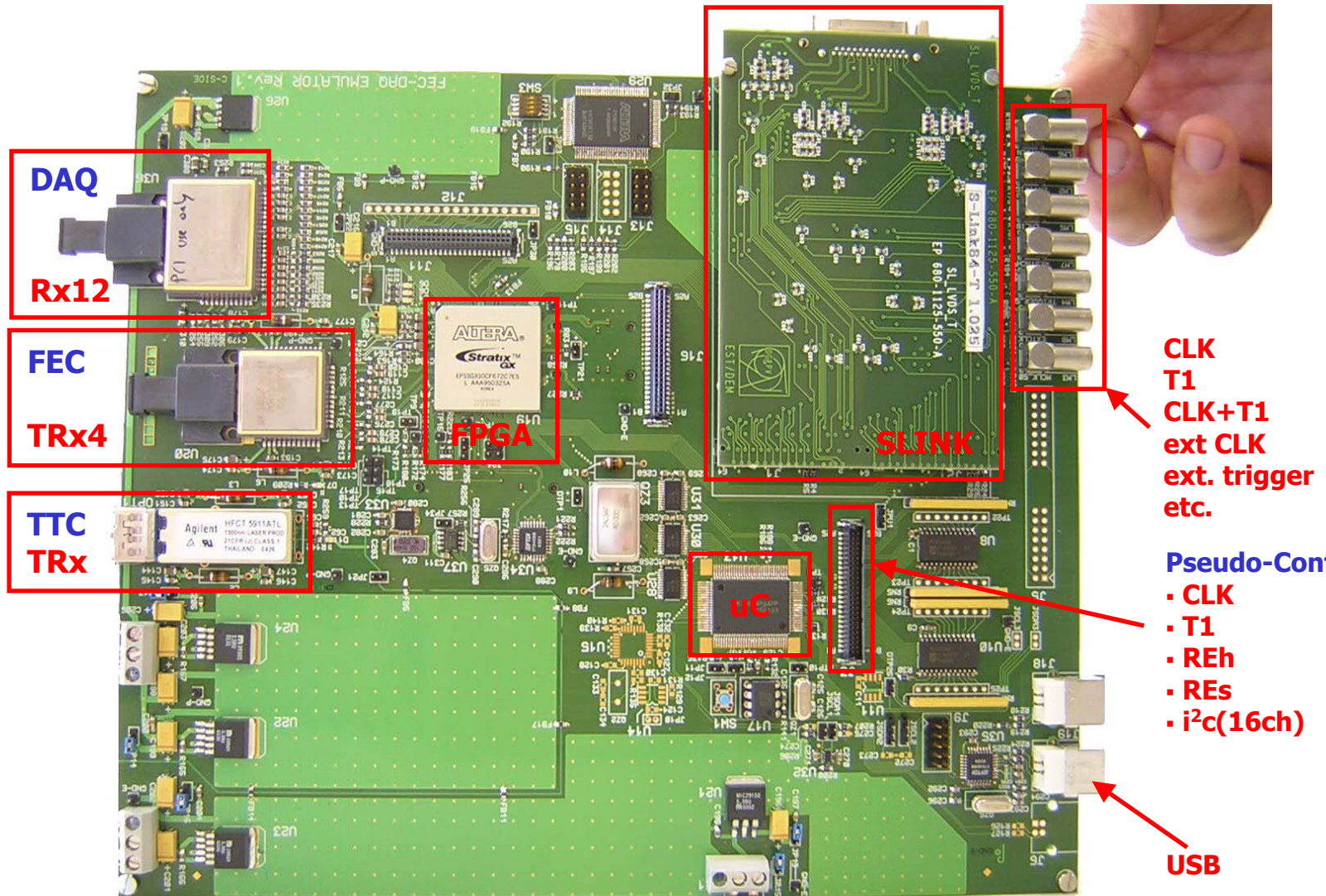
TESTBENCH - Features (1/2)





Programmable Trigger Generation

- ☞ Generate bursts of up to 1000 triggers - specifying the time (clock cycles) between each trigger
- ☞ Each "trigger" is actually two pulses
 - Calib – telling the PACE to generate an internal electronic injection signal
 - LV1 – sent <latency> clocks after the Calibration pulse





TESTBENCH - Software (1/2)



Timing Information

All values in # clocks

ColInjReg - Tn

Trigger Latency

Enable Trigger

Disable trigger

ReSynch period

Trigger

Control Register

CalPulse Length (clocks)

Pulse Mode

PACE Address

Mux Freq

Reset Flex

Setup FLEX

Start Running

Control Program

COM1 Port Time between commands (ms)

Register Status after Write

Time	ReSynch	Calib	LV1	EnTrigger	ReSynch'	Calib'	LV1'	EnTrigger'
0.0	0	0	0	1	0	0	0	0
25.0	0	1	0	1	0	0	0	0
50.0	0	0	1	1	0	0	0	0
75.0	0	0	1	1	0	0	0	0
100.0	0	0	0	0	0	0	0	0
125.0	0	0	0	0	0	0	0	0
150.0	1	0	0	0	1	0	0	0
175.0	1	0	0	0	0	0	0	0
200.0	1	1	0	0	0	0	0	0
225.0	1	0	0	0	0	0	0	0
250.0	1	0	0	0	0	0	0	0
275.0	1	0	0	0	0	0	0	0
300.0	1	0	0	0	0	0	0	0

Min time to display Update graph Max time to display



TESTBENCH - Software (2/2)



Global Preshower System-Board Control Panel

Initialize Read/Write Delta Registers Read/Write PACE-AM Registers Read/Write K Registers Single event Injection test Dynamic Range Pedestal scan Timing scan

Control signals: Start Master clk, Stop Master clk, Send ReH_B, Send ReS_B

K-chip identifier: 17FF, Delta Identifiers: 3709, PACE-AM Identifiers: 4809

Simple single event: off/on, Calpulse, Trigger, BCO

Injection OK: Events per channel: 1

Addresses OK: Events/cell: 50

Delta i2c address: 1, PACE-AM i2c address: 2, K-chip i2c address: 2

VISA resource name: ASRL2::INSTR, PACE connected: A, B, C, D

Waveform Graph: Amplitude (ADC counts) vs Multiplexed output

Directory: C:\PACE3, command sent: 0, s73IP0, CRC output: FFFF

Optical Input to display: 1, Storage Mode: full packet, Readout Mode: M16C readout

DATA INPUT electrical/optical, EXT TRIGGER POLARITY active hi/active low, Load Settings

Update Delta registers

Delta register names	Delta Present vals	Delta to write
Control reg 0	0 0 19 0	19 19 19 19
Control reg 1	0 0 0 0	0 0 0 0
Chip ID 0	0 0 246 0	251 251 251 251
Chip ID 1	0 0 200 0	224 223 232 220
Cal Chan 0	0 0 0 0	0 0 0 0
Cal Chan 1	0 0 28 0	0 0 0 28 0
Cal Chan 2	0 0 0 0	0 0 0 0
Cal Chan 3	0 0 0 0	0 0 0 0
Vcal	0 0 247 0	247 247 247 247
Wfrcamp	0 0 220 0	220 220 220 220
Vofshaper	0 0 88 0	0 88 0 88 0
Vipare	0 0 128 0	128 128 128 128
Ipreamp	0 0 128 0	128 128 128 128
Ishaper	0 0 128 0	128 128 128 128
ISF	0 0 128 0	128 128 128 128
Ipore	0 0 1 0	1 1 1 1 1

Control Registers: Run Mode, Gain, Calibration Precision, DAC Output to DCU

Calibration channels A, B, C, D

Ready, Auto read, Debug

Update PACE-AM registers

PACE-AM register names	PACE-AM Present vals	PACE-AM to write
Control reg	0 0 1 0	1 1 1 1 1
Latency	0 0 127 0	127 127 127 127
Chip ID 0	0 0 246 0	251 251 251 251
Chip ID 1	0 0 183 0	224 223 232 220
Vinhibit	0 0 76 0	76 76 76 76
Voutbuff	0 0 145 0	145 145 145 145
Voutbuff	0 0 153 0	153 153 153 153
BreadAmp	0 0 128 0	128 128 128 128
Ishft	0 0 128 0	128 128 128 128
Iminbuff	0 0 128 0	128 128 128 128
Ioutbuff	0 0 128 0	128 128 128 128
Ipore	0 0 0 0	0 0 0 0
UpsetReg	0 0 0 0	0 0 0 0

Control Registers: Run Mode, Probe Mode, Inhibit Data Valid, DAC Output to DCU, Latency Error/Enable

CRASH PROGRAM, PACE-AM update successful, Copy from PACE A, Copy to PACE A

PACE reg counter: 0

Data Packet Decoder

Event Counter: 1, Bunch Counter: 8F, K-chip ID: 2, Packet Size: 299, CRC: [OK]

Decoded Column Addresses: 0, 2E, AA, 2F, AA, 30, AA

Packet 1/2: PACE A Active, PACE B Active, PACE C Active, PACE D Active, K Trigger FIFO full, PACE Trigger FIFO full, K Data FIFO full, General Error in PACE sync

K Trigger Inhibit Logic Mode, Calibration Event, Reserved, Link Test Packet Flag

K-chip Register

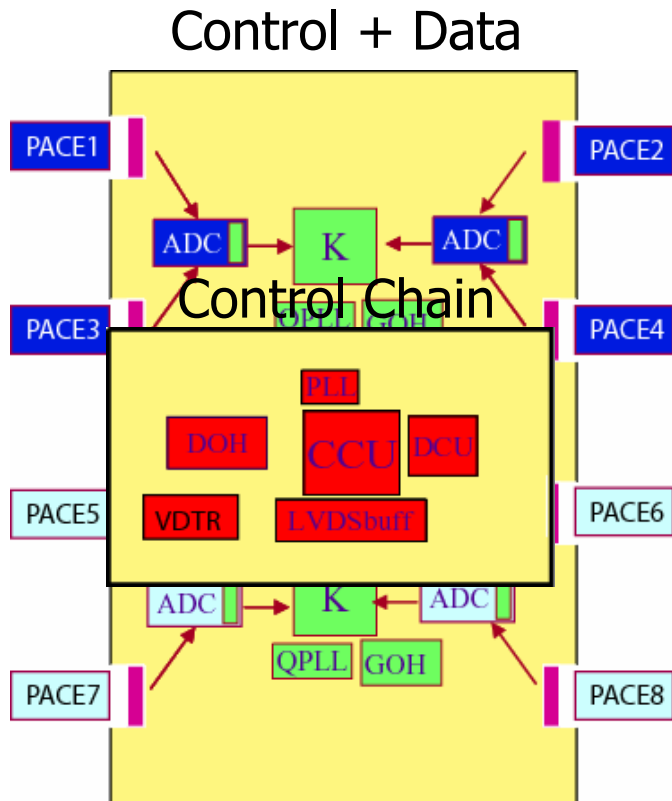
K-chip R/W registers	K-chip R/W values	K-chip R/W to write	Bits to Set	K Config
Config	15	1	Enable PACE A	[On]
Econfig	0	0	Enable PACE B	[Off]
K-chip ID Low	2	2	Enable PACE C	[On]
K-chip ID High	0	0	Enable PACE D	[Off]
Trigger Mask	0	0	Link Test: Normal/Test	[Normal/Test]
Trigger Latency	128	127	GOL Tx: Enable/Disable	[Enable/Disable]
Gol i/face Busy	0	0	Trigger: Inhibit/Passive	[Inhibit/Passive]
Gol i/face Idle	0	0	Mode: Normal/Test	[Normal/Test]
FIFO Map	0	0	Bits to Set 2	[K E Config]
FIFO Data High	0	0	DLL logic: Enable/Disable	[Enable/Disable]
FIFO Data Low	0	0	Calib: Enable/Disable	[Enable/Disable]
CalPulse Delay	254	1	Save Settings	[Save Settings]
CalPulse Width	20	2	Load Settings	[Load Settings]



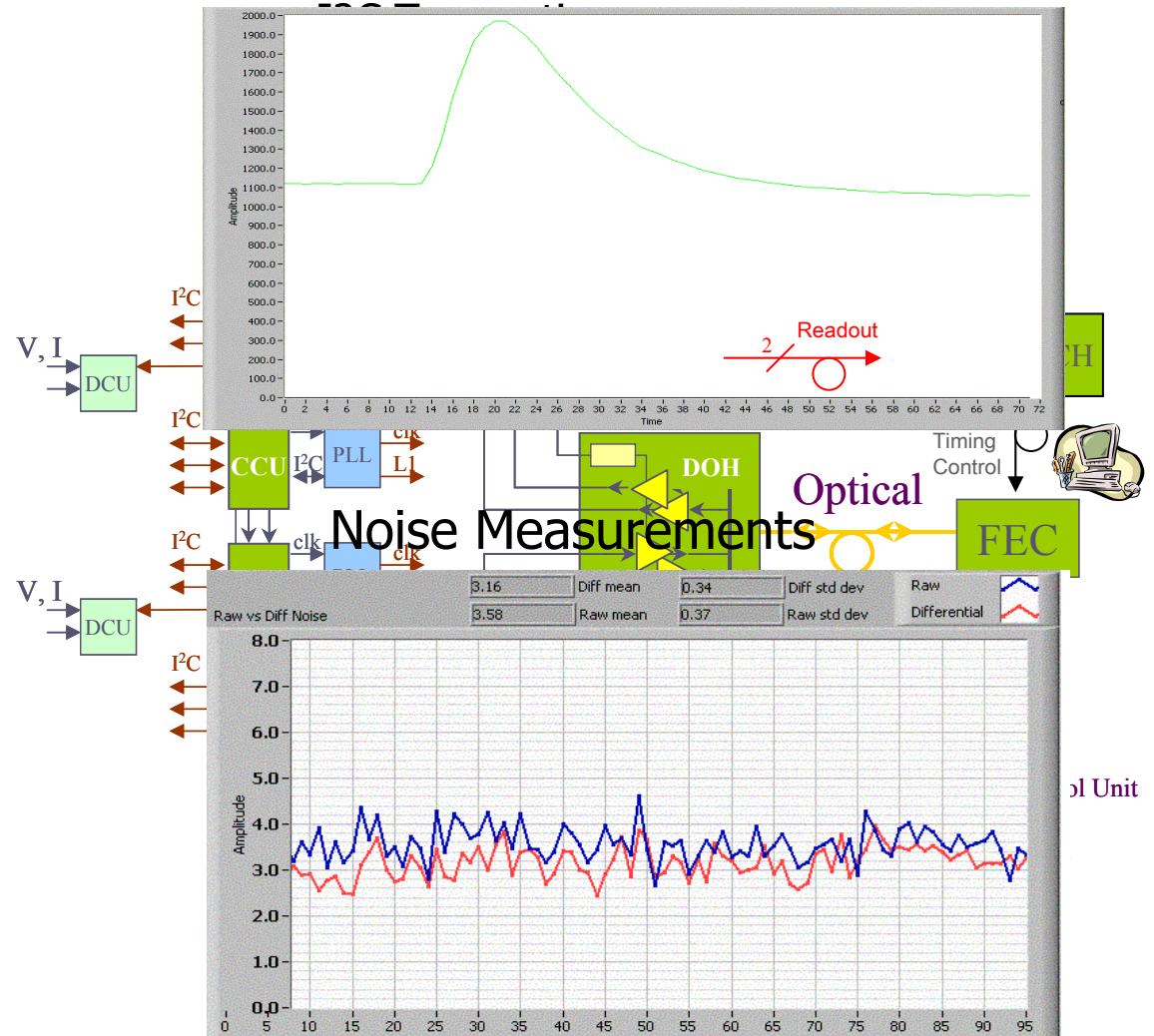
TESTBENCH – System Tests



Design Verification



Pulse Reproduction Distribution





TESTBENCH – Other Uses



- ➡ Production testing of system boards/micromodules Taiwan, Greece, CERN
- ➡ Test beam (end of September 2004)
- ➡ Prototype of CMS Preshower Data Concentrator Card, if necessary



SUMMARY



- Stand-alone PC-controlled evaluation system for Preshower on-detector electronics
- Timing, trigger and control signals & readout
- Optical interface available
- Flexible/Portable/Low Cost
- Principle production testing system for ~500 CMS Preshower system boards & ~4300 PACE hybrids in Taiwan, Greece and CERN
- Useful (?) for evaluating or production testing of other detector electronics systems, for LHC and beyond