A flexible stand-alone testbench for facilitating system tests of the CMS Preshower

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• Testbench
  – Motivation
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INTRODUCTION – CMS Preshower

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INTRODUCTION – Preshower Architecture

on-detector

Readout Path

Data Concentrator Card

VME module

Subdetector Event Builder

off-detector

Clock & Control System

VME module

TTCvi

VME module

Front End Control ASICs

DCU

CCU

Front End Readout ASICs

PACE

ADC

K chip

Slow Control & Fast Timing Signals

PC

Re

Clk

T1

Control Path

I

V

PC

Subdetector Event Builder

Data Concentrator Card

VME module

Slow Control

Fast Timing

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INTRODUCTION - On-detector electronics

μmodule

System board
**Main Purpose:** Evaluation of system board

**Requirements**
- Clock & control system
- Flexible Trigger Generation system
- Readout system

**Availability (Q3 2003)**
- Clock & control system: ✔ FEC
- Flexible Trigger Generation system: ✗
- Readout system: ✗
TESTBENCH - Features (1/2)

- Triggers Unit
  - Programmable trigger burst generation
  - Patterns up to 1000 triggers
  - Triggers in Poisson distribution at 100KHz
  - Multiple trigger format (TTC, T1, CLK+T1)
  - External Trigger

- Readout Unit
  - 4 Optical inputs
  - Embedded gigabit deserializers
  - High speed readout via S-Link64

- Control Unit
  - Electrical/optical FEC functionality [FEC firmware/software provided by its authors]
  - Pseudo-Control (CLK, T1, i2c lines)
  - PC Interface via USB

- Micro-controller
- S-Link64 transmitter mezzanine card

- USB interface
- Pseudo-control
Programmable Trigger Generation

- Generate bursts of up to 1000 triggers - specifying the time (clock cycles) between each trigger
- Each “trigger” is actually two pulses
  - Calib – telling the PACE to generate an internal electronic injection signal
  - LV1 – sent <latency> clocks after the Calibration pulse
TESTBENCH - Software (1/2)

Control Program

Load Configuration  Save Configuration

Register Status after Write

ColInjReg - Tn
Trigger Latency
Enable Trigger
Disable trigger
ReSynch period
Trigger
External
Control Register
CalPulse Length (clocks)
Pulse Mode
0: 1 RS, 1 Cal burst
PACE Address
Mux Freq
20 MHz
Reset Flex
Setup FLEX
Start Running

Min time to display
Update graph
Max time to display

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Global Preshower System-Board Control Panel

Update Delta registers

Update PACE-AM registers

Data Packet Decoder

K-chip Register

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Tests to be done

- Conclude Noise studies
- Behaviour under high trigger rate

Control Chain:

- Control + Data
- ADC
- K
- ADC
- DOH
- CCU
- DCU
- VDTR
- LVDSbuff
- QPLL
- GOH
- PACE1
- PACE2
- PACE3
- PACE4
- PACE5
- PACE6
- PACE7
- PACE8

Noise Measurements:

- Optical
- FEC

Design Verification:

- TESTBENCH – System Tests
- Control Chain
  - Clock/Trigger/Reset Distribution
  - I2C Transactions
  - Redundancy
  - Pulse Reproduction
  - Noise Measurements

Other Elements:

- 2 Readout
- V, I
- DCU
- PC
- V, I
- DCU
- PC
- 2 Readout
- Timing Control
- Control Unit
Production testing of system boards/micromodules Taiwan, Greece, CERN
Test beam (end of September 2004)
Prototype of CMS Preshower Data Concentrator Card, if necessary
SUMMARY

- Stand-alone PC-controlled evaluation system for Preshower on-detector electronics
- Timing, trigger and control signals & readout
- Optical interface available
- Flexible/Portable/Low Cost
- Principle production testing system for ~500 CMS Preshower system boards & ~4300 PACE hybrids in Taiwan, Greece and CERN
- Useful (?) for evaluating or production testing of other detector electronics systems, for LHC and beyond