Test results of the Data Concentrator Card of the CMS Electromagnetic Calorimeter Readout System

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Abstract

The Data Concentrator Card (DCC) is part of the Off-Detector (OD) Electronics sub-system of the CMS Electromagnetic Calorimeter. It is responsible for crystal and trigger data collection from the Front-End system and from the ECAL Trigger system respectively. DCC data are reduced by a factor of 20 in order to get an average data transmission flow of 200 MByte/s to the central CMS DAQ system. This reduction is obtained through selective readout (SR) of calorimeter regions and the application of crystal zero suppression (ZS).
The test system includes a DCC Tester Card (DCC-TC), which emulates all the external interfaces of the DCC. In this paper the functionality and design of both cards are summarized, the developed test bench is described and the first test results are reported.

I. Introduction

The CMS ECAL comprises approximately 77000 $PbW0_4$ crystals organized in supermodules, in the barrel, and in D-shaped modules in the endcaps. After amplification, crystal signals are digitised and then pipelined in the Front-End (FE) boards waiting for the first-level trigger decision (L1A). Each FE board processes the data from 25 crystals, corresponding to one trigger tower in the barrel and one super-crystal in the endcaps. In parallel, these rad-hard boards compute the tower trigger primitives in the barrel and the pseudo-strip energy sums in the endcaps [1].

In Figure 1 the ECAL OD trigger and readout architecture is sketched. Trigger tower or pseudo-strip energies from different FE boards are transmitted to the Trigger Concentrator Card (TCC). The TCC performs the final calculation of the trigger primitives. After non-linear compression [2] and synchronization [3], trigger data are sent to the Regional Trigger. The Selective Readout Processor (SRP) receives trigger data from the TCC and processes the selective readout flags at each L1 trigger [4,5]. The Clock and Control System (CCS) distributes the clock and control signals to the DCC, the TCC and the FE boards, being also responsible for their interface to the synchronous Trigger Throttling System (sTTS) [1].

The DCC [6] is a common collection point for crystal and trigger data. After each L1A, the DCC collects crystal data transmitted from 68 FE boards (comprising one supermodule in the barrel) and trigger data transmitted from the TCC (1 TCC in the barrel and 4 TCCs in the endcaps). The DCC also receives the selective readout flags from the SRP.

The main functions include opto-electric conversion and deserialization of the input data streams, verification of data integrity, reduction of the front-end data (through the combination of SR and crystal ZS), event formatting and transmission to the CMS DAQ system. The DCC is also responsible for reading spy events to the local DAQ.

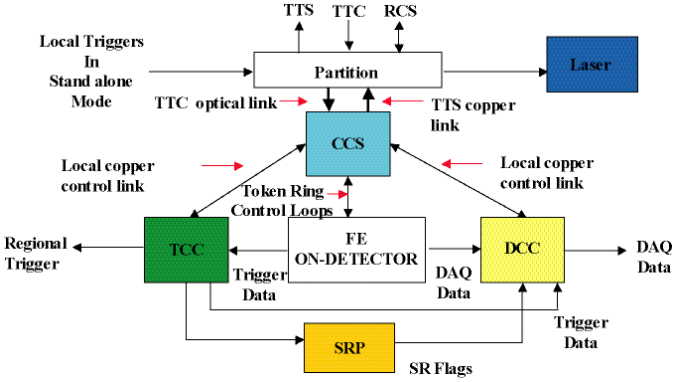

Figure 1: ECAL Off-Detector Trigger and Readout Architecture.

In Section II, the functionality, architecture and implementation features of the DCC are summarized. Section III presents the developed test bench and in section IV the first test results are reported.

II. DCC Description

The DCC is a VME-9U format board (Figure 2), VME64x compliant, following the new proposed design rules for custom VME hardware in CMS [7].

Figure 3 shows the DCC general architecture, which was motivated by the studies presented in [8]. After optical to electrical conversion and deserialization into 16-bit words, input data enter the Receiver Block where is stored in the input memories after data integrity checks and crystal zero supression (Figure 4).

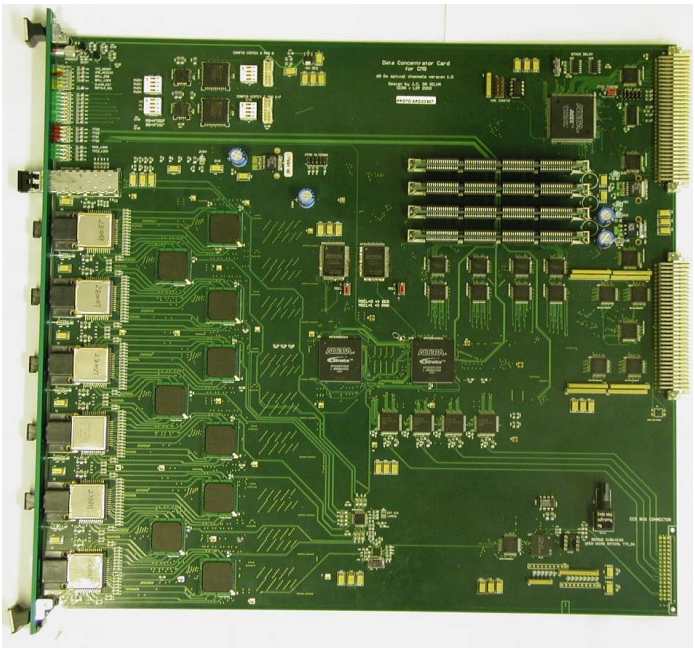

Figure 2: DCC prototype.

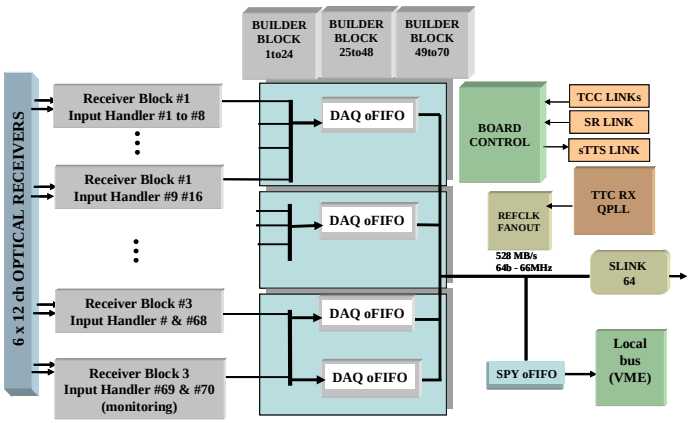

Figure 3: General DCC architecture.

The received SR flags indicate the level of suppression of crystal data that must be applied in each input channel (no suppression, level 1 ZS, level 2 ZS, or full suppression). Zero supression is based on the estimation of the crystal energy using a FIR filter and on two programmable thresholds.

Three Event Builders working in parallel collect the data fragments of three groups of channels and build partial events in three output memories. A separate memory is used for the laser monitoring channels (channels 69 and 70) in conjunction with the monitoring triggers. The Event Builders monitor the occupancy of the memories to prevent buffer overflows. If a first occupancy level is reached the sTTS signal Warning Overflow is issued, requesting a reduction of trigger rate. If a second level is exceeded empty events are stored in the memories while the sTTS signal Busy inhibits new triggers. In case of buffer overflow the DCC enters in the error state.

The Output Handler is responsible for the transmission of the data from the output memories to the central or local DAQ.

The DCC event is transmitted to the central CMS DAQ using the S-Link64 protocol [9] implement by a LVDS high speed parallel link [18]. A spy memory (16 MByte) is used for local DAQ, allowing VME access to full DCC events for monitoring. A combination of SR and ZS yields the necessary reduction factor of the incoming data with no significant effects in the physics reconstruction [10,11], resulting in an average transmission data flow of 200 MByte/s. The output data rate is limited by design to a maximum of 528 MByte/s.

The board has 72 optical 800 Mbit/s inputs converted by 6 NGK 12-Channel Receivers. These are followed by 8b/10b deserializers implemented in nine Xilinx® Virtex-II Pro™ devices with eight embedded RocketIO™ transceivers on each [12,13]. All high-speed traces are impedance controlled, the corresponding differential pair signals is AC coupled and all the transceivers power supply pins are filtered with an individual LC filter. The required low-jitter clock is generated by a QPLL chip [16] out of the Trigger Timing and Control (TTC) clock. Each Xilinx receives a high-quality reference clock differential pair from an individual buffer.

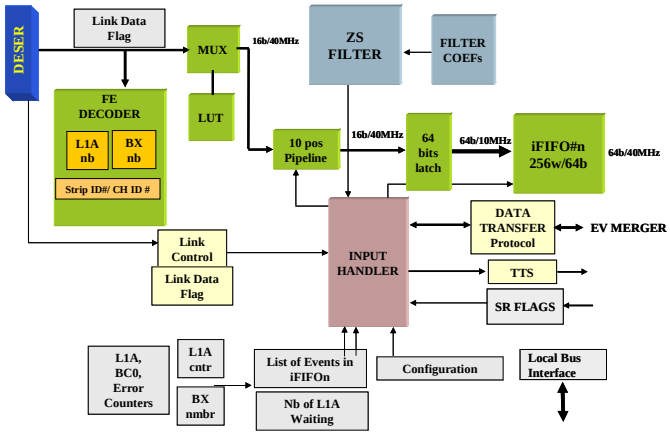

Figure 4: Architecture of the Receiver Block (one channel).

The Receiver Blocks and the input FIFOs are implemented in the Virtex II FPGAs and the Event Builders and the Output Handler are implemented in two large Altera FPGAs. The SRP interface uses one individual optical link and the trigger data are received in 4 electrical LVDS links. Trigger, clock and fast commands are received by a TTCrx chip. The TTC and sTTS electrical connections to the CCS board are implemented on a dedicated backplane occupying the P3 area. The S-Link64 interface port uses the VME J2/P2 connector to connect to a transition board housing the DAQ link. The DCC module has a VME64x auto-configurable VME Slave (A32/D32) compliant with CMS rules. The card is built on 12-layer 9U PCB (36cm x 40cm), with four power planes and eight routing layers, assembling 1262 components, including 12 fine pitch BGA packages.

As for JTAG programming, the same group of EPROMs is used to configure eight of the nine FPGAs. One of the FPGAs

is the master and provides the clock for all the devices in the chain. The ninth FPGA has a different pinout and a separate EPROM for itself.

III. DCC TEST SYSTEM

The test system includes a dedicated test module specifically built for this application. The DCC Tester Card (DCC-TC) is a VME-9U format board that emulates the interfaces between the external sub–systems (FE, TCC and SRP) and the DCC (Figure 6).

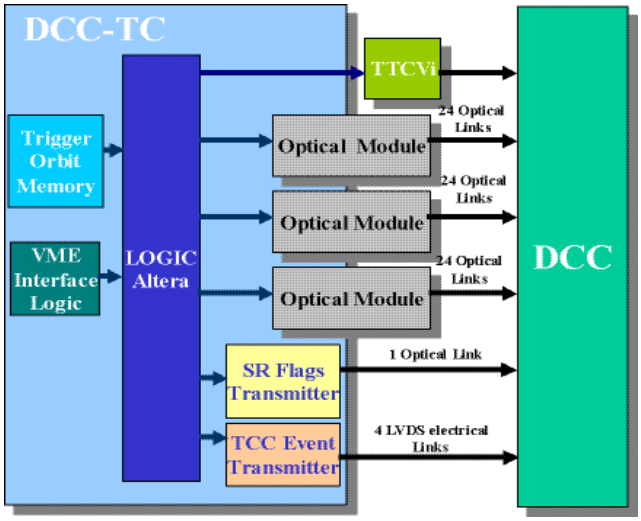

Figure 5: DCC Tester Card architecture.

In Figure 5 a scheme of the DCC-TC architecture is presented. The Optical Module (OM) emulates the FE interfaces. Each one of these mezzanine cards has 24 Gigabit Optical Links (GOL) [14] and three 8-channel NGKoptical drivers. Three OM comprise 72 channels. The TCC

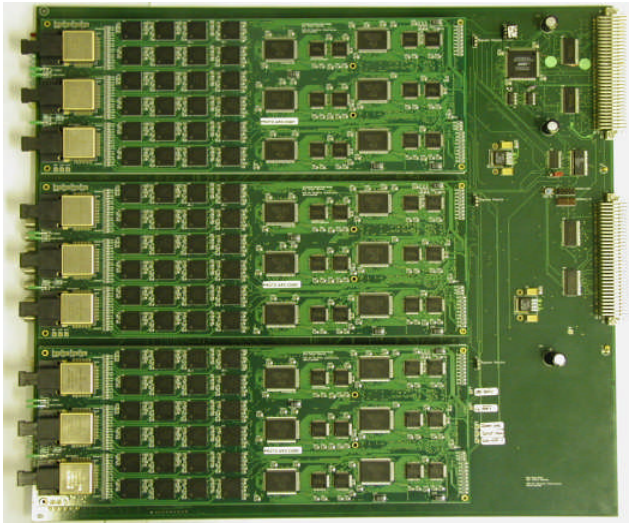

Figure 6: The DCC tester Card

Transmitter emulates the TCC interface through 4 electrical LVDS connections. The SR Transmitter emulates the SR interface through a GOL chip and a single optical driver. The DCC-TC was designed to store approximately 1000 simulated events. Both the TCC and the SR Flags Transmitters have one dedicated memory (8 MBit) for trigger data and SR flags storage. Crystal data are stored in the OMs with a storage capacity of 4 MBit/channel. The timing of each event, namely, the bunch crossing number and the orbit number are stored in the trigger-orbit memory (8 MBit).

The TTC system [16] provides distribution of timing, trigger and fast control signals. The DCC-TC controls the operation of the TTCvi by generating the LHC clock, the orbit signal, the L1A and the fast commands (bunch counter reset, event counter reset, reSync, and monitoring commands) [17].

The DCC-TC is able to generate physics and monitoring triggers. Physics triggers are generated by issuing a L1A for each trigger position. After generation of the L1A, the FE data, the SR flags and the trigger data of the corresponding simulated event are transmitted. Different latencies can be specified among the different data transmitters. The monitoring triggers (laser and test pulse) are generated with a programmable orbit rate and a programmable bunch crossing position. Monitoring triggers are identified by a TTC command prior to the L1A transmission [17].

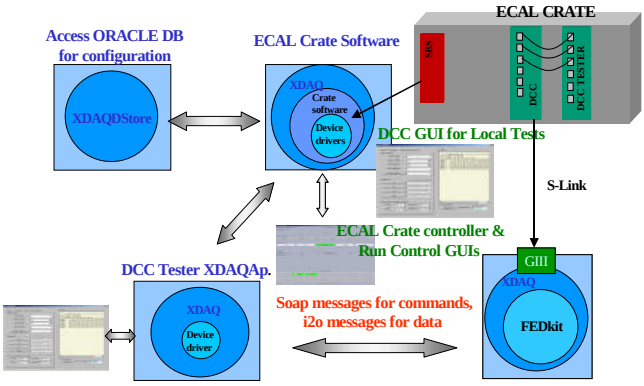

Figure 7 : DCC Hardware and Software Test Setup.

Four trigger operation modes have been foreseen: the step mode (triggers are transmitted individually upon a VME step command); the continuous mode (triggers are transmitted continuously until a VME stop command); the reSync mode (triggers are transmitted continuously followed by a reSync procedure) and, the auto stop mode (only a programmable number of triggers are transmitted).

In Figure 7 a diagram of the test bench used for testing the DCC is presented. In terms of hardware this comprises a VME-9U crate with a VME-PCI interface, a TTC system (not shown in the picture) and a DCC-TC connected through the required links to the DCC. A generic PCI GIII receiver board [18] is also included to test the DCC S-Link64 port.

The test system includes software for control, monitoring and configuration of the DCC [19], the DCC-TC and the GIII

receiver card [20]. This software is developed in C++ and in the XDAQ environment [21]. The DCC and the DCC-TC configuration were specified following the Generic Configurator Model [22,23].

Software for raw data generation, which is performed with the CMS physics simulation and reconstruction package [24], was also developed. Raw data were generated for jet events (50 GeV < Et < 100 GeV), which are representative of the CMS triggered events. High luminosity ($L \sim 10^{34} cm^2/s$) was assumed, corresponding to approximately 17 pileup events per crossing. The simulated data were made persistent as ASCII files. After configuring the boards in the crate, the simulated files are parsed and software objects representing the DCC input data blocks are instantiated.

A trigger generator class is responsible for the simulation of the trigger bunch and orbit number using a Poisson generator, also ensuring that the CMS trigger rules are fulfilled [1]. Different trigger conditions and rates can be tested with the same data.

The constructed data are loaded in the DCC-TC memories. Simultaneously the DCCTester xdaqApplication requests to the ECAL Crate Controller the actual readout configuration of the DCC (DCC active channels, readout mode, ZS thresholds and crystal weights used in the ZS algorithm). Based on the DCC readout configuration the Tester Event Builder emulates the expected DCC events. The output events are made available through the DCC spy memory or the GIII receiver card and finally compared with the emulated events.

IV. Test Results

The first prototype of the DCC was tested using the setup described above. No major design problems where found. The critical high-speed part of the design performed very well. Figure 8 shows the quality of the high-speed differential signal at the deserializers input.

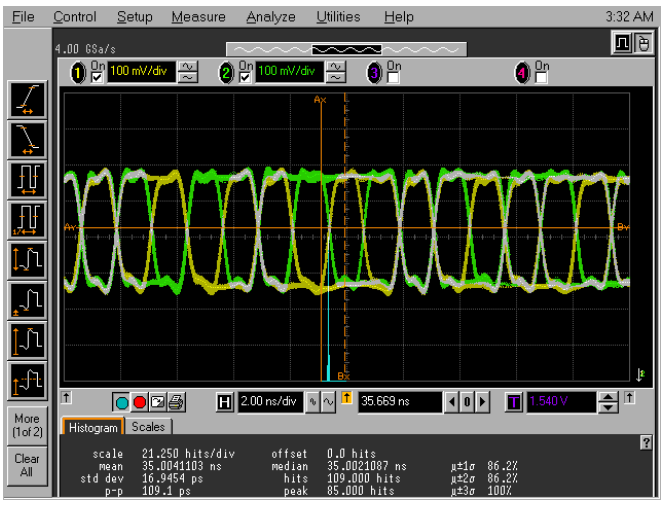

Figure 8: High-speed differential signal at the deserializers input.

The need for a high-quality reference clock should be emphasized. We made sure that the reference clock was as clean as we could get. The quartz-based phase-locked loop (QPLL) circuit provided a clock source with a jitter 100 ps peak-to-peak. We found that a number of problems in the performance of the RocketIO devices could be traced to a noisy reference clock.

Event data were routinely generated in the DCC-TC and transmitted to the DCC. The performance of the Rocket I/O devices was quite satisfactory, and the links transmitted data for long periods without errors. Systematic measurements of bit error rate were not yet concluded.

The processing of event fragments in the Receiver Modules and the event building and merging processes, performed according to the expectations. Events were simultaneously read from the spy memory via VME and transferred via the S-Link64 interface to a data acquisition PC.

Presently the DCC is being integrated in the ECAL test beam, reading a complete supermodule with 1700 crystals.

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