ECAL DCC Design Report

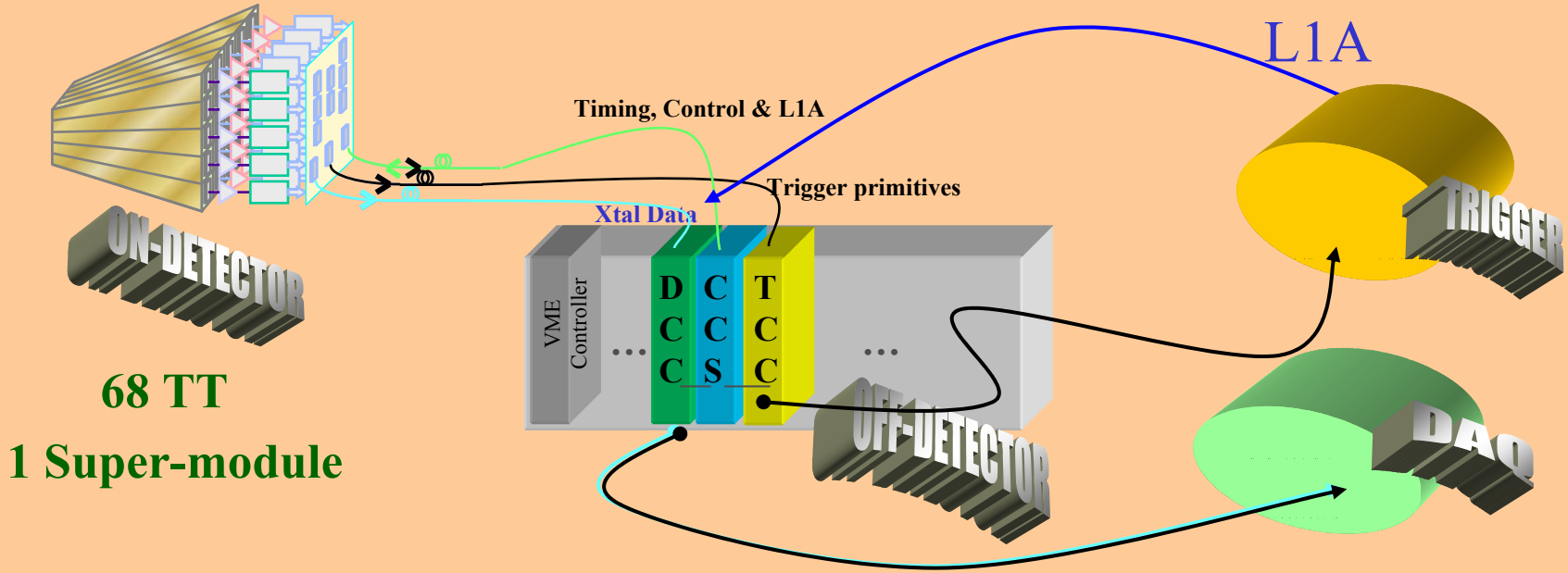
- DCC Design requirements
- Data reduction techniques (study and implementation)
- Technical Choices and Critical Design Issues
- DCC Testbench
- Results and Status

LECC, 14 September 2004

José C. Da Silva

DCC System View

FE data collection and event builder for DAQ System @ L1A rate



68 TT

1 Super-module

DCC Requirements

- **70 Opto-Electric converters and High Speed deserialisers (800 MBit/s - 8b/10b)**
  - *needs low Jitter Clock, High speed design techniques*
- **Input data integrity verification**
  - *Link status, source id, data block length, word parity bits, Event ID.*
- **Input data volume reduction (~20)**
  - *Application of the zero suppression (ZS) and selective readout (SR) algorithms.*
- **Event data format**
  - *Builds DCC event in DAQ format, including crystal data (FE), trigger data (TCC) and SR flags.*
- **Bandwidth**
  - *Data transmission to the central CMS DAQ max throughput is 528MB/s (average ~200 MByte/s)*
  - *Spying and monitoring events readable by the local DAQ.*
- **Monitoring of Event memories occupancy (TTS interface)**
- **Errors and Statistics**

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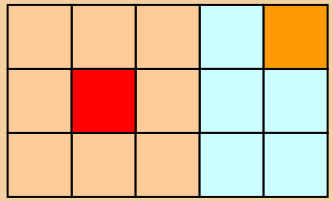
Data Volume Reduction methods

- ECAL Event Size tranfered to DAQ should be 100 KB on average (~2KB per DCC).
- Full ECAL event size is 1.86MB -> Data reduction tecniques must be applied to achieve a reduction factor of ~20 in ECAL data:
  - Zero Supression

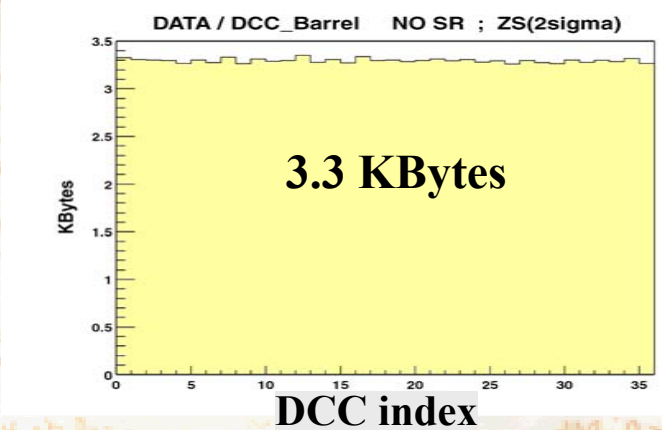
    Supression of crystals with energy lower than 2σ
    ~ 60MeV (Barrel) and ~ 300 Mev(EndCaps)
  - Tower Selective Readout Flags from SRP = (read tower /not read tower)



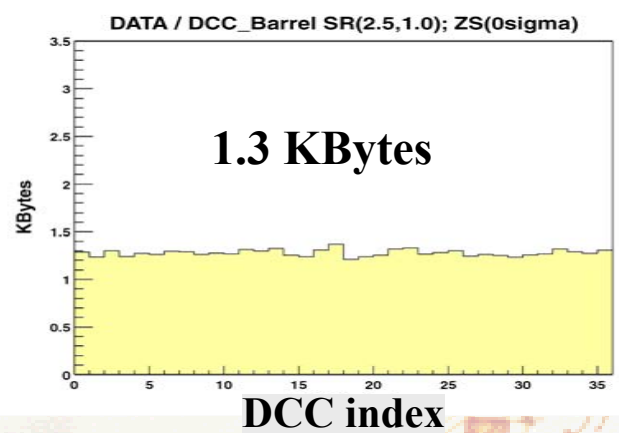
CENTER → $Et > H_{TH}$
SINGLE → $H_{TH} > Et > L_{TH}$
NEIGHBOUR → $Et < L_{TH}$
NOTREAD → $Et < L_{TH}$
and not neighbour....

Barrel DCC Event Size

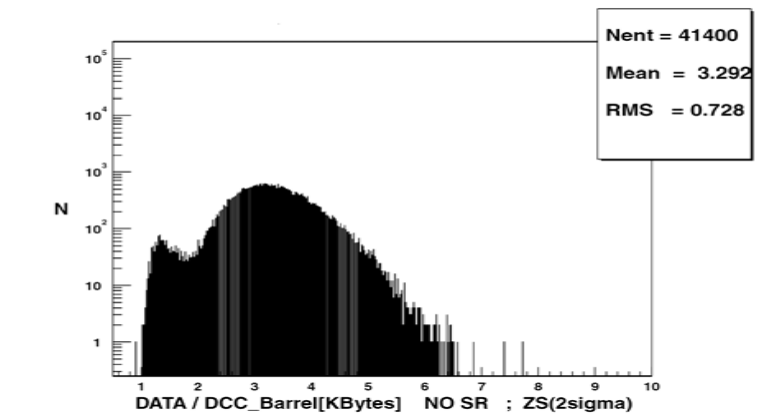
Zero Supression (2 σ)

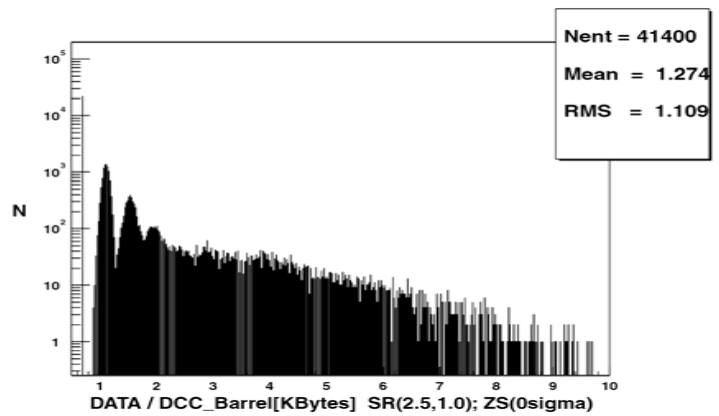


Selective Readout & Zero Supression (0 σ)



Distributions of DCC Event Size





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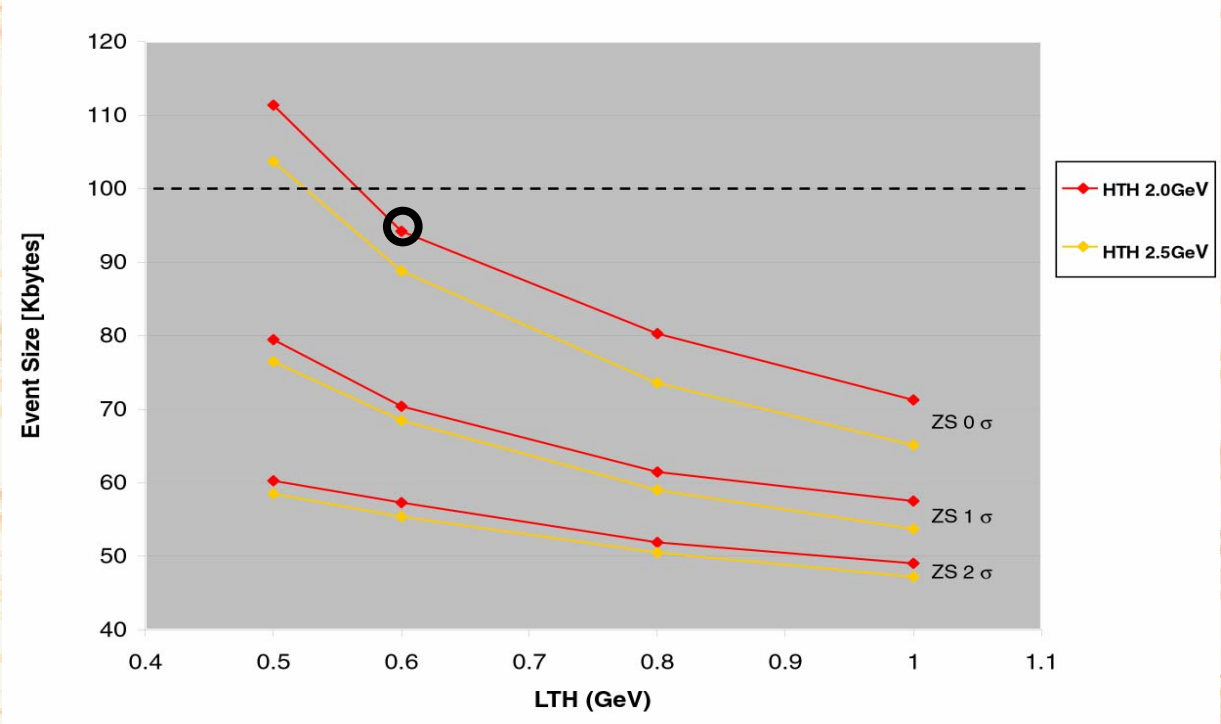
ZS & SR Scenarios



Setting Hth = 2.0 GeV, Lth = 0.6 GeV with ZS at 0σ we obtain an average ECAL Event Size of 95 KB without losing significant physics data and obeying ECAL data volume target of 100KB .

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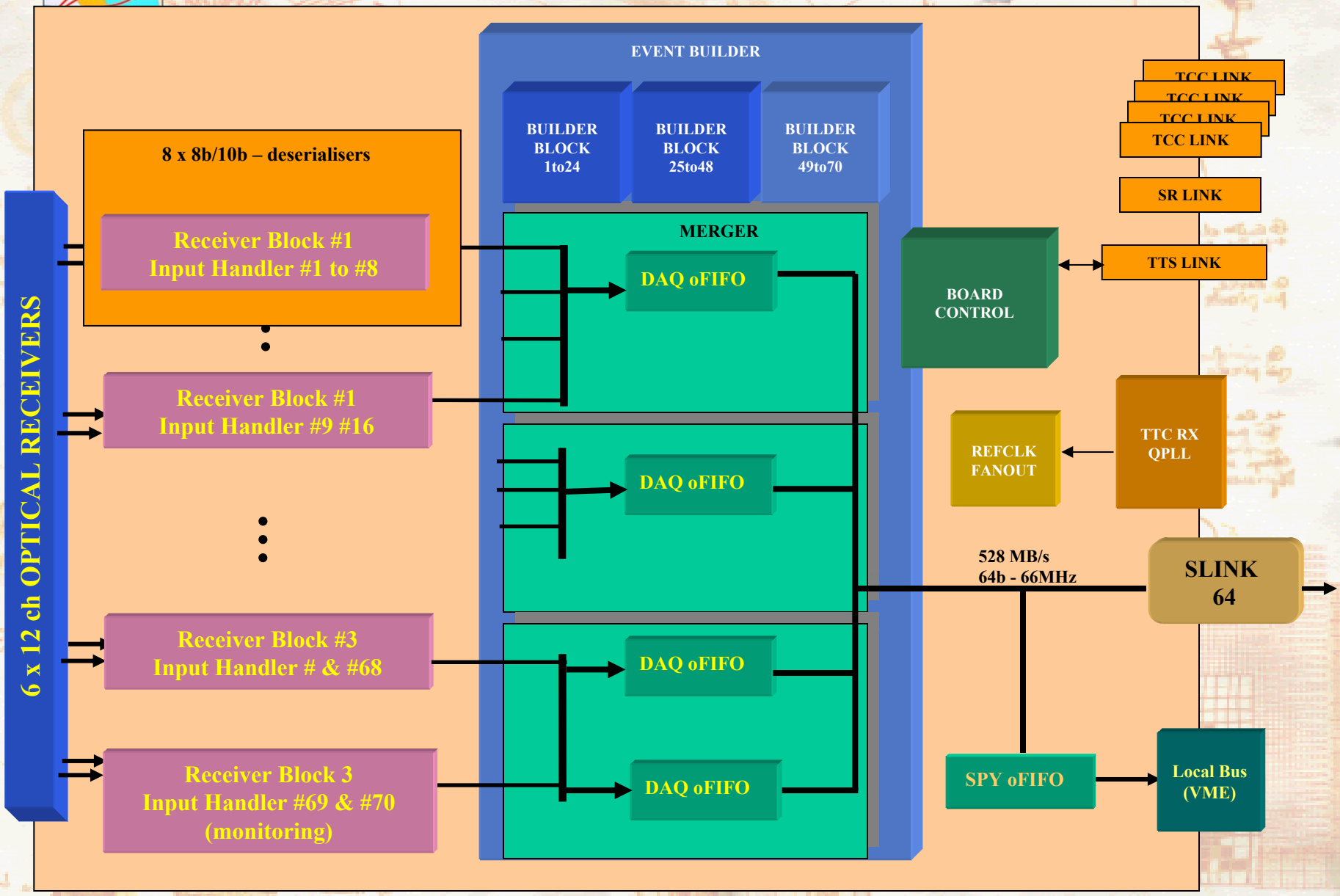
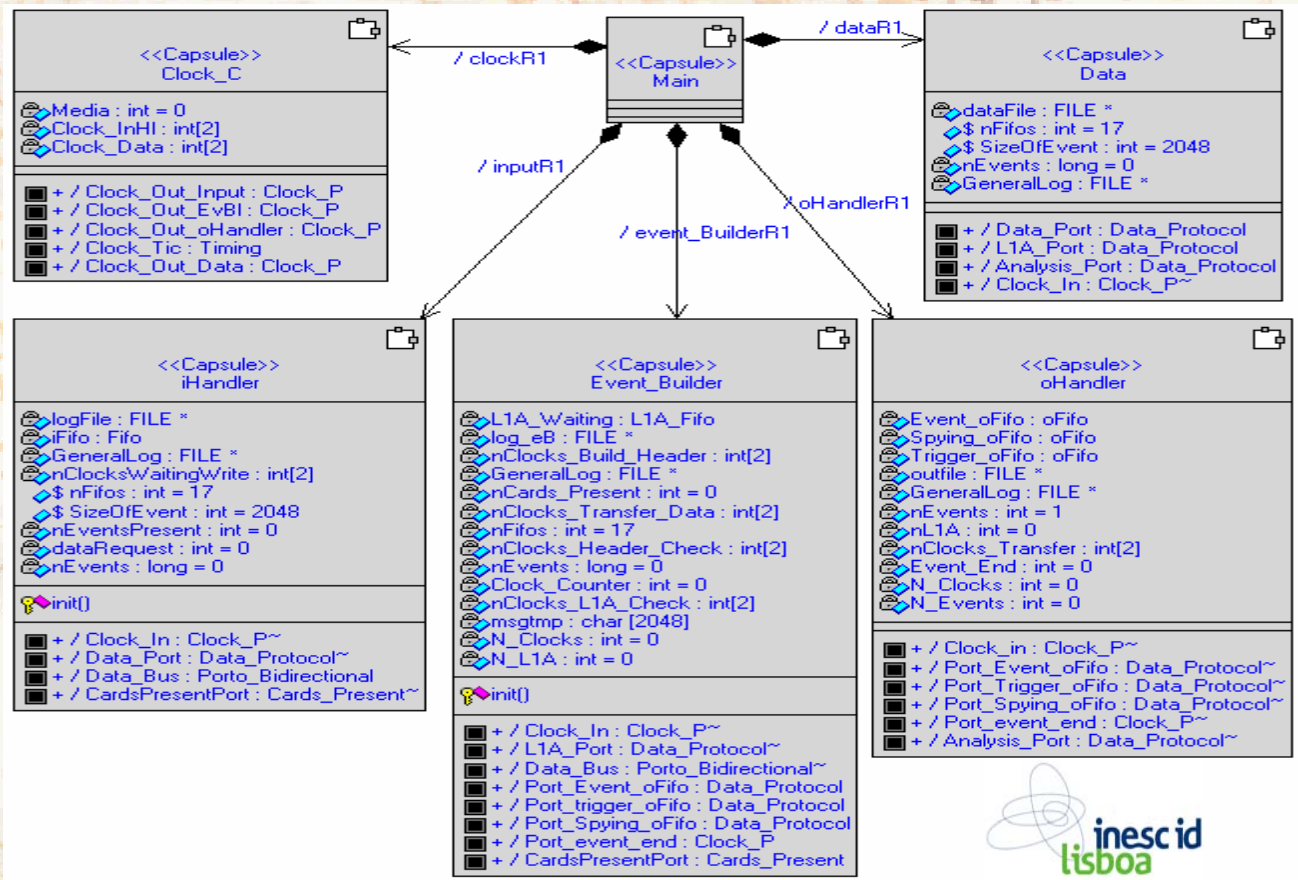
DCC Block Diagram



Hardware Modeling

- System Simulation using Rational Rose Real Time
- Input Raw Data from ORCA simulation



DCC High Level Model

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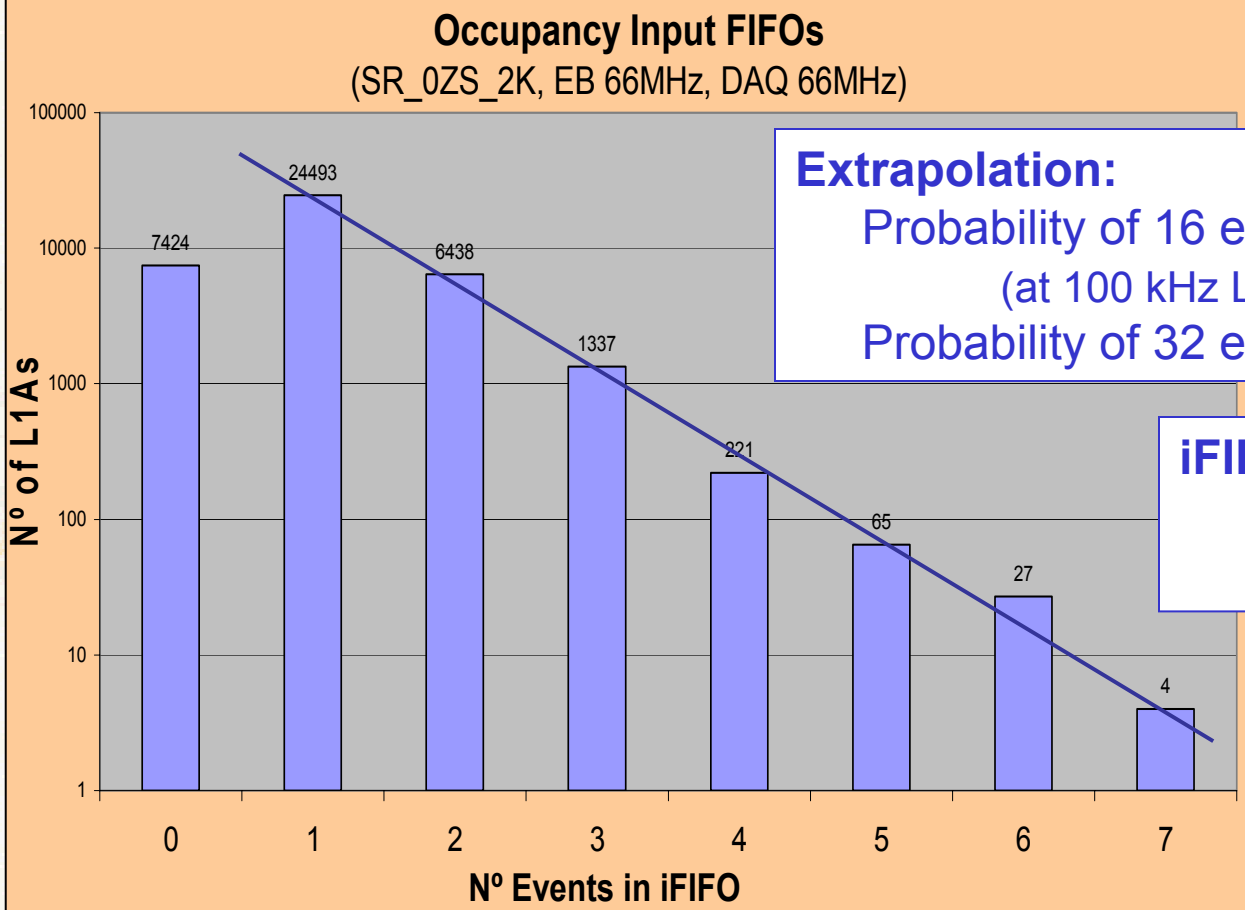
Overflow Probabilities (1)

SR and ZS thresholds tuned for 2kByte DCC event size

DCC bandwidth: 528 Mbyte/s



Extrapolation:

Probability of 16 events in iFIFO = 4 E-10

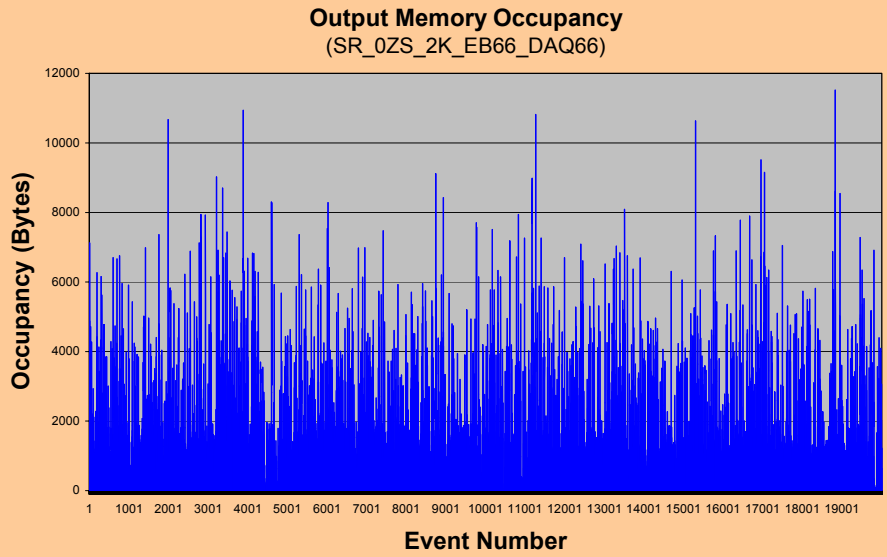
(at 100 kHz L1A, one overflow per 6.5 h)

Probability of 32 events in iFIFO = 7 E-20

iFIFOs size (each channel):

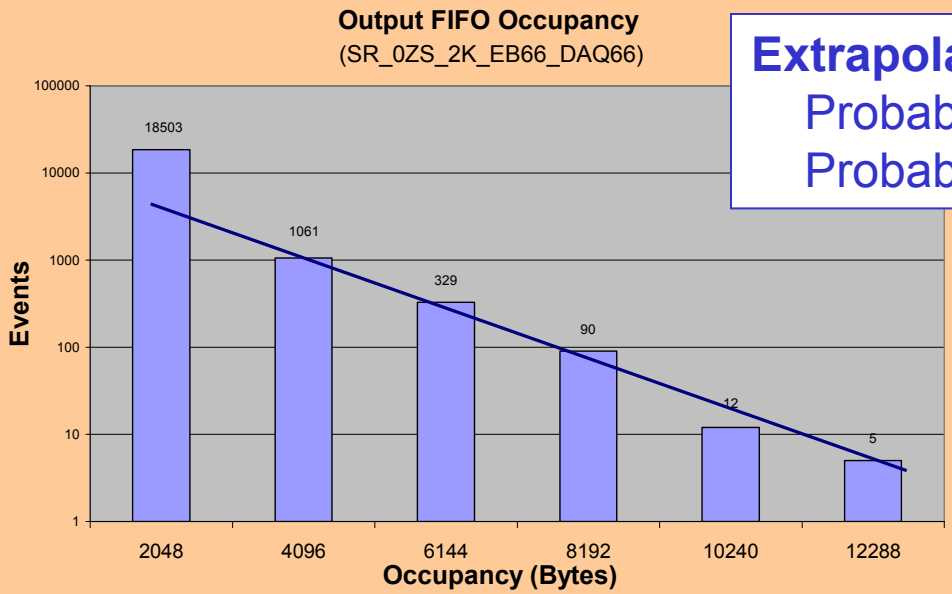
1 kByte = 32 events

Overflow Probabilities (2)



SR and ZS thresholds tuned for 2kByte DCC event size

DCC bandwidth: 528 Mbyte/s



Extrapolation:

Probability of 32 kB used = 3 E-10

Probability of 64 kB used = 1 E-19

oFIFOs size:

64 kByte = 32 events

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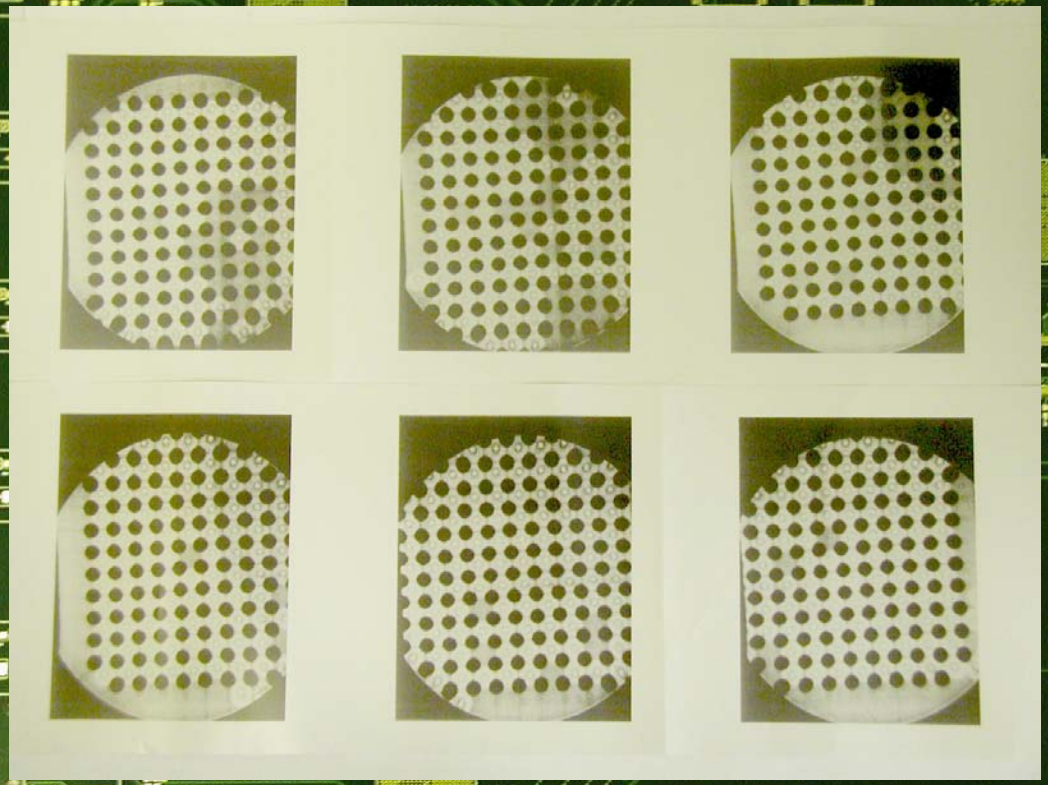
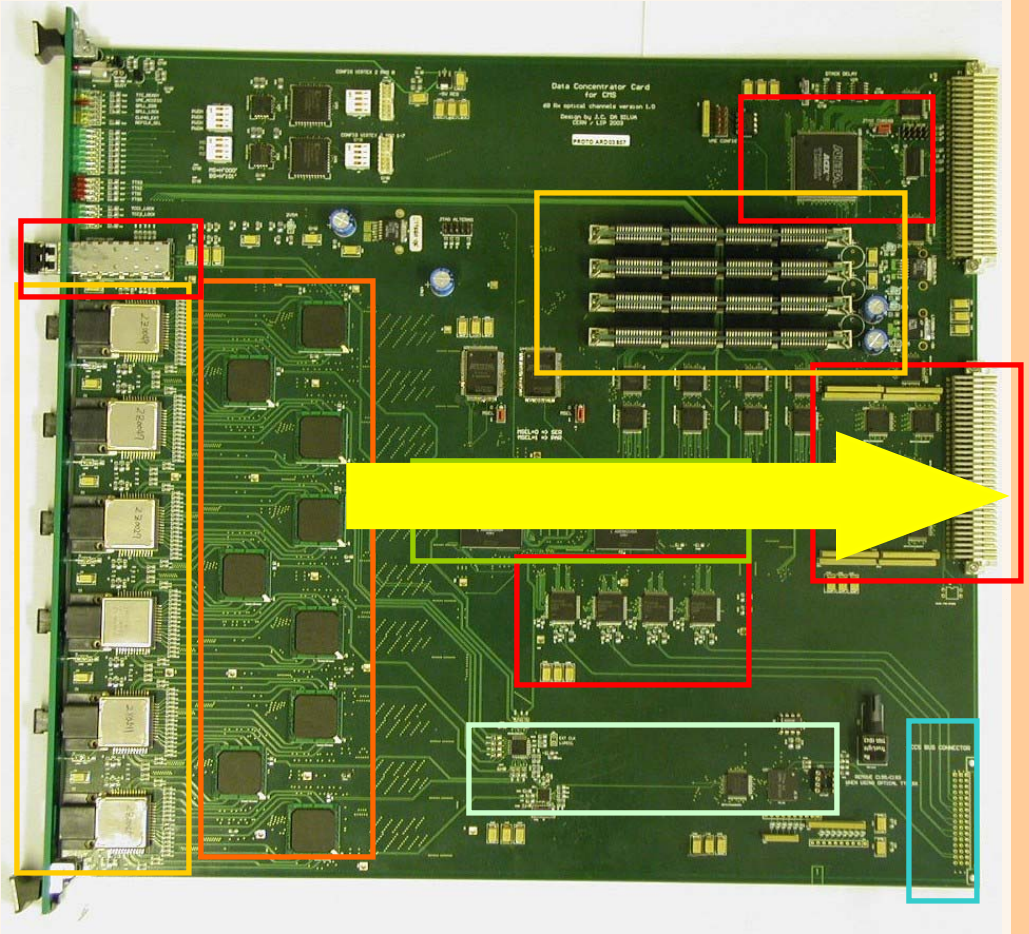
Critical Issues

- Number of High Speed channels / DCC
- Implementation of Optical Components
- High Speed Deserialisers (8b/10b)
- TTS, TTC, TCC, SRP and DAQ interfaces
- ~5000 Events Memory buffer (for test beam)
- Bandwidth (528MB/s)
- Testability, Reprogrammability
- Internal Power Supply
- DCC Testbench
- PCB 9U form factor (Design, Production, Assembly)

- 1262 components
- 48323 tracks
- 8850 vias
- 11270 holes
- 1647 nets
- Fine Pitch BGA packages
- 12 layers –9U (36cm x 40cm)

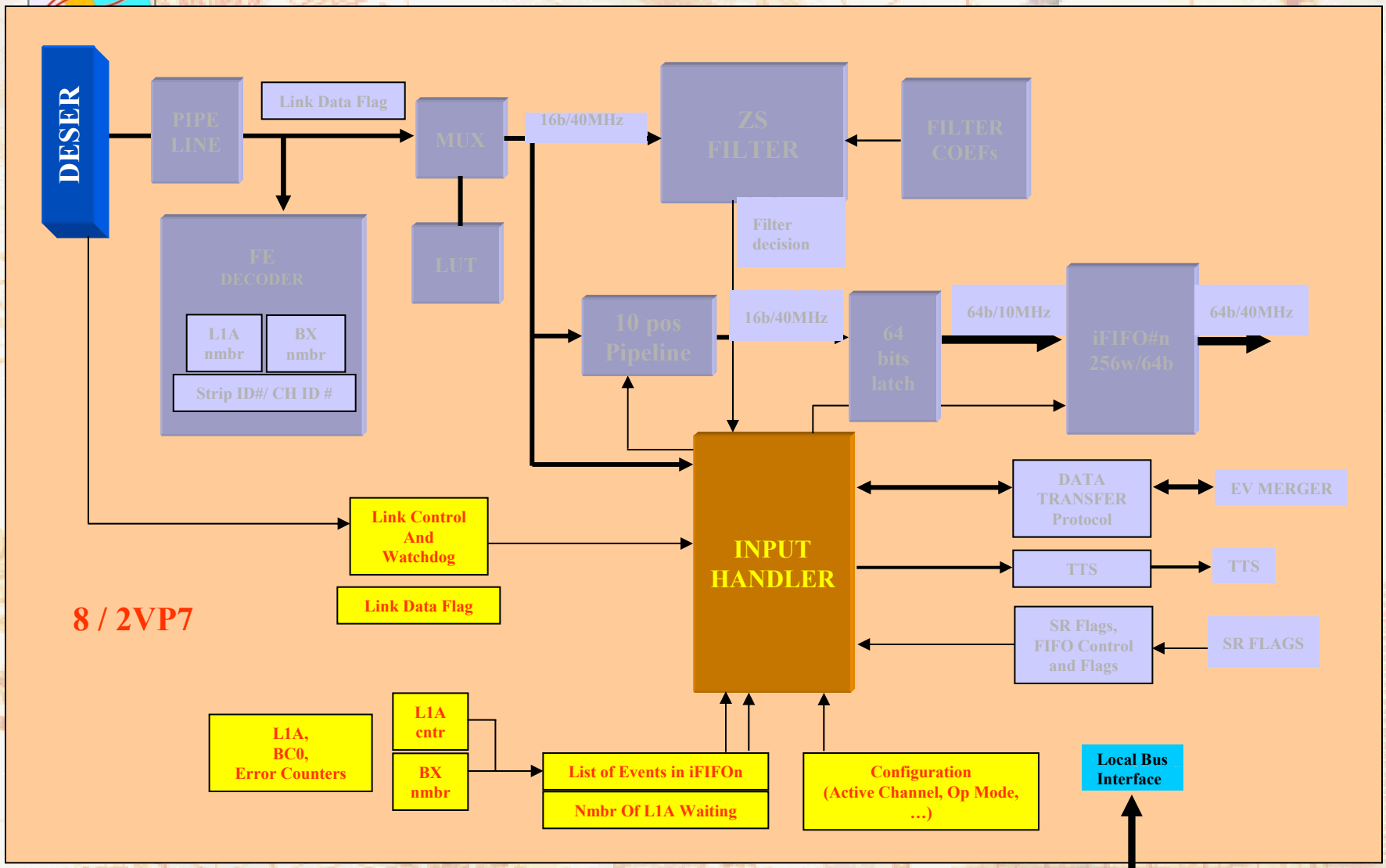


DCC Technical Choices



- VME64x Auto-configurable VME Slave (A32/D32) -> CERN
- 9 Virtex II pro FPGAs (Xilinx)
  - (8 Deser. 8b/10b, 8 Input Handler)
- 70 optical inputs (68 FE+ 2 MEM channels)
  - NGK 12Ch Receivers
- 1 SRP optical input
- 4 TCC electrical LVDS links
- TTC-rx and QPLL
- TTC, TCC, TTS interface (CCS Board)
- 1 S-Link64 port (J2/P2)
- Spy Memory Block (16 MB)
- Event Builder and Event Merger (Altera)
- Output Data Bandwidth up to 528 MByte/s (64b x 66MHz)

INPUT HANDLERS



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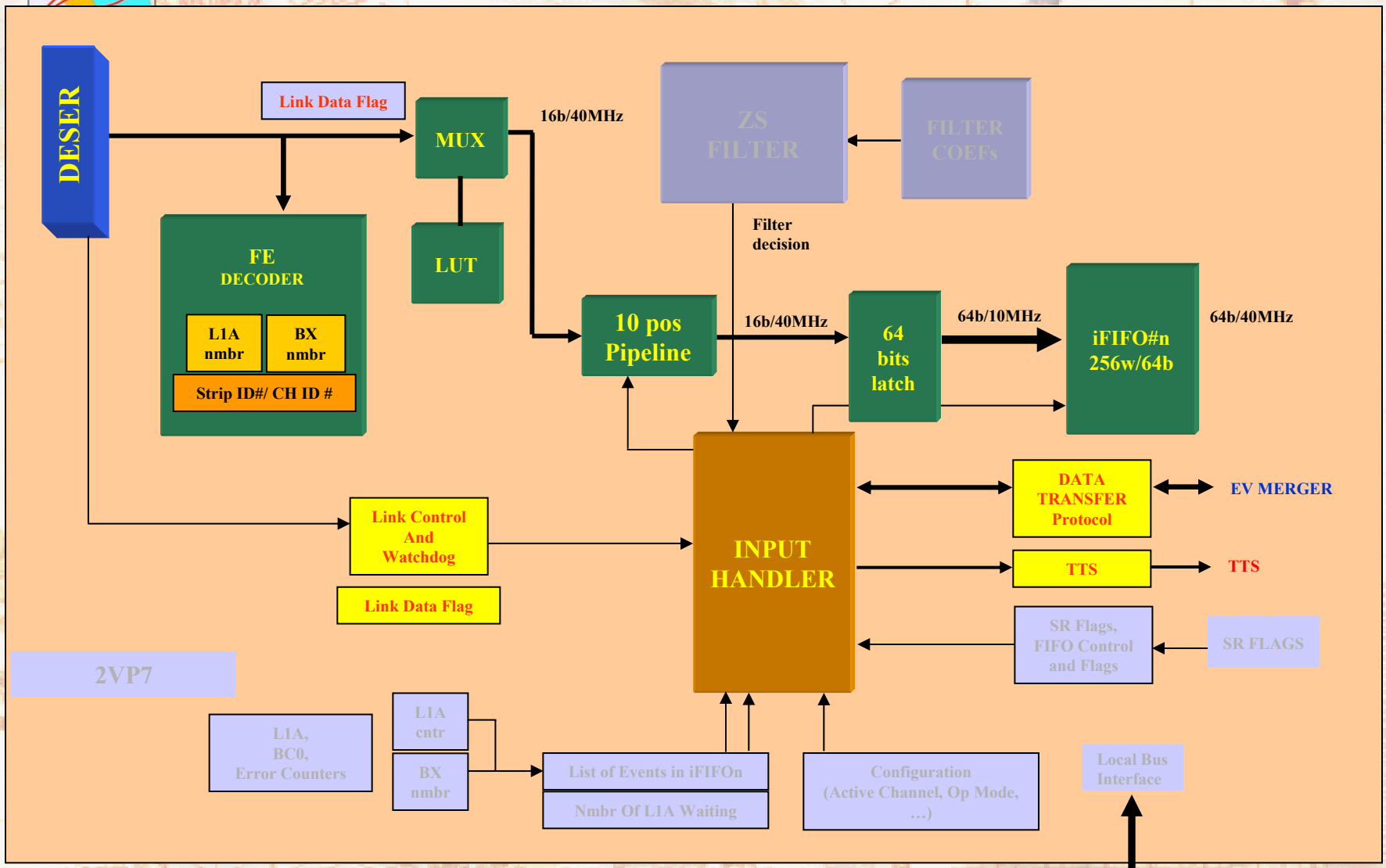
Full Readout



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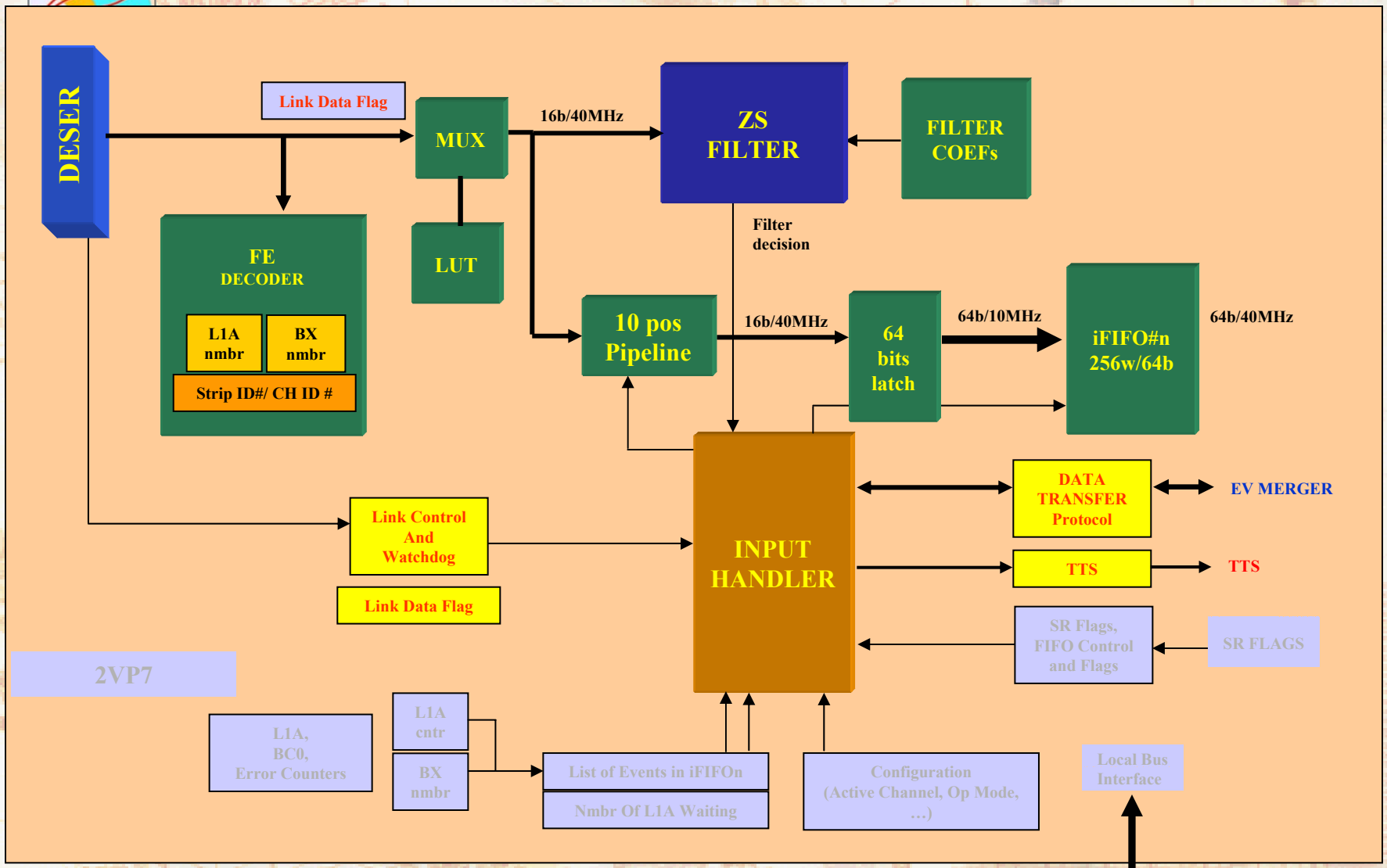
Zero Suppression



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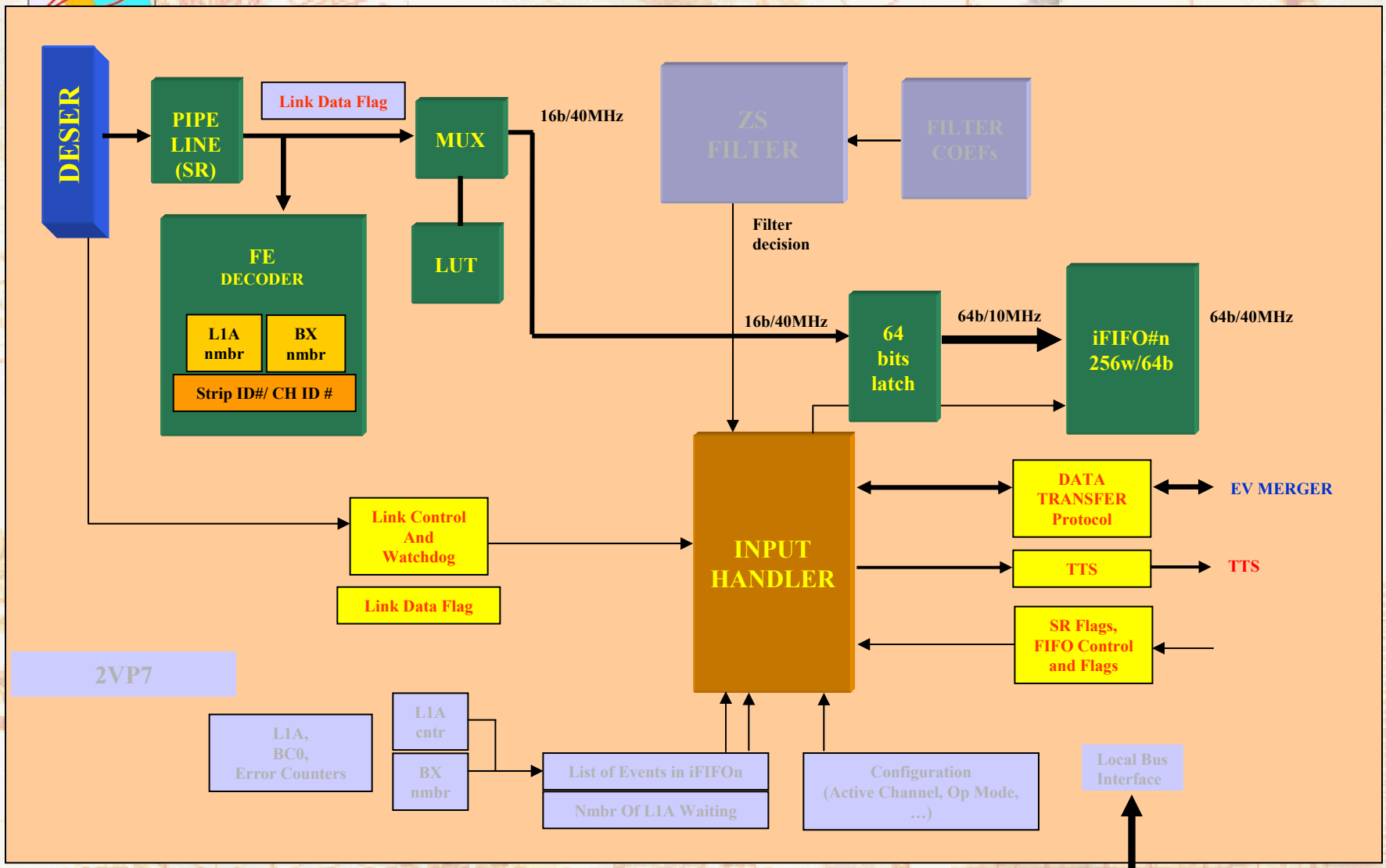
SR Decision



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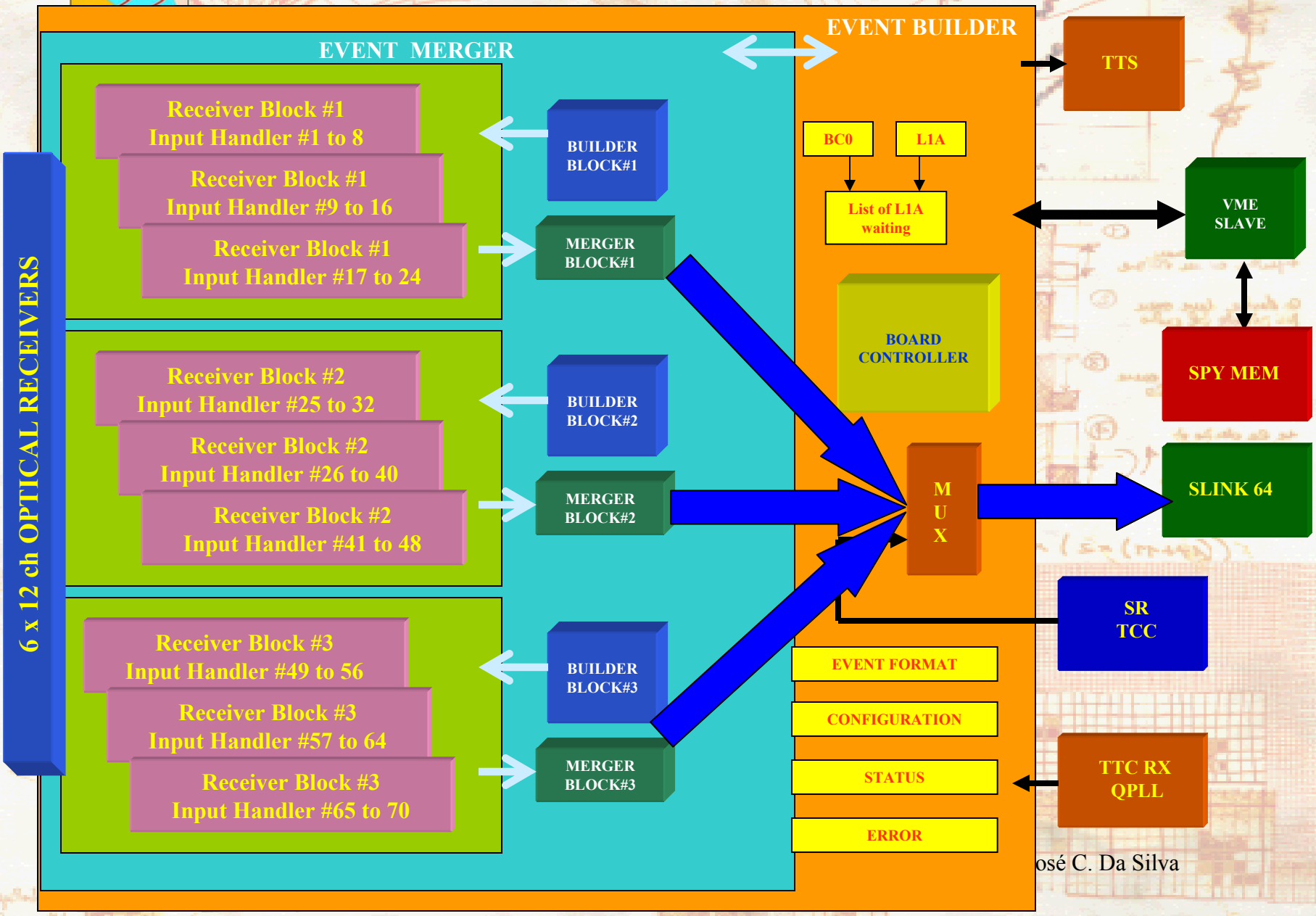
EVENT BUILDER BLOCK



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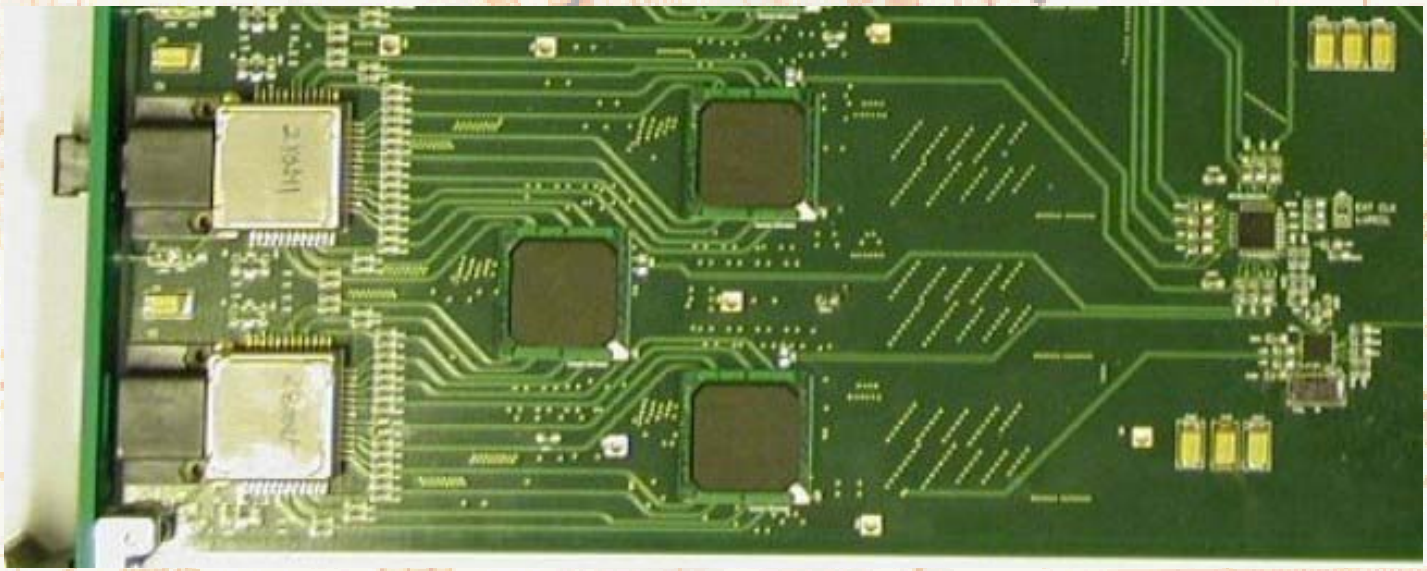
Input links test setup (1)

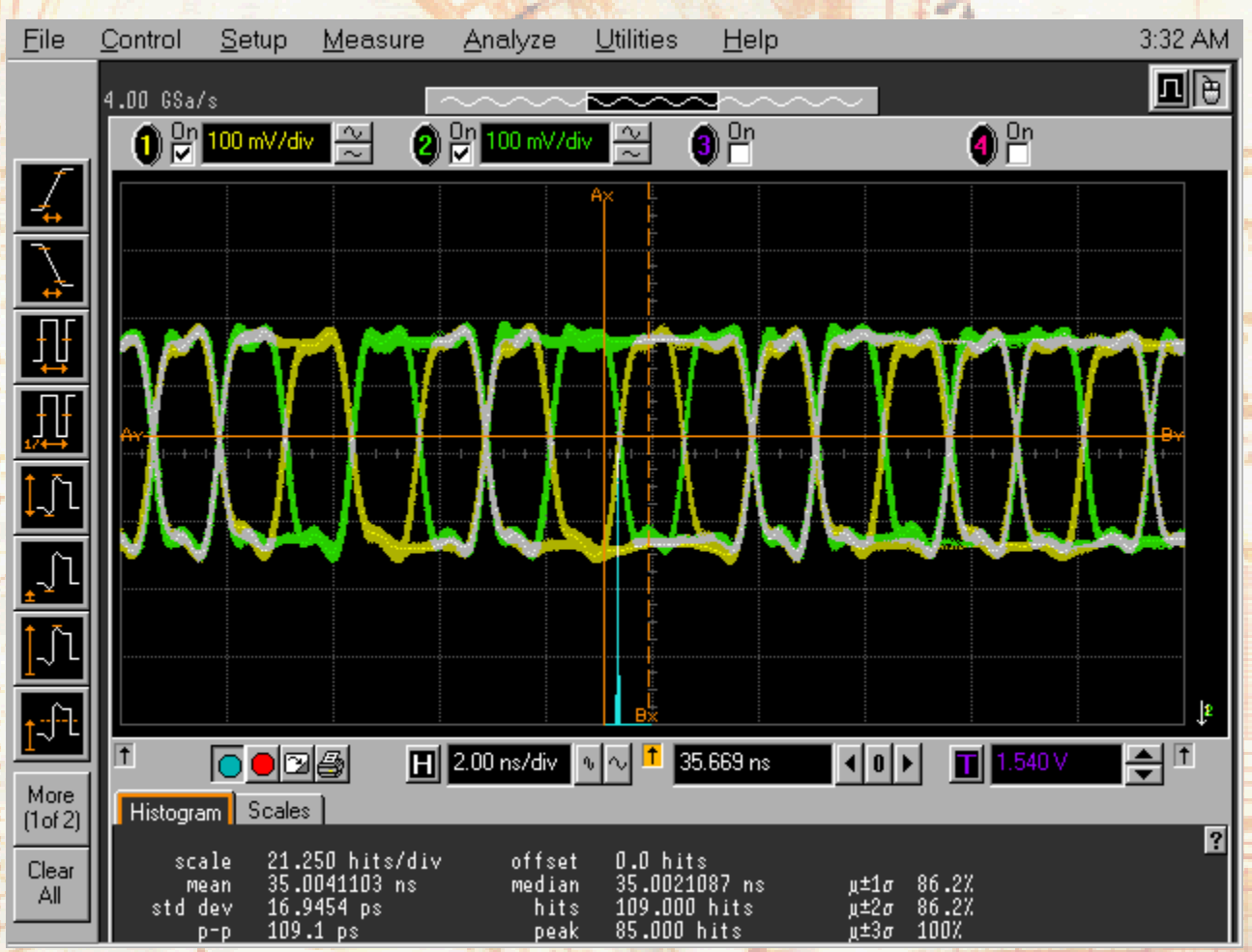
NGK and Virtex 2 pro



- Impedance controlled layers
- PCB Manual routing
- 12ch NGK rx
- 8 deserialisers per Virtex 2 pro

Input links test setup (3)

Differential Input Signal



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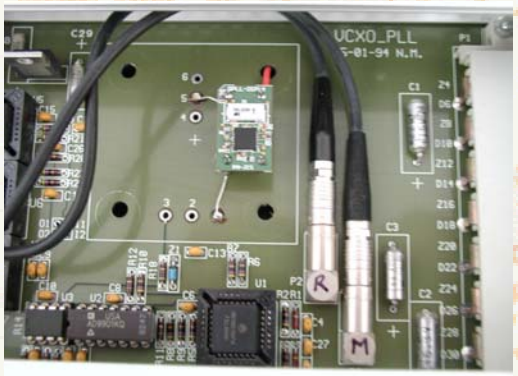
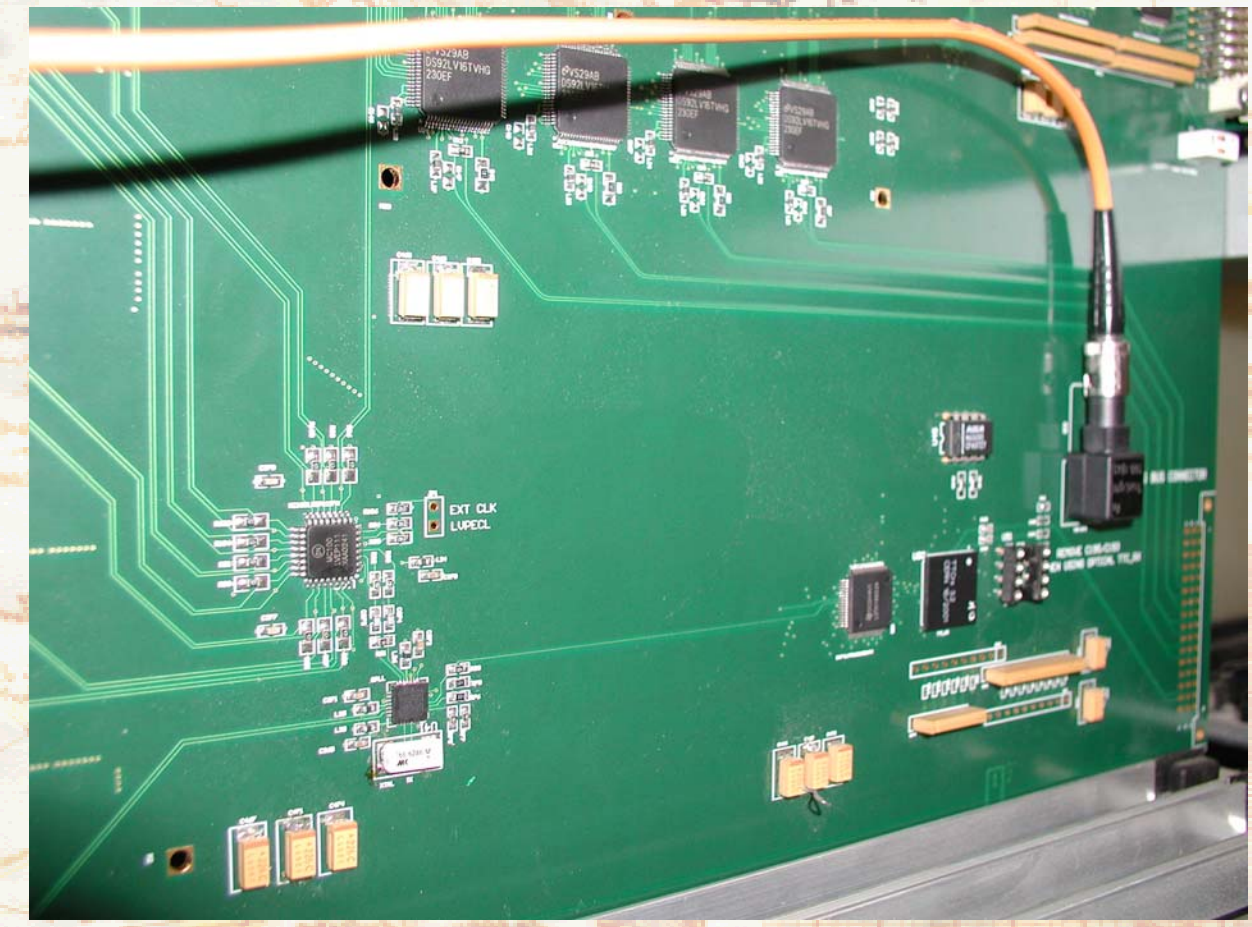
Deserialisers Reference Clock

QPLL – Deserialisers Refclk





Same Clock frequency

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Deserialisers Reference Clock

Refclk Jitter

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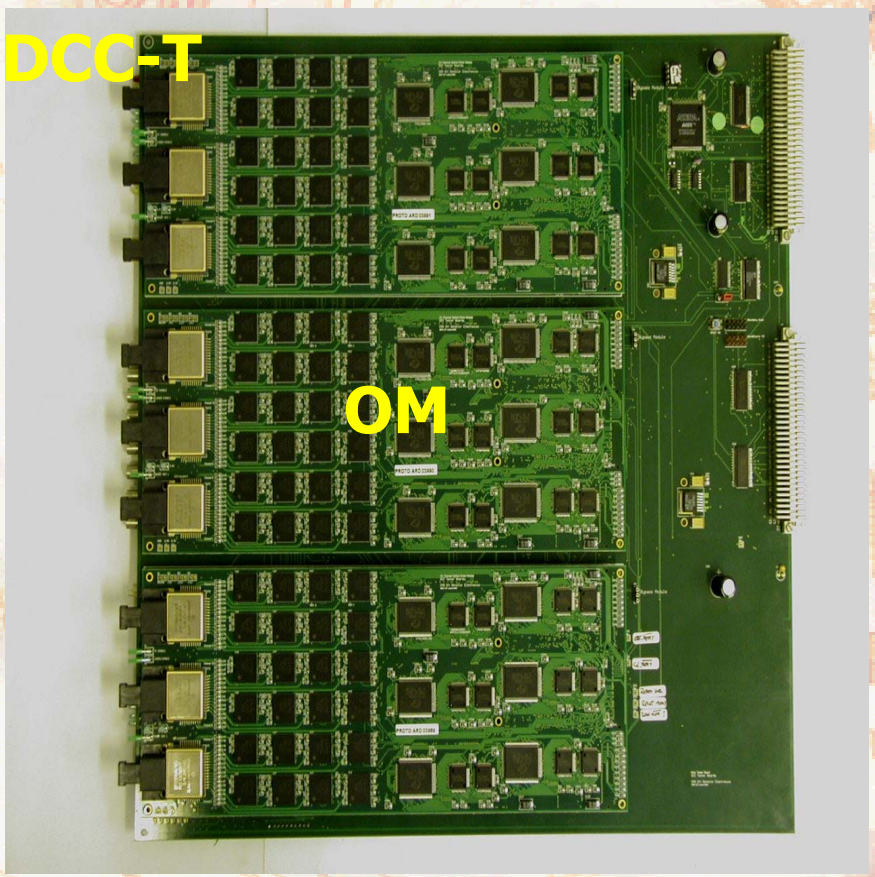
DCC Tester



DCC Tester (DCC-T)

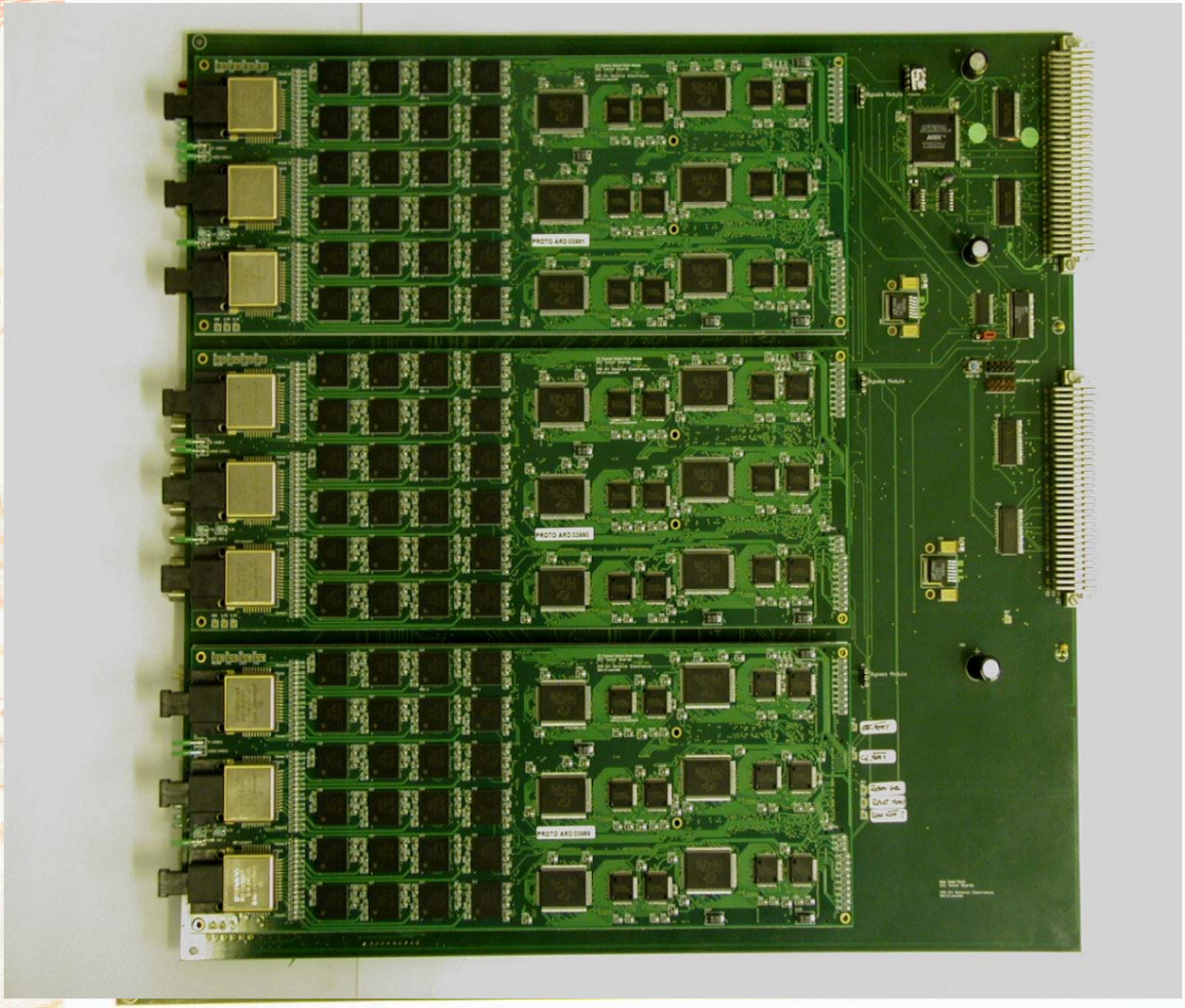
- **9U VME board, VME64x compliant.**
- **Emulates the DCC Interfaces (FE,SRP and TCC):**
  - **70 GOL links (2MEM +68FE working at 800MBit/s) by 3 Optical Modules (OM).**
  - **1 SRP GOL link.**
  - **4 TCC LVDS electrical links.**
- **Storage Capacity of 40 MBytes (~ 1000 Events).**
- **Controls the operation of the TTCVi**
  - **generates the LHC clock, the orbit signal, the L1A and the fast commands.**
  - **Synchronous Event transmission**

DCC Tester

DCC
Motherboard
Optical Modules
24 Channels
3 x 8 NGK tx

DCC and OM
Motherboard

Used as
TCC
Tester



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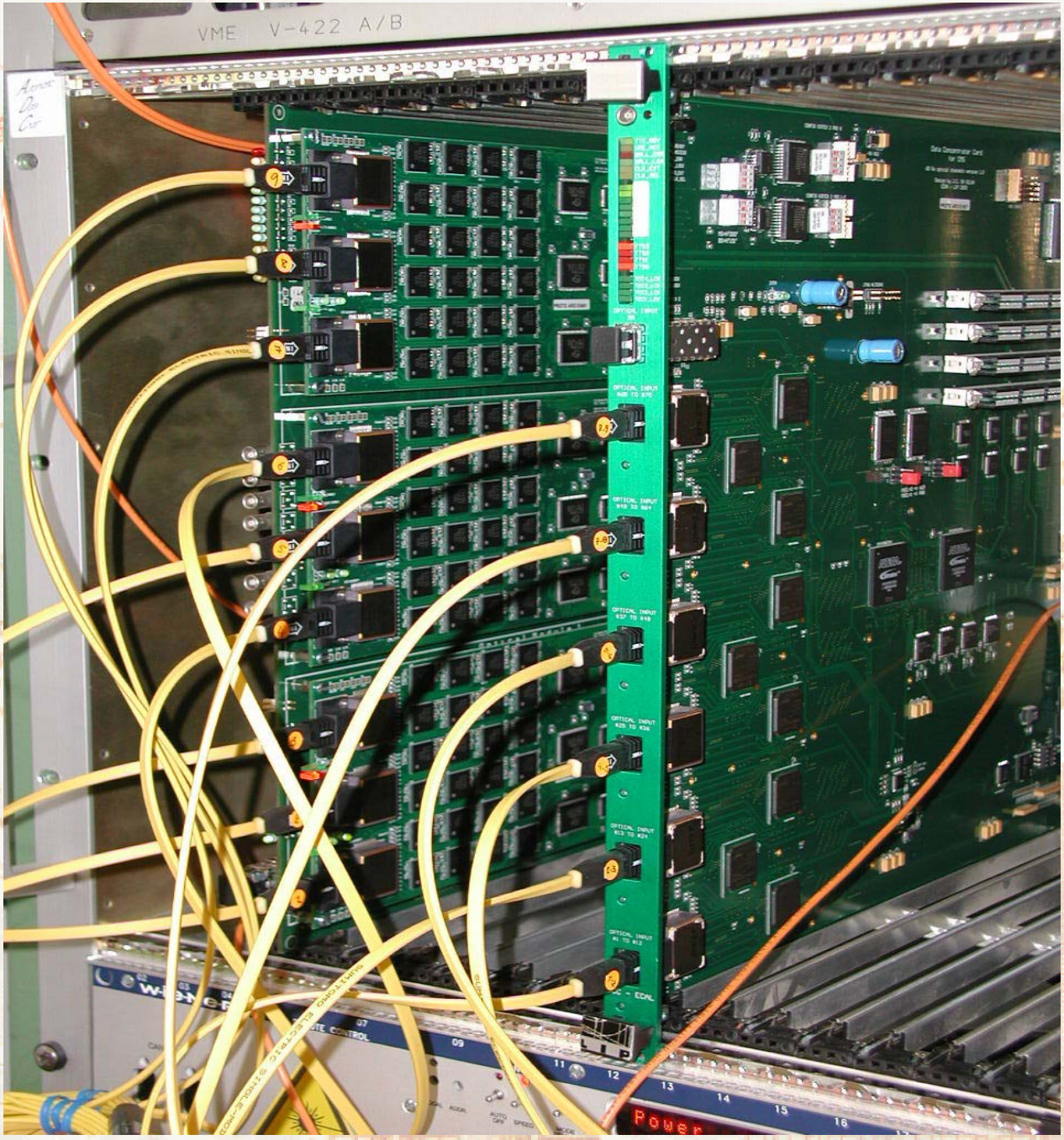
High Speed channels testbench

DCC Tester:
all channels sending data at L1A rate
(68 FE + 2mem)

DCC :
all channels receiving data correctly
(284w 16b / L1A)



Planning for Test Beam

- 2 DCC assembled / under tests
- Working Version of the DCC for Test Beam
- Integration with FE on BLDG11

  - Data transfer 8b/10b protocol work on 1st shot (GOH-DCC)
  - Data length received per L1A is correct
  - Data Format mismatch .

  - Debug all data building (software)
  - Test performances (VME/SLINK64) with present firmware.

-

Planning

- **Final Design review**

- **Production 2005**
  54 - CMS ECAL (+ spares)
  3 – RPC
  Preshower