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Pixel Multichip Module for the BTeV Experiment at Fermilab

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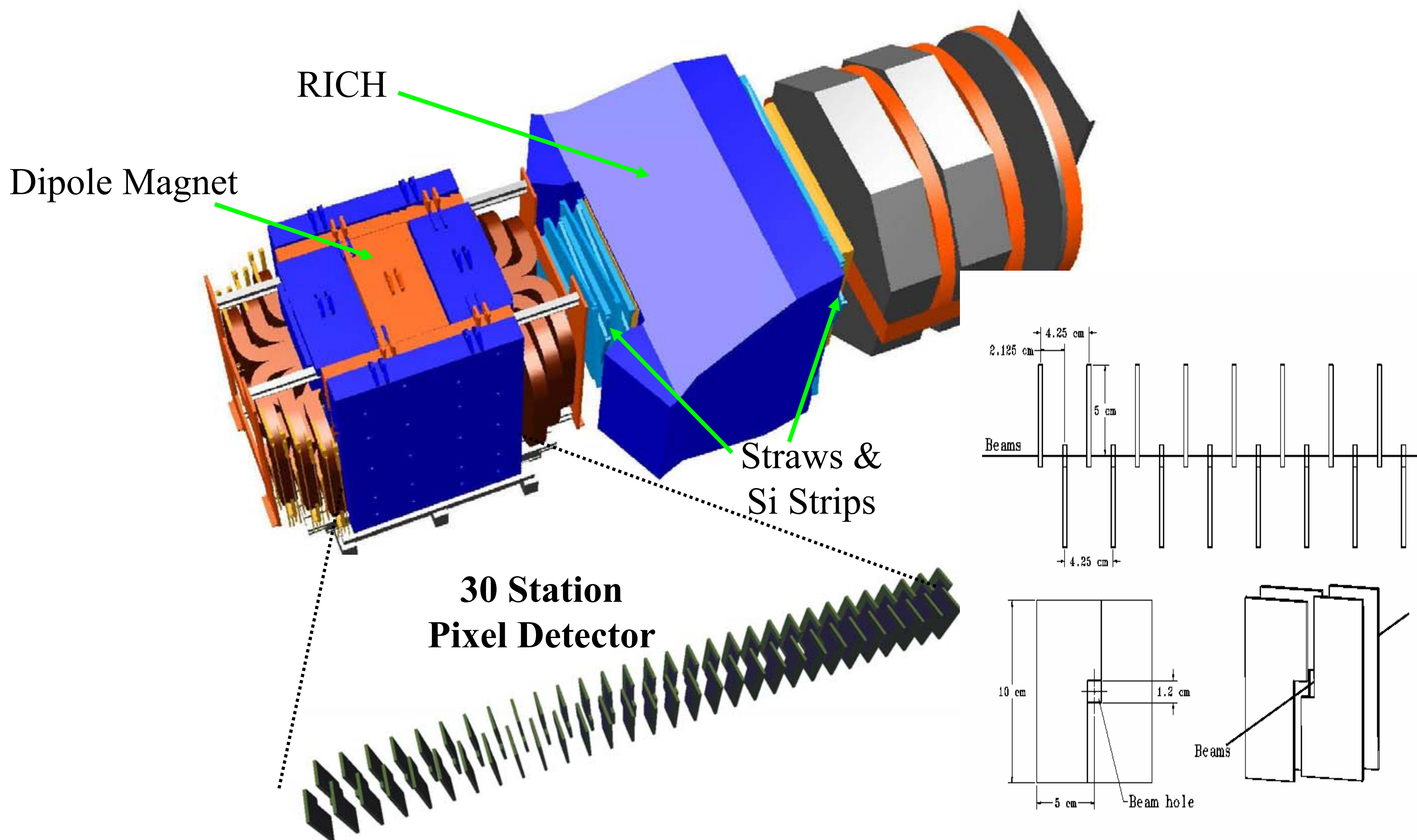
Outline

- Overview of the BTeV detector
- Electronics challenges
- Pixel data rates & readout bandwidth
- Pixel detector baseline design
- Flex circuit technical challenges
  - *Pixel multichip module prototype*
- Bump bonding results
- PCI test stand
- Characterization results
  - *5 chip module with sensor*
- Conclusions

BTeV Detector



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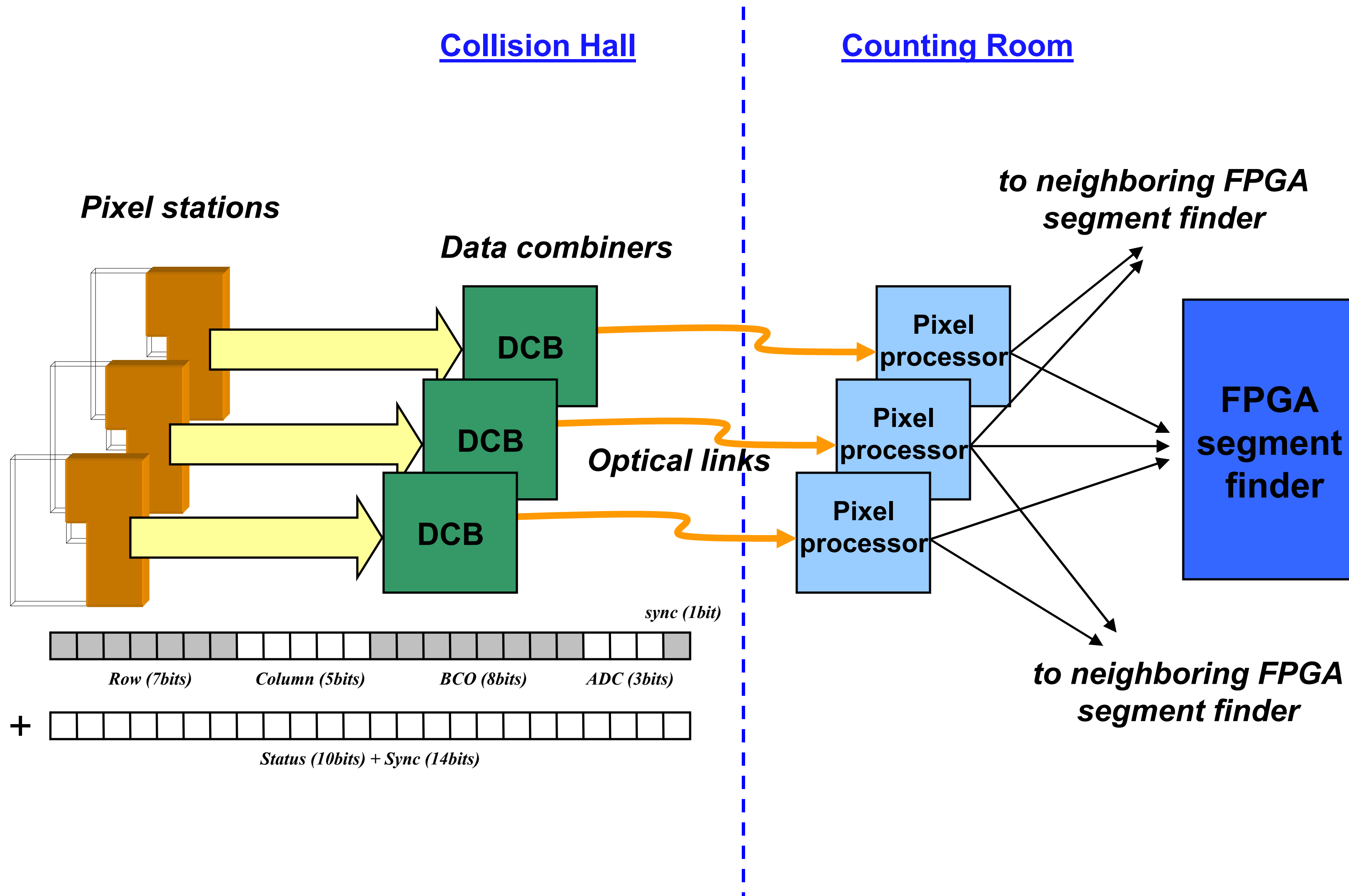
Challenge for Electronics, Trigger, and DAQ - I

- **From Joel Butler's presentation on Monday:**

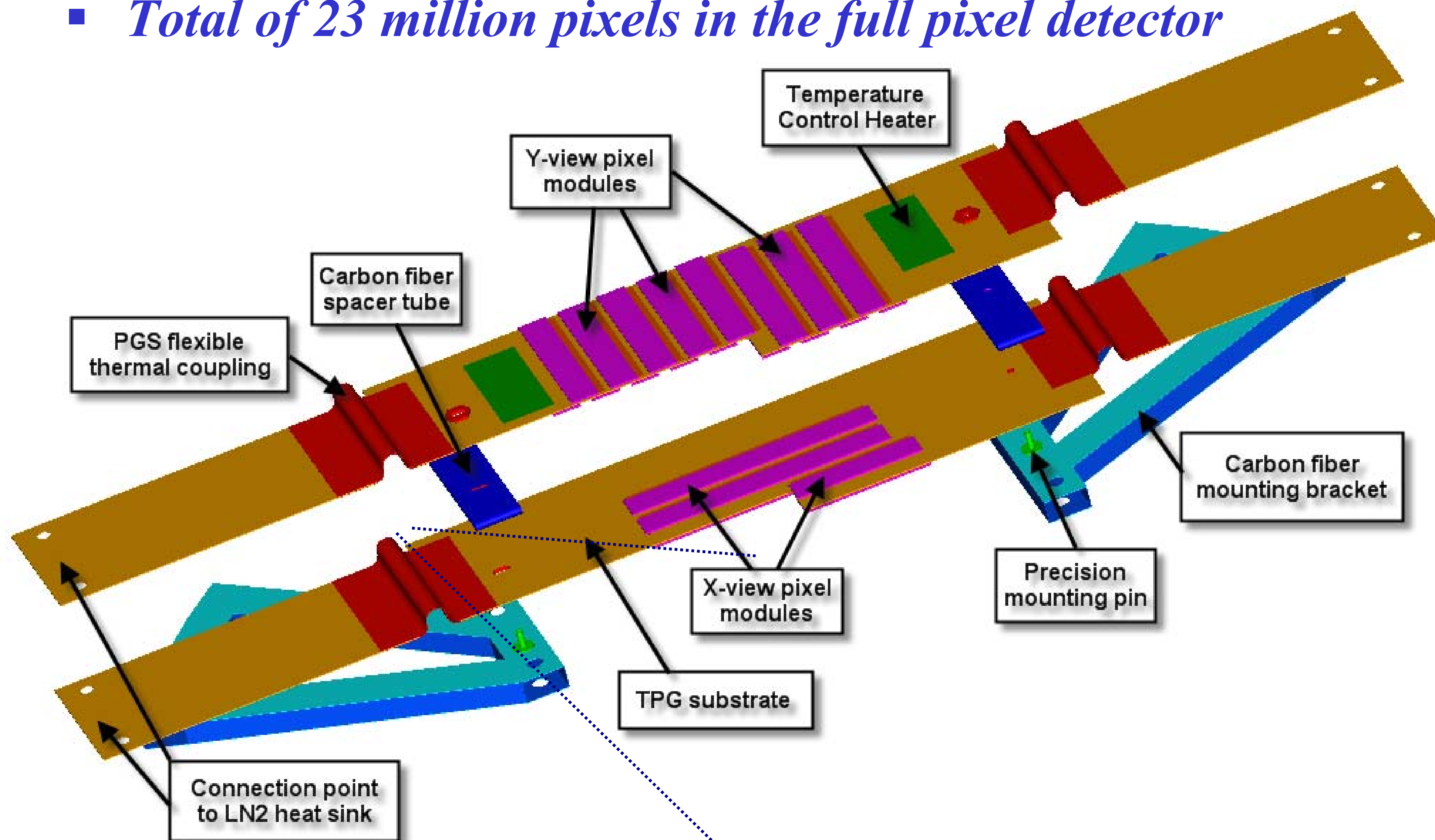
- **We want to select events (actually crossings) with evidence for a "downstream decay", a.k.a "detached vertex."**
  - **THIS REQUIRES SOPHISTICATED TRACK AND VERTEX RECONSTRUCTION AT THE LOWEST LEVEL OF THE TRIGGER**
- To carry out this computing problem, we must
  - **Provide the cleanest, easiest-to-reconstruct input from the vertex tracking system – hence the silicon Pixel Detector**

Pixel data readout

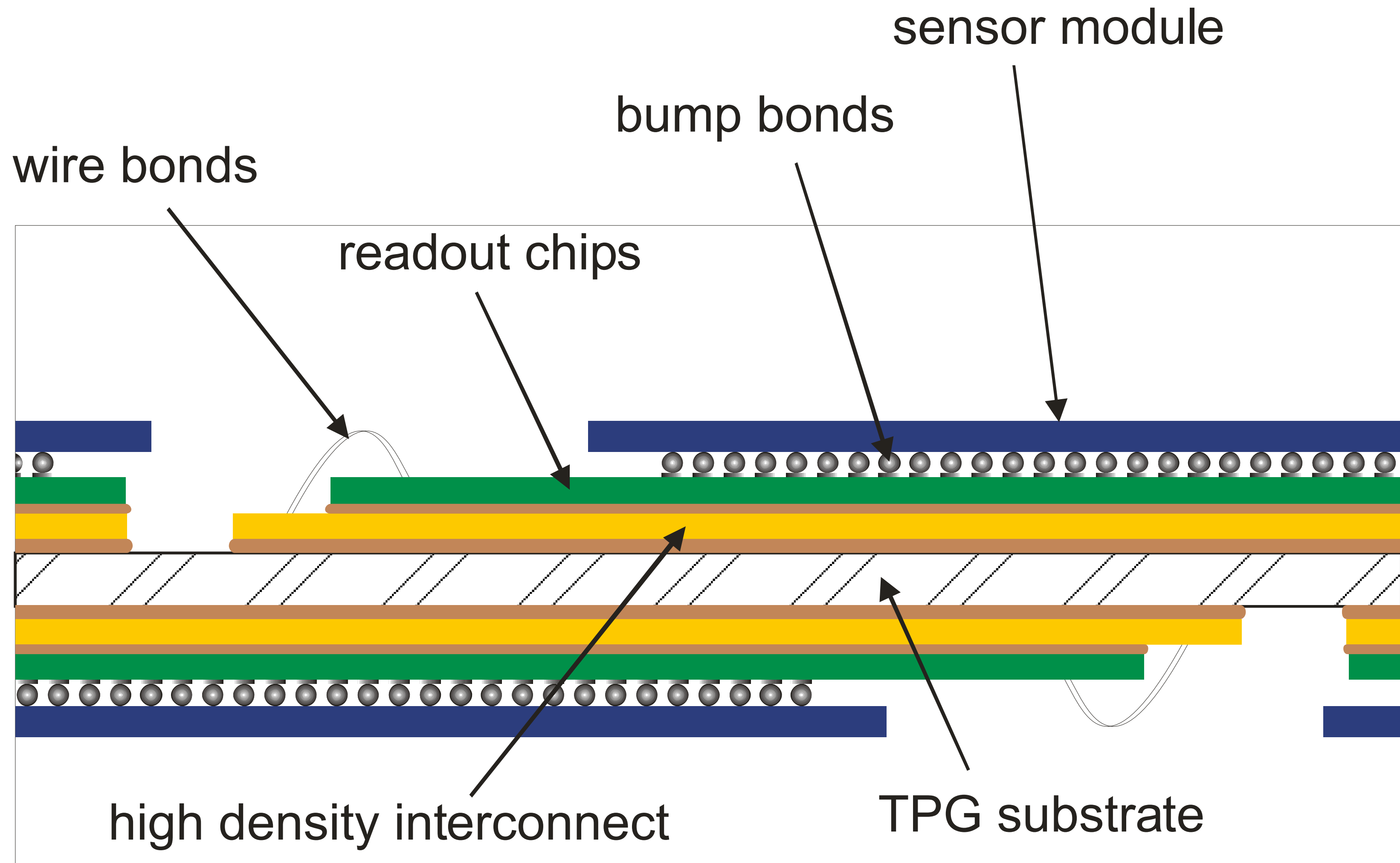


Pixel Detector Plane

- *380,160 pixels per half-station*
- *Total of 23 million pixels in the full pixel detector*

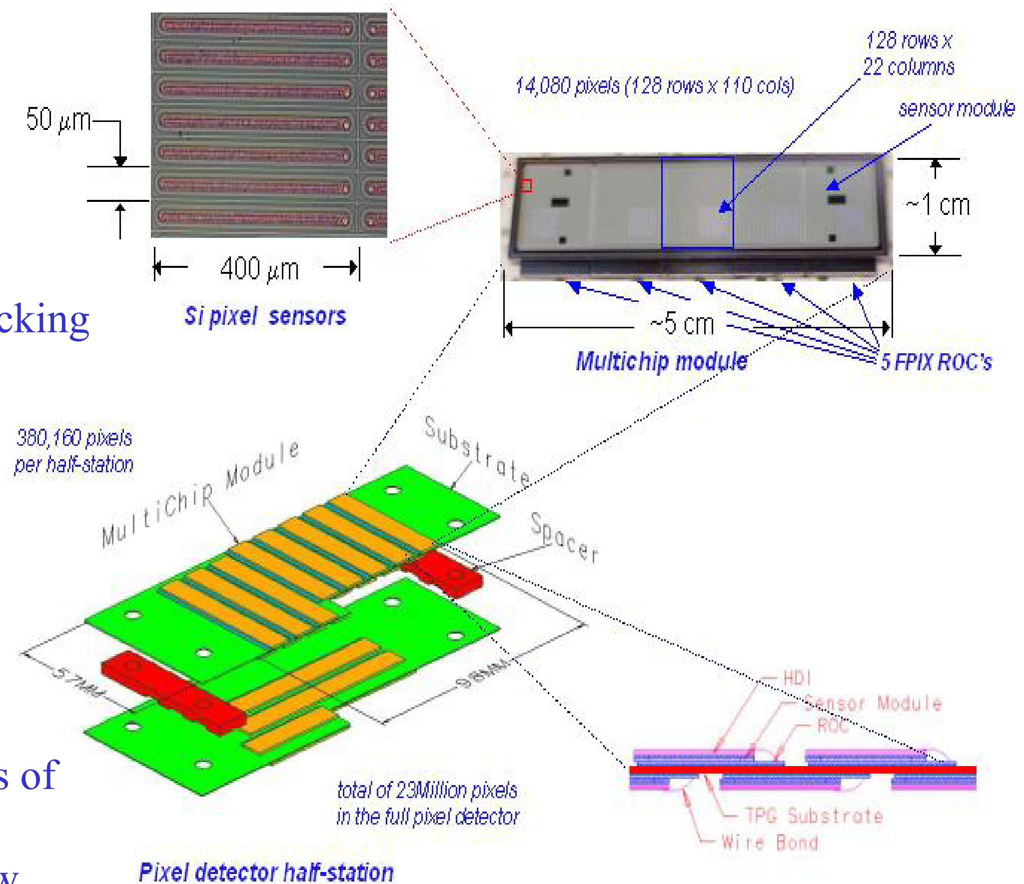


Cross Section - Pixel Detector Plane

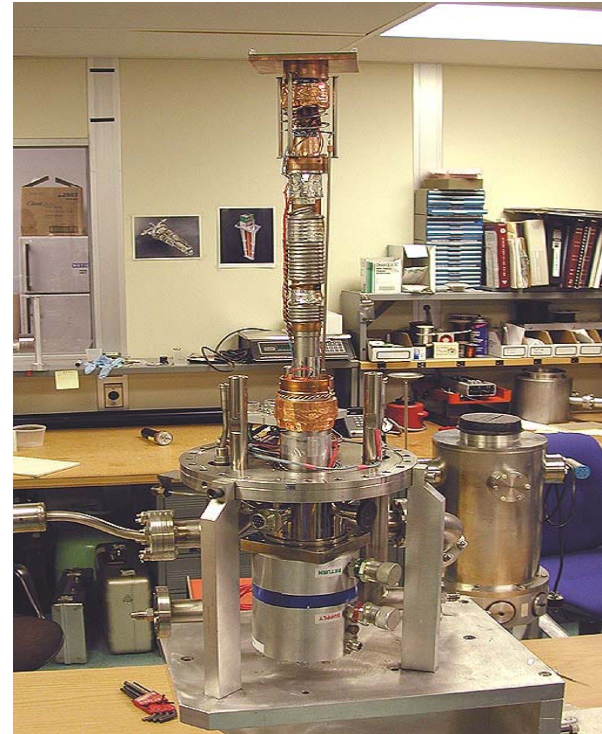


Pixel Detector Building Blocks

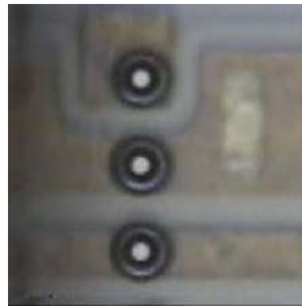
- Pixel sensor bump-bonded to readout chip (FPIX)
- Fine segmentation
  - 23 million 50μ x 400μ pixels
- High power and low mass
  - Front end electronics in the tracking volume
  - High power density (~3kW)
  - Low material budget
- Multi-Chip Module (MCM)
  - Four types (4, 5, 6, 8-chip)
  - FPIX mounted to HDI
- Pixel "views"
  - Modules mounted to both faces of TPG substrate
  - Larger coverage in "bend" view
  - Orthogonal pixel orientation on pair of views in each half-station



Bump Bonding Progress

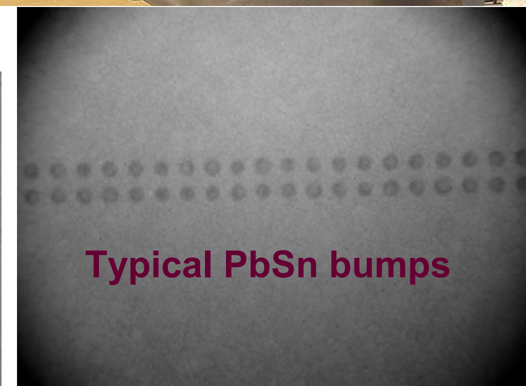


- Investigating In and PbSn bumps
  - Recently received parts using thinned wafers
    - 200µ chips and 250µ sensors
  - Six chips tested (~18k bumps)
    - All tested channels work!



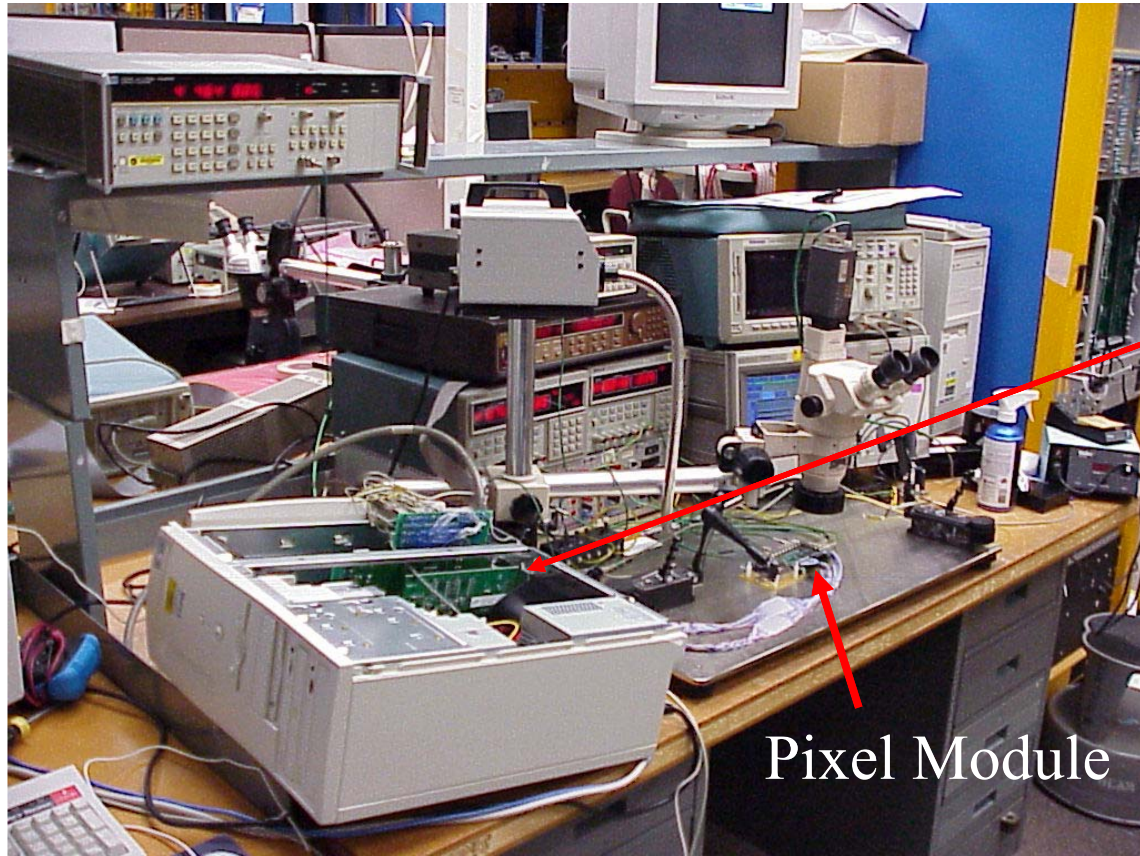
- Concerns:
  - Yield for thinned wafers
    - AIT indium bumps not so good
      - 10% of chips fell off
    - VTT solder bumps very good
      - >400K bumps inspected, one flaw seen
  - Effects due to thermal cycling
    - CTE mismatch with substrate
- Bump bonding studies
  - Thermal cycle studies on glass-Si modules
  - Thermal cycle studies on detectors
  - Radiation effects
  - CTE mismatch effects
  - Connectivity at cryo-temperature
  - X-ray imaging of bumps
    - Works well for PbSn

"Flaw" in PbSn bumps

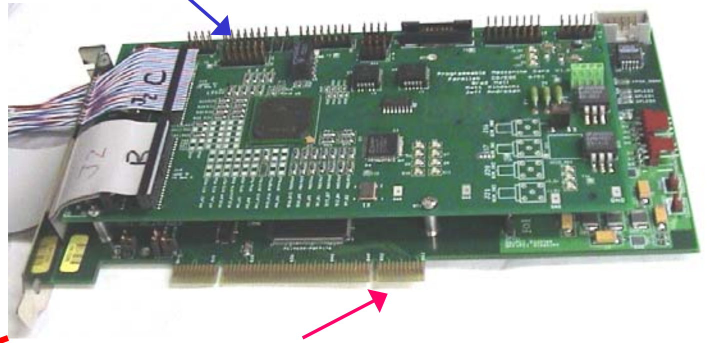


Typical PbSn bumps

PCI Test Stand



Programmable Mezzanine Card (PMC)



PCI Test Adapter (PTA) Card

- FPGA controlling all functions
- PCI interface
- 4MB of RAM
- Daughter card interface (IEEE1386)
- JTAG
- USB
- RS232

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HDI Technical Challenges

- Fine-pitch traces
- Multilayer (4 layers)
- Small via pads
- Limited choice of materials: Problems with outgassing, ferromagnetism, and low temperature
- Small production quantities (by industry standards)

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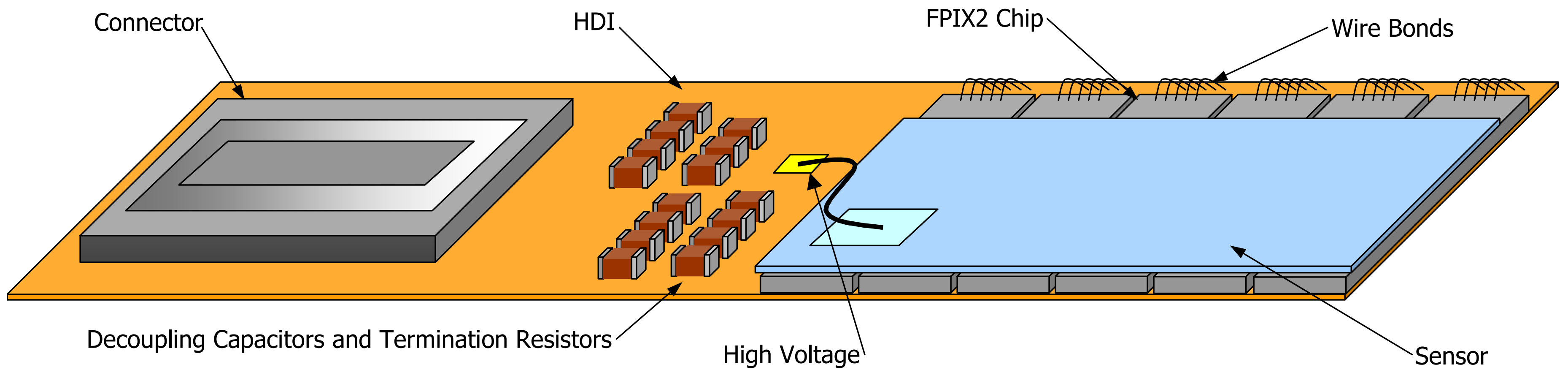
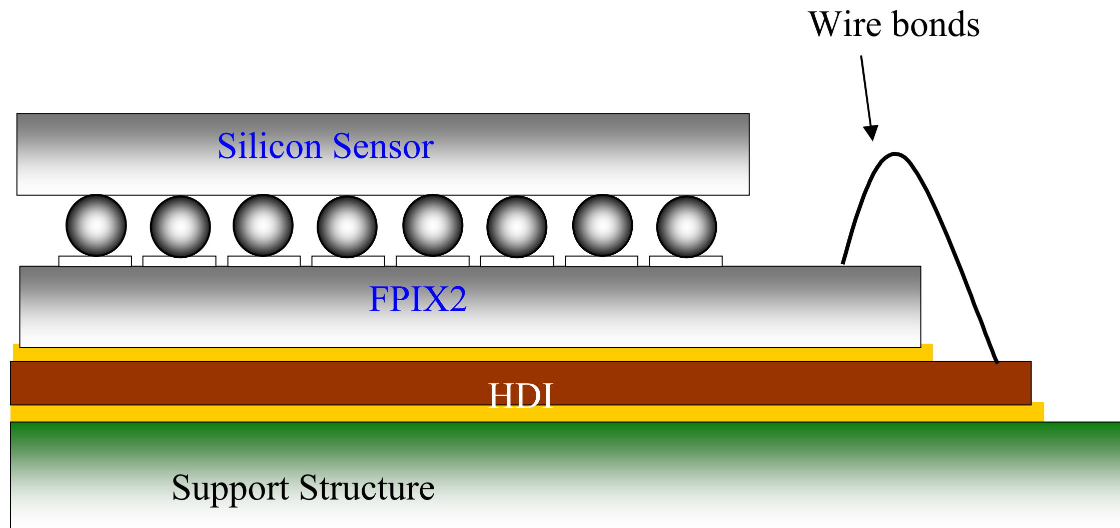
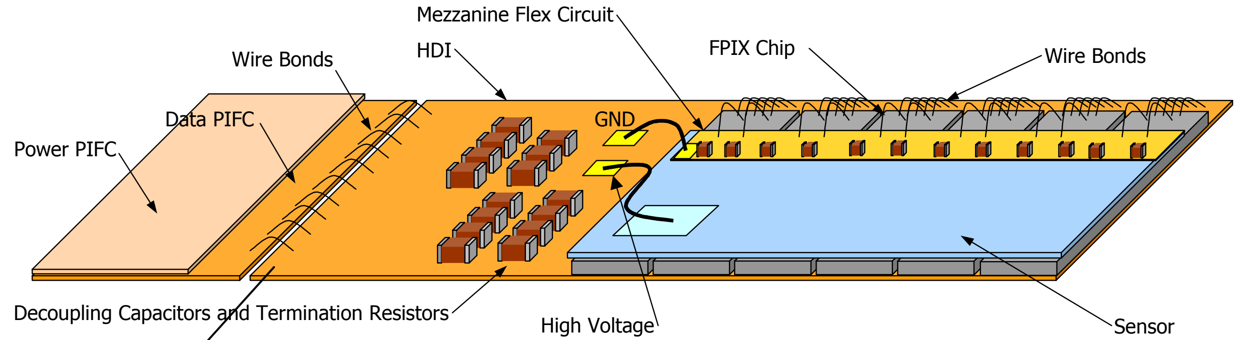
Prototype pixel module

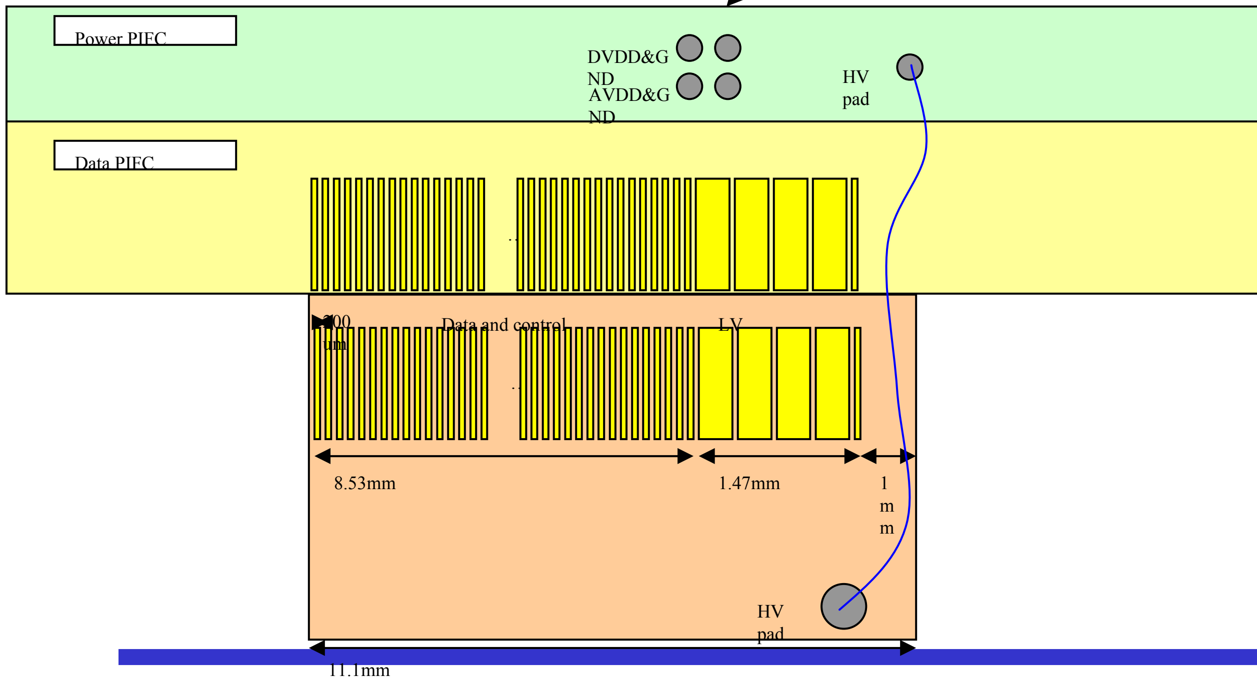




NOT TO SCALE

HDI to PIFC wire-bonding





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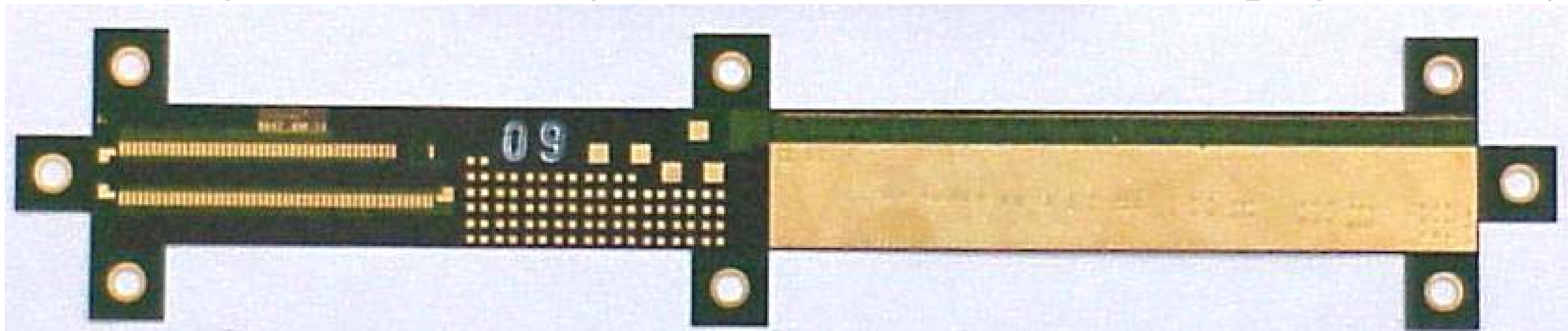
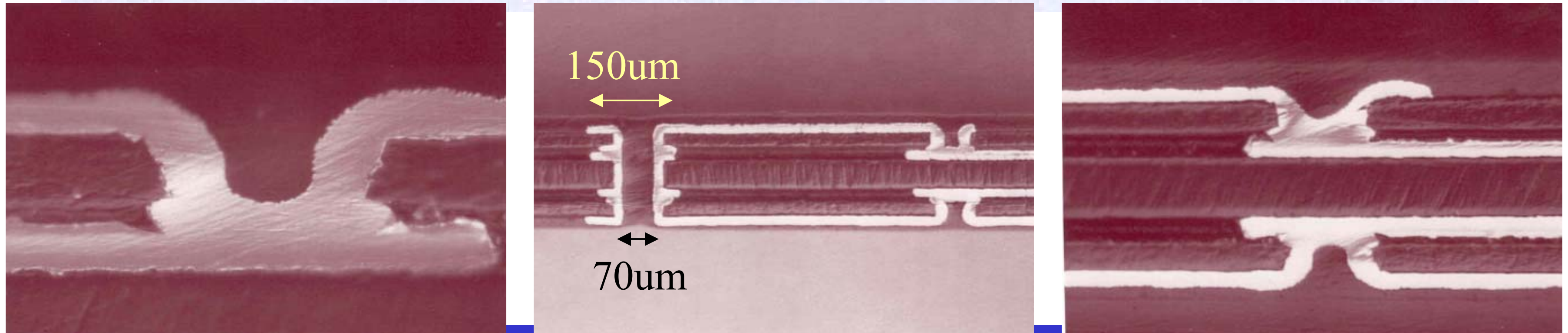
6 chips (FPIX2) HDI design

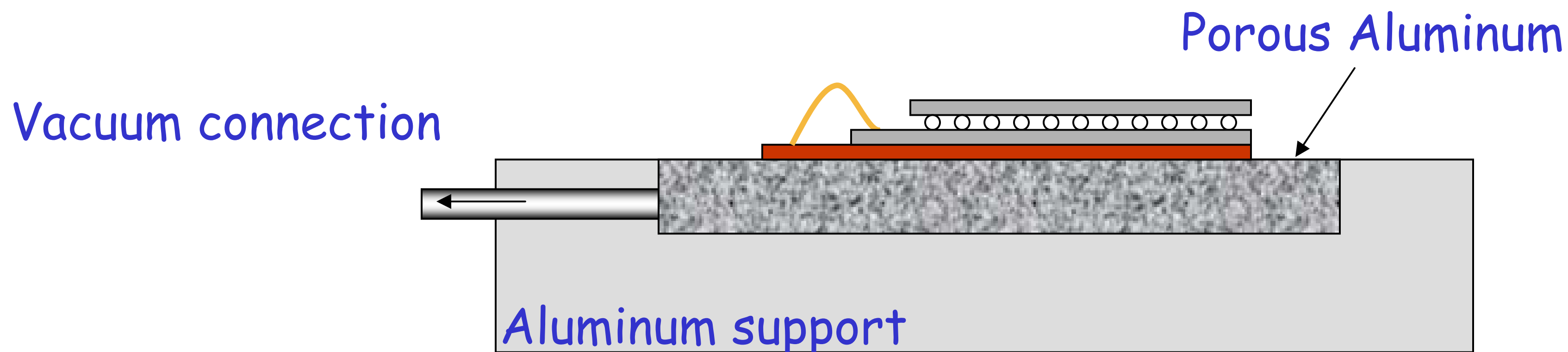
HDI made by Dyconex

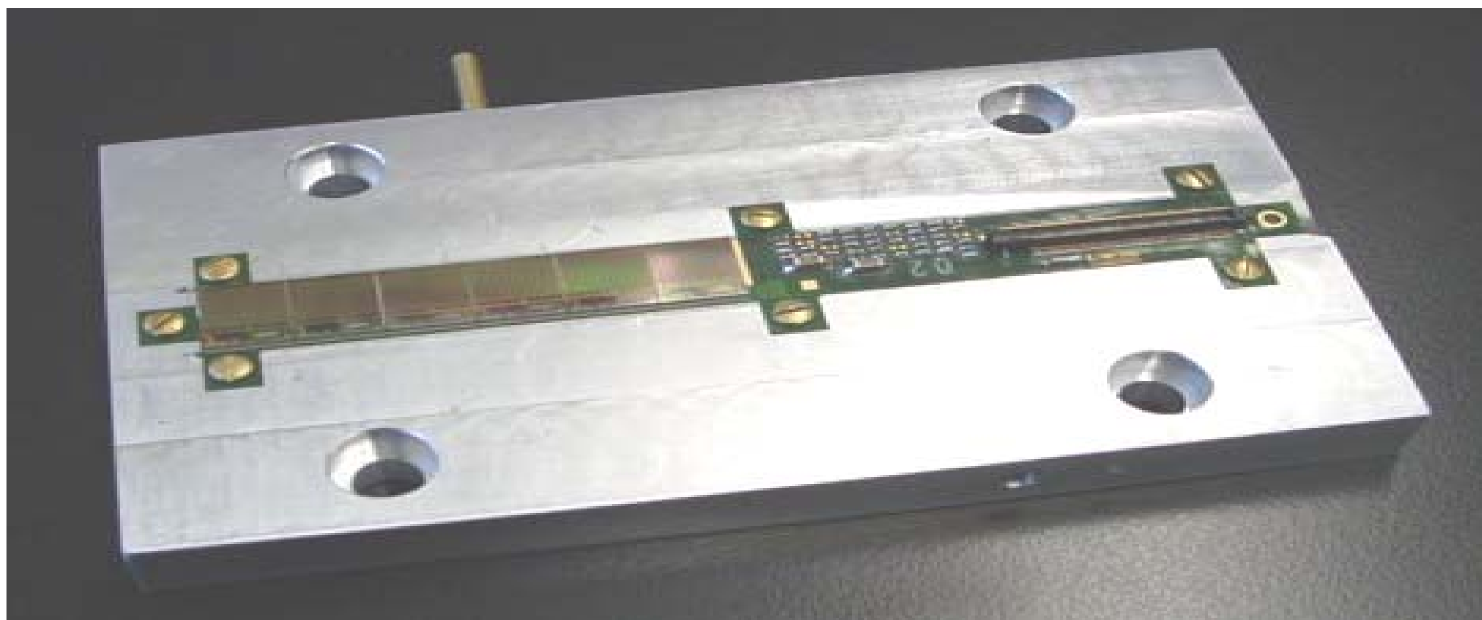
- **Dimensions:** 109.3mm x 11.1mm
- **Line width:** 50µm
- **Line to line clearance:** 50µm
- **Metal layer thickness:** 10µm
- **Number of layers:** 4
- **Via pad/hole:** 150/70µm
- **Lamination:** 25µm epoxy
- **Film thickness (polymide):** 50µm





Pixel Module Mechanical Assembly





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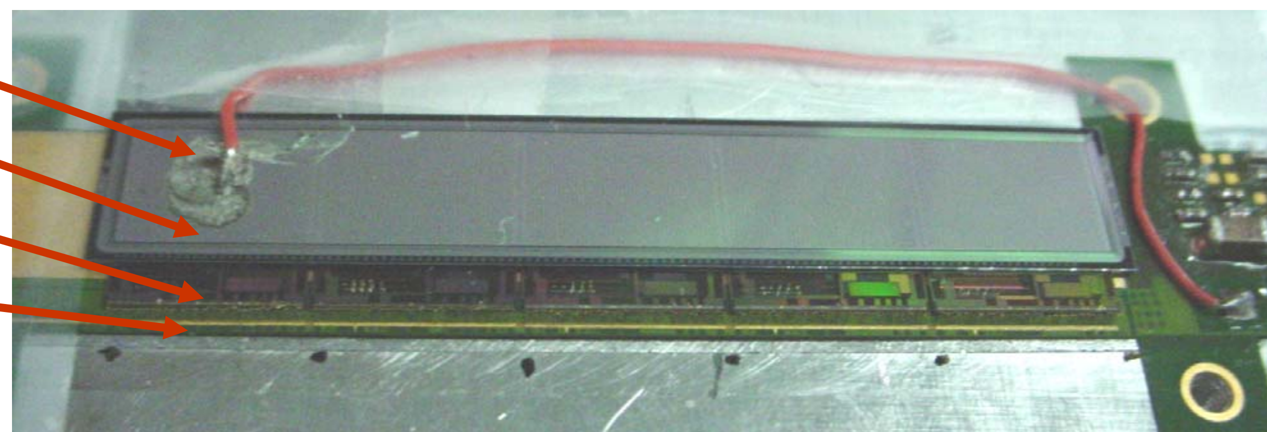
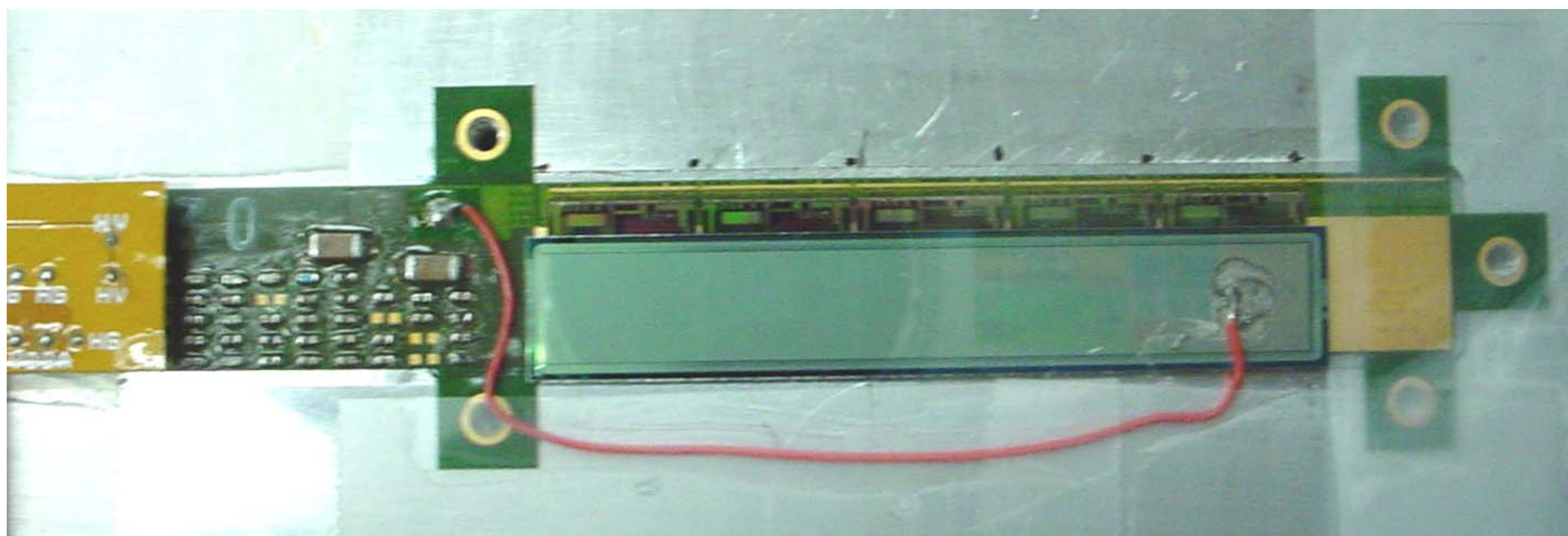
5-chip Pixel Module

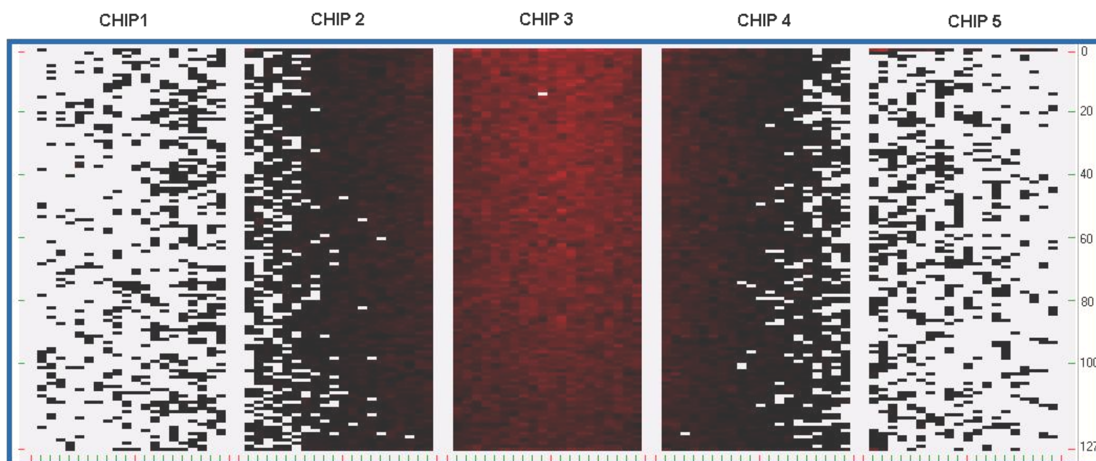
H.V.
Sensor
FPIX2
HDI





First 5-chip Module with Thinned Silicon

FPIX2A - 5 CHIPS MODULE
Vbias=-250V@85nA
IDDA=234mA@2.5V IDDD=232mA@2.5V



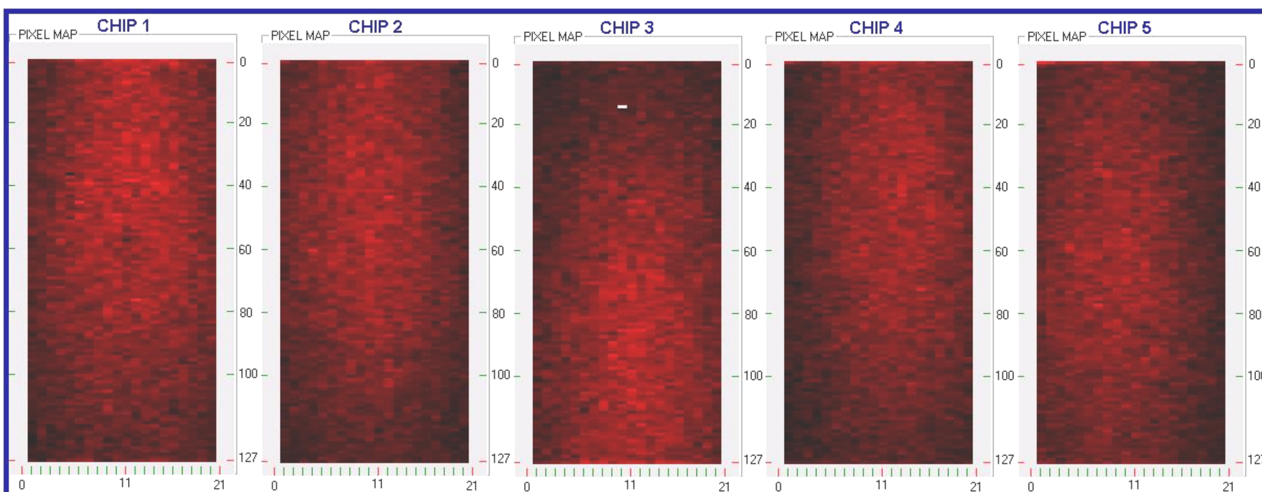
PICTURE 1

All 5 chips are setted to a threshold of 16300 electrons to avoid noise cells.

Column 0 and 21 are killed in all chips due the fact that the threshold in this columns is different because the pixels in this columns are larger.

In picture 1 a beta gun source (Sr90) was kept iluminating the module centred on chip3 during 4 minutes the source was orthogonal to the module and distant 4cm from the center of chip 3.

In picture 2 a individual hit map of each chip was done, a beta gun is placed 2 cm from each chip for 2 minutes of exposion per chip.



PICTURE 2

NUMBER OF HITS

Characterization Results [e$^-$] – 5 chips

		CHIP 1	CHIP 2	CHIP 3	CHIP 4	CHIP 5
Threshold	μ	4000	4000	4000	4000	4000
	σ	200	180	217	194	180
Noise	μ	76.4	80.6	90	87	90
	σ	7	8.6	7.8	8.2	9

Bare die results

Mean Noise: 70e$^-$

Mean Threshold Dispersion: 231e$^-$

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Characterization Results [e^-] – 1 chip

CHIP 1							
Threshold	μ	4000	3700	3300	2700	2300	1800
	σ	200	178	172	165	152	164
Noise	μ	77	92	92	79.7	79	77.6
	σ	7	8.6	9.5	8.6	8	9.9

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Conclusions

- Pixel Module
  - Good agreement between circuit simulation and real measurements
  - Good performance characteristics.
  - No significant increase in noise and threshold dispersion when compared with previous single chip prototypes
  - No crosstalk problems between the digital and analog sections of the readout chip and HDI.
- FPIX2 is "almost" the production readout chip
- Hybridized (FPIX2+sensor, single chips and modules) tested in test beam
- For the remainder of this year
  - Tests of radiation damaged hybridized parts.
  - Bench and beam tests with the single-chip and multichip pixel modules (including irradiated parts).

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END

Data Rate

- **Chip data rate depends on:**
  - **Size of the active area**
  - **Distance from the beam**
  - **Number of bits in the ADC output**
  - **The way the data is arranged**

Readout Bandwidth

Readout Bandwidth

- Hottest module ~737 Mbps
- All pixel hit data needs to be readout, once pixel detector is used in the lowest level trigger
- Tradeoff between flex circuit density & readout clock frequency