

The Powering Scheme of the CMS Silicon Strip Tracker

A. Bocci^{1,2} R. D'Alessandro^{1,2} S. Paoletti² G. Parrini^{1,2}

¹ Dip. di Fisica Univ. di Firenze, Sesto Fiorentino (Firenze) Italy

² I.N.F.N. Sezione di Firenze, Sesto Fiorentino (Firenze) Italy

e-mail: paoletti@fi.ifn.it

Abstract

The silicon strip tracker of the CMS experiment comprises ~15000 silicon strip detectors, divided into ~2000 "power groups" to share power, control and cooling services. The high voltage (0-600V) biasing the detectors and the low voltages (1.25V and 2.5V) required to power readout and control electronics are provided by a modular system of "power supply units" (PSU), which has to deliver ~15 kA inside the tracker volume. The voltage drop along the ~50m long cables is compensated using the sense wires technique. The designed system and the PSU implementation are described in detail. Also a cable of new design, featuring low resistance and low impedance, has been developed for this specific application. The performances of the system with PSU prototypes and close-to-final detector configurations are shown.

I. THE CMS SILICON STRIP TRACKER

The tracker of the CMS experiment [1] at the LHC collider is composed of a central pixel detector, located at a small distance ($R < 15\text{cm}$) from the beam pipe, and a silicon strip detector (SST), which extends 5.5m longitudinally and 88cm radially (from 22 to 110 cm from the beam pipe) covering the pseudorapidity region $\eta < 2.6$ [2].

The SST is subdivided into:

- four inner concentric layers ("Tracker Inner Barrel", or TIB);
- two mini-endcaps, complementing the TIB system, named "Tracker Internal Disks" (TID);
- six concentric outer layers of detectors ("Tracker Outer Barrel" or TOB);
- two endcaps, each one composed by nine disks of detectors, named "Tracker Endcap" (TEC).

The entire SST will be kept at a temperature of -10°C , in order to minimize the degradation of the sensor performances due to irradiation, due to the increase of the sensor dark current and reverse annealing effects. This will also help maintain the full depletion voltage at a reasonable level: namely below 600V after ten years of operation at nominal LHC luminosity [2].

The readout is based on the APV25 front end chip [3]. Each detector module is equipped with either four or six

APV25 chips, depending on the number of strips to be readout.

The digital control of the detector modules is based on "Communication and Control Unit" (CCU) chips. Each CCU takes control of more than one module. Several CCUs are daisy-chained to form a so-called CCU-ring (or control group).

Analog outputs and digital control signals, between the detector modules and the "outside world", are transmitted via optical fibres.

II. POWER GROUPS

Each SST detector module requires:

- one high voltage (HV) regulator (0-600 V) to bias the sensors;
- two low voltage (LV) regulators (+2.5V and +1.25V) to power the FE chips and the other circuitry.

The sensor's leakage current, even after 10 years at LHC, should still be well below 1mA [2]. The typical current (per module) on the 2.5V line ranges from $I_{2.5} \sim 510\text{mA}$ (4 APV25 chips) to $I_{2.5} \sim 750\text{mA}$ (6 APV25 chips). Correspondingly, the current on the 1.25V line ranges from $I_{1.25} \sim 260\text{mA}$ to $I_{1.25} \sim 390\text{mA}$. The digital control optoelectronics require one +2.5 V line. The total power consumption of one CCU-ring is about 5 W, depending on the number of CCU units present in the ring.

Silicon strip modules are conveniently grouped into 1944 "detector power groups" in order to share power, cooling and control services. Grouping criteria are governed by the mechanics (power groups are parts of the mechanical structure) and by the density of channels (a higher powering granularity is adopted close to the interaction point). Table 1 shows the main parameters characterizing the current and power requirements of the tracker groups. The total current to be delivered inside the tracker volume is $I_{\text{TOT}} = I_{2.5} + I_{1.25} \sim 15$ kA.

Table 1: the SST power consumption

| | n. APV | 12.5 [A] | 11.25 [A] | Pw [W] |
|--------------|---------------|---------------|--------------|---------------|
| Avg./group | 37 | 5.2 | 2.4 | 16.0 |
| Max./group | 56 | 7.6 | 3.6 | 23.7 |
| Min./group | 12 | 1.6 | 0.8 | 4.9 |
| Total | 72 784 | 10 066 | 4 731 | 31 079 |

The digital control optoelectronics requires a distinct powering system. The control services are grouped to form 352 CCU-rings, each of them powered by one 2.5V power source. The total power consumption of all the CCU-rings is less than 2 kW, a small fraction of the total.

Figure 1 represents the total power to be sourced by the power supply system as a function of the total current consumption. The zero of the x-axis is set at the typical consumption $I_{TOT} = 15$ kA. The already noticeable difference in power consumption between the no cables and the cables included situation, becomes even more so as the current increases from the typical value. The power supply system is anyway designed to cope with a current consumption of up to 1.7 times I_{TOT} and a cable length up to 50m.

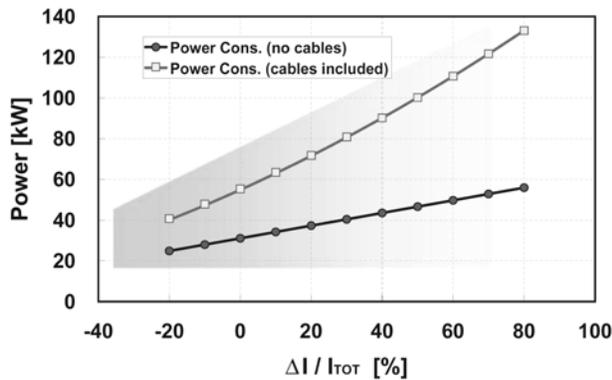


Figure 1: The SST power consumption with 45m of cables.

III. DESIGN OF THE SYSTEM

The power supply project for the CMS SST was initiated by the Florence CMS group in the year 2000 according to the following guidelines:

- the system is modular, based on "Power Supply Units" (PSU) serving the detector groups and equipped with both LV and HV regulators, and on a modified version of PSU, equipped with only one 2.5V regulator, serving the CCU-rings and integrated into the same powering system;
- LV regulators are placed outside the tracker volume. The sensing technique is adopted in order to ensure the nominal voltage values (+2.5V and +1.25V) on the load;
- PSUs feature a hard-wired safeguard system, ensuring the safe operation of the system;
- the PSU regulators are served by two external +48V DC sources, coupled by means of the DC-DC technique: one source (48VP) for the final power stage of the regulators, the other (48VS) for the service electronics.

PSUs are lodged in standard crates (19" wide, 6 U high) and controlled by a set of external Array Controllers (A.Co.), through a CANBUS communication link. Array Controllers are interfaced to the tracker "Detector Control System" (DCS)

and to the CMS "Detector Safety System" (DSS) via "Supervisor Units". The crates themselves provide the required CANBUS, Interlock and Reset bus lines.

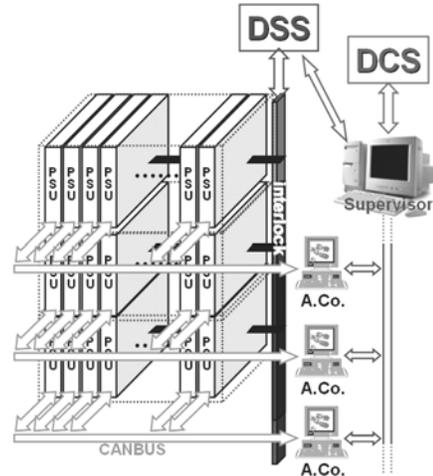


Figure 2: Scheme of the power supply system.

Each PSU features one 1.25V ($I_{1.25} \leq 6A$) and one 2.5V regulator ($I_{2.5} \leq 13A$), two distinct HV regulators ($I_{HV} < 10mA$ each) and one micro processor (μP) which, connected to one Array Controller through the CANBUS link, controls the regulators and monitors their status, voltage and current values. LVs and HVs are software programmable and remotely controlled. The presence of two distinct HV regulators allows some flexibility in the way sensors of the same power group are biased.

LV regulators ensure the stabilization of the voltage at up to 50m distance on active loads (filtered by up to several hundreds of μF capacitors) deploying the sense wires technique. They can compensate voltage drops up to 4V. LVs and HVs have distinct reference voltages and their return lines are connected together on the load. The regulators are "floating": i.e. they are electrically isolated from the surroundings (48V DC lines, contiguous PSUs etc.); the isolation is at least 100Ω , at 5 MHz and higher at lower frequencies. The input/output of the μP with the exterior are opto-coupled.

HV ramps are software programmable (by default: 10 V/s ramp up and 50 V/s ramp down; the emergency ramp down is 200 V/s).

The following commands and alarms are handled by PSUs through the μP intervention:

- **Reset:** it forces the PSU to ramp voltages down to zero. The reset may be addressed, to each individual PSU, either by the Array Controller or by the manual reset button. A reset may be also generated by the watch-dog circuit monitoring the PSU's μP . A General Reset line is also available on the crate, which triggers a reset command in all PSUs hosted in the crate;
- **Interlock:** up to six interlock lines are available on the crate. In the presence of an interlock signal each PSU of the crate ramps voltages down to zero. The PSU can

be operated again only when the interlock signal is removed;

- **48V DC failure:** it is generated by the power distribution network in case of failure of the main power, triggering the fast ramp down of all regulators and leaving the system in a safe configuration.

The PSUs feature also the following hard-wired safety systems:

- **Current Limiters:** they keep the current flowing out of each regulator within the (software set) "Current Limit" (CL) value. Their intervention sets the "Over Current" status (OC) and switches OFF the regulator;
- **Low Voltage Comparators:** set the "Over Voltage" status (OVV) whenever the voltage difference of any sense wire pair or the voltage output of any voltage regulator is outside the settled range. An OVV status is for example set in case of sense wires shorts or exchange. The OVV status forces all regulators in the PSU to switch OFF;
- **Temperature Sensors:** all voltage regulators are inhibited if the temperature rises above 70 °C.

IV. IMPLEMENTATION OF THE SYSTEM

After experimenting on a few PS prototypes the designed system has been successfully implemented using CAEN technology. In the implemented system PSU pairs are lodged inside one mechanical drawer (6U x 55 x 4.4 cm²) to form one "Power Supply Module", or PSM.



Figure 3: Two power supply modules lodged in the crate

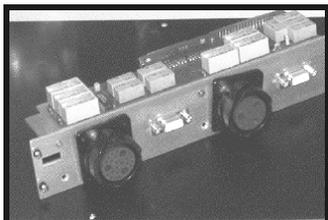


Figure 4: One PSM "back board"

The front of the PSMs is easily accessible to the operator and features a manual reset button, status and alarm LEDs and a series of status and alarm test points for each PSU.

Figure 3 shows two PSMs lodged inside one crate. The back side of each PSM is connected to an extension board ("back board" fig. 4), which holds the connectors for the power cables, HV fan-outs and a custom area equipped with "D" connectors routing the signals of the tracker ambient sensors out to the DSS system.

Nine PSMs are hosted in one crate. Each crate has two back-planes: the "back-plane1" hosts the PSM connectors, Cu-bars for the 48V DC, CANBUS communication lines, the "General Reset" track, the six interlock lines and the 48VP/VS failure signal tracks. The "back-plane2" is formed by the back-boards and holds the cable connectors.

Up to six crates are located in one 52 U high rack; one "Array Controller" (the CAEN A1676 "branch controller") controls all the PSMs located in one rack, through 6 CANBUS links, one per crate. Up to 16 racks are controlled by one Supervisor, the CAEN SY1527 model. Two SY1527 are thus sufficient to control all the 1944 power groups distributed on 20 racks.

V. OPERATIONAL ENVIRONMENT

The CMS detector will be located in the "Underground Experimental Cavern" (UXC), while the control-room of the experiment will be in the "Underground Service Cavern" (USC), shielded against radiation and magnetic fields.

Placing the PS system in USC implies using more than 100 m long cables to reach the powered detectors; placing the PS system inside UXC, on "balconies" at a distance of around 10 m from the beams crossing point, implies using shorter cables (around 50 m long) but exposes the PS system to the "Hostile Environment" (HE) of a magnetic field up to 1 KG and to a neutron flux estimated to reach up to $4 \cdot 10^{10}$ n/cm² in 10 years of operation at nominal LHC luminosity.

The developed PSMs can be used either in the "Standard Environment" (SE) or in the HE by simply changing the DC-DC transformers, leaving the same mechanics and electronics.

One PSM full size prototype was tested under magnetic field in the H2 CERN facility and under neutron irradiation at the Louvain-la-Neuve (UCL) facility by CMS and CAEN experimenters. The tests performed have shown no relevant degradation of the conversion efficiency with magnetic field and no damages or irreversible faults under neutron irradiation [4].

CMS plans to locate the PSMs in UXC, while the Array Controllers and Supervisors will be placed in USC, around 100 m apart.

VI. THE LOW IMPEDANCE CABLE

Power cables have to cover a total distance of roughly 50m from the PSUs down to the tracker structures. They have to route the LV power, the HV, the sense wires and other

services bringing ambient information (humidity and temperature) from the tracker structure.

The connection is made by one 35-40m long cable placed mostly outside the CMS detector volume, and one ~5m long one lying entirely inside the CMS detector volume. The two parts are connected at the periphery of the CMS detector.

In the inner section the major issue is to keep the material budget as low as possible, so cables of various diameters with Aluminum power conductors are deployed in this part (Aluminum "Multi Service Cables", or MSC).

In the external longer section, major issues are the cost and the cable performance. Since the cable is part of the feedback loop of the voltage regulators, both the stability and the transient response of the PSU depend on the quality of the cables. The rule of thumb is that low impedance and low resistance are to be preferred, in order to reach better system performances. The Florence CMS group designed on purpose a new kind of cable, named "Low Impedance Cable" (LIC).

Figure 5 is a sketch of a LIC cable cross section. Ten twisted pairs are located in the core of the cable, and are used for sensing, high voltages and other services required. Fifty enamelled 0.6 mm² copper wires are displaced around the core, to form two concentric layers of conductors which bring the power. The disposition of the LV wires is such that any 1.25V and any 2.5V wire is flanked by two Return wires. This structure keeps low the inductive self coupling and maximizes the distributed capacitance. The number of RTN, 2.5V and 1.25V wires is such that $N_{1.25} \sim N_{2.5}/2 \sim N_{RTN}/3$, to minimize the power dissipation.

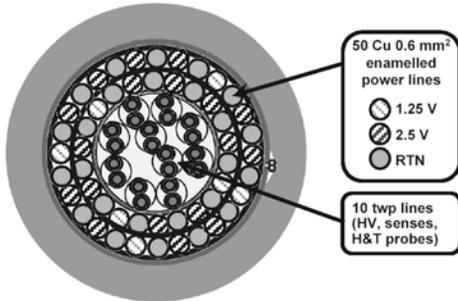


Figure 5: A sketch of the LIC cable section.

The resistance and impedance of the cables which are going to power the SST were accurately measured. Assuming that $I_{2.5} \sim 2 I_{1.25}$, a power dissipation factor (Q_R) can be calculated from the individual $R_{2.5}$, $R_{1.25}$ and R_{RTN} values: $Q_R = 2.5 \text{ m}\Omega/\text{A}^2\text{m}$ for the LIC cable and $Q_R = 11.5 \text{ m}\Omega/\text{A}^2\text{m}$ for the Al MSC cable. The capacitance, inductance and impedance measured (between the RTN line and the 2.5V line connected in parallel to the 1.25V line) for the two cables are respectively: 6.7 nF/m, 13 nH/m, 1.4 Ω/m for the LIC and 0.17nF/m, 206nH/m, 34.5 Ω/m for the Al MSC.

VII. THE SYSTEM PERFORMANCE.

The performance of various PSU prototypes was extensively tested (both in the laboratory and on beam tests)

with close-to-final detector configurations, checking the stability of operation, the OVV and OC protections, measuring the noise of the regulators, the AC isolation, the voltage regulator efficiency and the response to sudden current load variations.

A. Noise

The noise on LV regulators is required to be less than 10mV (measured peak-to-peak, ripple included with a bandwidth limit at 20 MHz) and the noise on HV regulators has to be less than 30 mV. Current PSU prototypes better this requirement approaching half of the requested value.

Performances as good as with a single detector with a dedicated power supply and short cables in the laboratory, were achieved in a beam test (CERN, X5 beam facility) using a group of six TIB modules powered by a PSU prototype, connected through a 150 m long LIC cable (see Fig. 6).

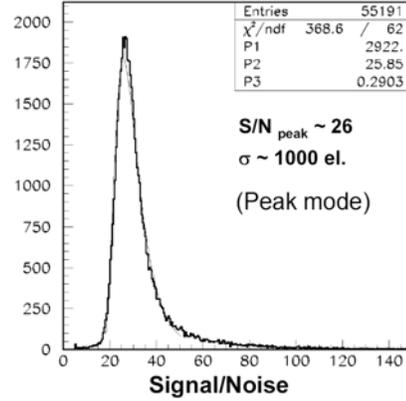


Figure 6: Signal-to-noise ratio measured with a TIB module in a beam test

B. Response to sudden current transients

Since the voltage drop across the LV distribution lines may be considerable (the present PSUs are designed to compensate up to 4 V drop), special care is devoted in order to prevent over-voltages affecting the powered electronics whenever an abrupt current consumption variation occurs. This is a common problem experienced when electronic devices are operated from a long distance using the sensing technique. The PSUs feature a non-linear sense circuit intervention which ensures the voltage recovery within 0.5ms.

This feature was tested through several laboratory tests, where the typical power distribution to the detector groups was reproduced. Figure 7 shows the result obtained working with one PSU prototype connected to passive loads through a 35m LIC cable. A sudden current consumption variation of 3A is generated simultaneously on both the 1.25V and 2.5V lines by means of a custom electronic circuit. This situation corresponds approximately to the simultaneous reset of all the APV chips belonging to one power group (a pessimistic assumption, since this operation would be forbidden by DCS). The fast PSU intervention keeps the duration of the voltage

spike within a few hundreds of microseconds. Its peaking value is around 0.5 V. No voltage oscillations are observed after the PSU intervention. This result depends also on the quality of the cable, which is part of the feedback loop of the regulators.

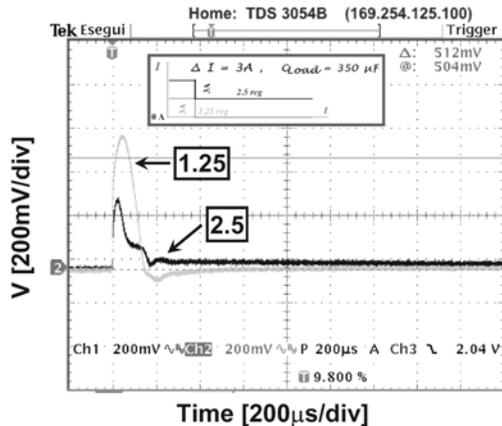


Figure 7: Overshoot test. 2.5V dark, 1.25V light.

C. Electrical isolation

By design, PSU channels have to be "floating", i.e. electrically isolated from the surroundings. Figure 8 shows the impedance measured between the LV/HV Return lines and the +48V Return line (laboratory ground) in a PSM prototype equipped with one "UXC" PSU (squares) and one "USC" PSU (circles). In both cases, the isolation is around 100 Ω at the APV bandwidth limit (the shaded area boundary) and increases at lower frequencies. Triangles represent the isolation measured between the LV/HV Return lines of the two PSUs.

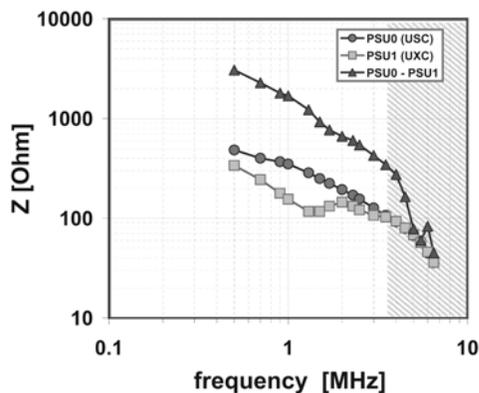


Figure 8: Electric isolation of PSUs belonging to the same PSM prototype (see text).

D. Efficiency

The ratio between the power supplied to the external load and the power required from the 48VP to this end is called efficiency. Figure 9 shows the measured values for an UXC prototype linked to a resistive load with 35m of LIC and 5m

of Al MSC cables. The performances are very good. The shaded area represents the typical PSU working range in the experiment, where the observed PSU efficiency is satisfactorily above 70%.

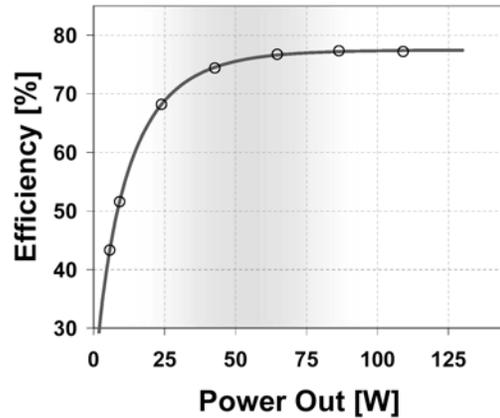


Figure 9: Efficiency curve of one PSU prototype (UXC).

In addition to the power necessary for the regulators, each PSU requires an additional $\sim 9W$ for the internal circuitry (48VS).

VIII. CONCLUSIONS

The powering scheme for the CMS silicon strip tracker has been defined and the procurement has started.

The detector is subdivided into 1944 groups of contiguous modules powered by a modular system of Power Supply Units featuring complex channels with low voltage and high voltage regulators. Power Supply Units are characterized by a very good electrical isolation of the channels and excellent electrical characteristics. They also feature full remote control, and a robust, hard-wired, safeguard system.

The power cables are Aluminum for the $\sim 5m$ long internal section and copper for the $\sim 40m$ external section, where a custom-designed "low impedance" cable, featuring low inductance and high capacitance, is used.

Performances achieved with these PSUs and cables on quasi-final detector setups, are on par with the ones obtained in single detector tests with short cables.

REFERENCES

- [1] CMS Coll. "The Compact Muon Solenoid, Technical Proposal", CERN/LHCC 94-38 (1994).
- [2] The CMS Tracker Coll. "The Tracker Project: Technical Design Report" CERN/LHCC 1998-006; "The Tracker Project: TDR Addendum" CERN/LHCC 2000-016.
- [3] M. J. French *et al.* "Design and results from the APV25, a deep sub-micron front-end chip for the CMS tracker" Nucl. Instr. and Meth. **A466** (2001) 359-365.
- [4] M. Costa communication.