The CMS ECAL Very Front End Electronics: Production and Tests

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1. Overview of the ECAL electronics
2. Very Front End card (VFE)
3. The VFE production schedule
4. Test program of the VFE
5. Power On test, Burn In and the Calibration test
6. First Super Module: results of the pre production
7. Conclusions
ECAL: system overview

ECAL BARREL

36 Super-modules for EB
61200 crystals with APD’s
1700 crystals per Supermodule
340 VFE per SM
12240 VFE in total
68 Trigger Towers

ECAL ENDCAP

4 Dee’s for EE
14648 crystals with VPT’s
734 VFE per Dee
2936 VFE in total
3662 crystals per Dee
156 Supercrystals per Dee
Trigger Tower / Super Crystal Electronics

Control Token Ring Board

Fiber Patch Panel

Fiber Patch Panel

Trigger Fiber(s)

Data Fiber

Front End Electronics

Voltage Distribution

Power in

INHIBIT

LV

FE

RE

VL

FE

ER

Fiber Patch Panel

Mother Board

Flexible Connection to APD’s / VPT’s

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Very Front End Electronics

Five read out channels per VFE

**Multi Gain Pre Amplifier (MGPA) has:**
- Gain ranges of 1, 6 and 12.
- Full scale signal 60 pC
- LVDS output signal to match ADC
- Linearity +/- 0.1%

**Quad Channel ADC (AD41240) has:**
- 12 bit, 40 MS/s
- Digital logic selects the highest unsaturated gain

**The LVDS_RX Buffer:**
- adapts the LVDS output of the AD41240 to the single ended inputs of the FE board

**All chips designed in 0.25 micron CMOS technology and radiation hard.**

<table>
<thead>
<tr>
<th>Chip</th>
<th>N chips per VFE</th>
<th>+2.5 V analog Current (mA)</th>
<th>+2.5 V digital Current (mA)</th>
<th>Sum 5 Channels (A)</th>
</tr>
</thead>
<tbody>
<tr>
<td>MGPA</td>
<td>5</td>
<td>240</td>
<td></td>
<td>1.20</td>
</tr>
<tr>
<td>AD41240</td>
<td>5</td>
<td>104</td>
<td>90</td>
<td>0.97</td>
</tr>
<tr>
<td>Buffer</td>
<td>5</td>
<td>24</td>
<td></td>
<td>0.12</td>
</tr>
</tbody>
</table>

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The Very Front End card

- LVDSMUX
- LVDS_RX buffer
- ADC 40 MHz 12bit (AD41240)
- MGPA
- 3 LVDS signals for the 3 gains
The Very Front End card

VFE also contains a DCU (Detector Control Unit) chip for the measurement of the APD leakage currents and the crystal temperature.

The guard ring keeps the housing at the GND potential.

fpBGA package for ADC
The Test program

The production test program is the following:

1. Automatic Optical Inspection (AOI) of the card done by the manufacturer.

2. Power-On test, including limited functional testing by the manufacturer; the required test setup is provided by the ECAL collaboration (ETHZ).

3. Burn-in test for three days at IN2P3 Lyon.

4. Calibration of the characteristics of each gain of each individual channel by measuring the gain, the pedestal, the noise and the linearity. Calibration of the leakage currents and temperature measurements.

- The production of the VFE cards started in summer 2004 with a pre-series of 420 pieces. This is followed by the production of 12000 pieces, about 2000 pieces/month, for the ECAL Barrel.
1. Power On test

LVPS 1
Auxiliary power: +5V

LVPS 2
VFE power: +5V

PC
NI DAQ 6013

Bar Code Reader

adapter

ERNI

ERNI

VFE
PCB under test

adapter

SAMTEC

LVR 2.5 V aux

LVR 3.3 V aux

LVR 2.5 V analog

LVR 2.5 V digital

LVR 2.5 V buffer

RS = 0.033 Ω

Rs

Rs

Rs

5 times: R_I_leak
1 times: R_T_sens

POTB

CLK

TTL LVDS

LED / Buffer

XILINX

RS232

RS232: 2Tx, 2Rx

DATA (8 x 14 bit)

RS232

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1. Power On Test

- VFE under test
- Barcode
- Power supply
- Low Voltage regulators and shunt resistors
- PC

[Image of a circuit board with labels for components]
1. Power On test

![Graph](image)

<table>
<thead>
<tr>
<th></th>
<th>2.5V analog</th>
<th>2.5V digital</th>
<th>2.5V buffer</th>
<th>total</th>
</tr>
</thead>
<tbody>
<tr>
<td>Average current in A</td>
<td>1.724</td>
<td>0.439</td>
<td>0.121</td>
<td>2.285</td>
</tr>
<tr>
<td>Standard deviation in A</td>
<td>0.007</td>
<td>0.007</td>
<td>0.005</td>
<td>0.007</td>
</tr>
</tbody>
</table>
2. Burn In Test

A burn in period of 3 days is proposed, at an elevated ambient temperature of 60°C ± 1°C:

- Burn-in will start with 50 cards from the pre-serie in order to accumulate statistics and confirm whether the burn-in period is appropriate.
- T is measured in several points of the rack.
- VFEs are powered with 2.5 V and the clock is provided.
- Current is monitored through shunt resistor.

Power Supply 3x 2.5V/200A

Control and PC interface via RS232

Temperature regulation: heating and cooling

Air mixer

10 lines of 15 VFE boards on the front and on the back
3. Calibration Test

Power Supplies

Low voltage regulators

3.3V

+2.5V

+/-5V

Temperature and leakage current simulation

Q input

Digital commands

Data

5x14 bit

Alterra

VFE

PCB under test

Clock & I2C

Charge generator

Bar Code

RS 232

RS 232

 Riotage
3. Calibration Test

Steps of the test are:
• Varying a charge pulse injection over the full dynamic range and get the response in ADC counts (5x 14 bit).
• Testing the temperature read out channel of the crystal.
• Simulating the leakage current of the APDs.
• Verifying the communication with the chips via the I2C bus.
• Measure the pedestal and noise in three different gains.

For the pre-production the set up was not fully operational so the first 420 cards were only functional tested.
3. Calibration Test

- Low voltage regulators
- Analog part of the board
- VFE under test
- Digital part of the board
- Q input
Temperature and leakage current results

Temperature read out channel of the crystal: a digital potentiometer changes its value to simulate a temperature variation on the crystals.

Leakage current of APD: the test board generates a current, through a DAC and a V to I converter to simulate a variation of the leakage current of the photo-detectors for the 5 channels of the VFE.

The Detector Control Unit (DCU) chip on the VFE reads the data of temperature and leakage current and sends them to the data acquisition system.
Pedestal and noise

- Noise distribution of 27 trigger tower (~700 channels) after installation in the SM

- Pedestal measured on one channel for 2 days to check its stability
Linearity

GAIN 6

CHARGE (picoCOULOMB)

N ADC count

GAIN 12

CHARGE (picoCOULOMB)

N ADC count

LINEARITY in GAIN 6

LINEARITY in GAIN 12

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Results from the pre-production

The test injects 30 samples of charge per each gain per each channel in the VFE. The charge varies between 0 and full-scale in gain 1.

On 420 VFE delivered:
- 3 failed power on test
- 35 failed the functional test:
  - 12 failed in CH. X GAIN Y
  - 4 failed in ALL CH.
  - 15 failed the temperature measurement
  - 4 were damaged on connectors during test and installation

- The functional test will be included in the Power On test
Summary

1. The production of 16000 cards is started with the fabrication of 420 cards of the pre-series in August.

2. The test set up has been successfully developed and built:
   - Power On test already powerful and it has still to be integrated with a functional test, in order to identify the majority of the failures directly at the manufacturer.
   - A pre-series of 50 VFE cards will burn in in first half of October.
   - Calibration test has to be finalized, it has been improved a lot in the last 2 months.

3. 7% of cards failed the tests … NEXT STEP IS TO INVESTIGATE ON THE FAILURES!

4. Performance of the cards in a Super-module very good with noise in the highest gain around 1.2 ADC counts and stable pedestal.
Each of them has the noise measured for 27 trigger towers. The parameters from the gaussian fit are:

- G1 mean = 0.5332 +/- 0.0014, sigma = 0.0338 +/- 0.0014
- G6 mean = 0.7248 +/- 0.0014, sigma = 0.0366 +/- 0.0014
- G12 mean = 1.091 +/- 0.002, sigma = 0.048 +/- 0.002

The sigma of the 3 distributions is:

- 0.36 +/- 0.04 ADC counts for Gain 12
- 0.30 +/- 0.05 ADC counts for Gain 6
- 0.25 +/- 0.03 ADC counts for Gain 1
A full Trigger Tower (25 channels) with 5 VFE, 1 FE board and 1 LVR board was tested with beam at PSI with $10^9$ p/cm$^2$/s for 2 hours:

- Data after irradiation OK
- Power consumption didn’t change (consistent for this technology)
- Baseline moves from 200 to 600 ADC counts after 2h irradiation, normal for this high radiation dose, and anyway it can be adjusted via a DAC in the MGPA chips

More information on the VFE behavior under irradiation we will have after the test beam of 1700 channels (a complete Super Module) in October.