LECC 2004, Boston USA

The Fast Merging Module (FMM) for readout status processing in CMS DAQ

Second and final prototype

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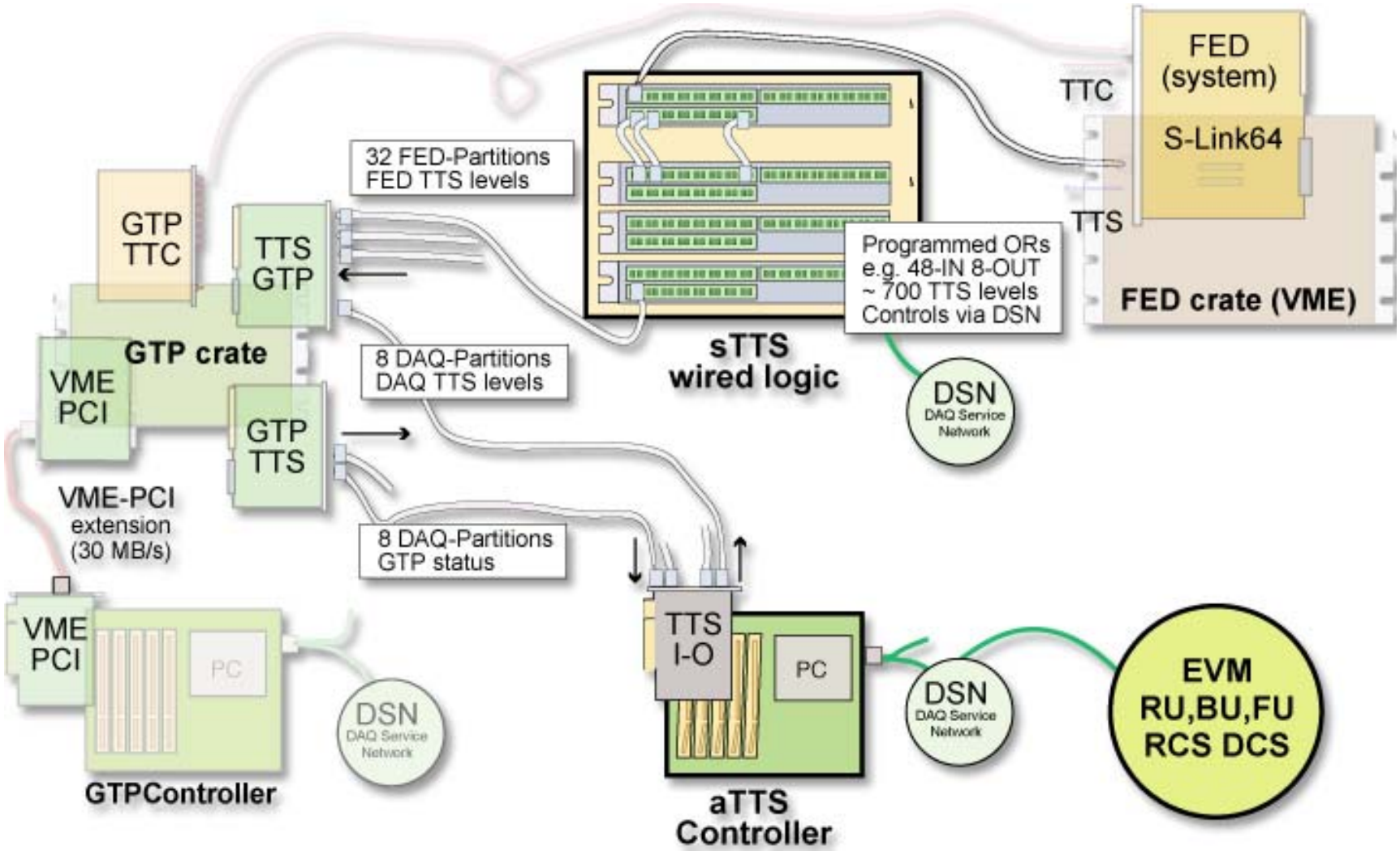
on behalf of the CMS DAQ group

Trigger Throttling System

- DAQ designed for 100 kHz maximum average trigger rate but…
  - Higher instantaneous trigger rate is possible (Poisson)
  - DAQ must not die by overflow if it happens!
    (and it will…)

- The TTS adapts the trigger pace with the DAQ processing capabilities
  - sTTS for small buffer devices (fast response time, hardware parts)
  - aTTS for large buffer devices (slow response time, software messages)

TTS global view



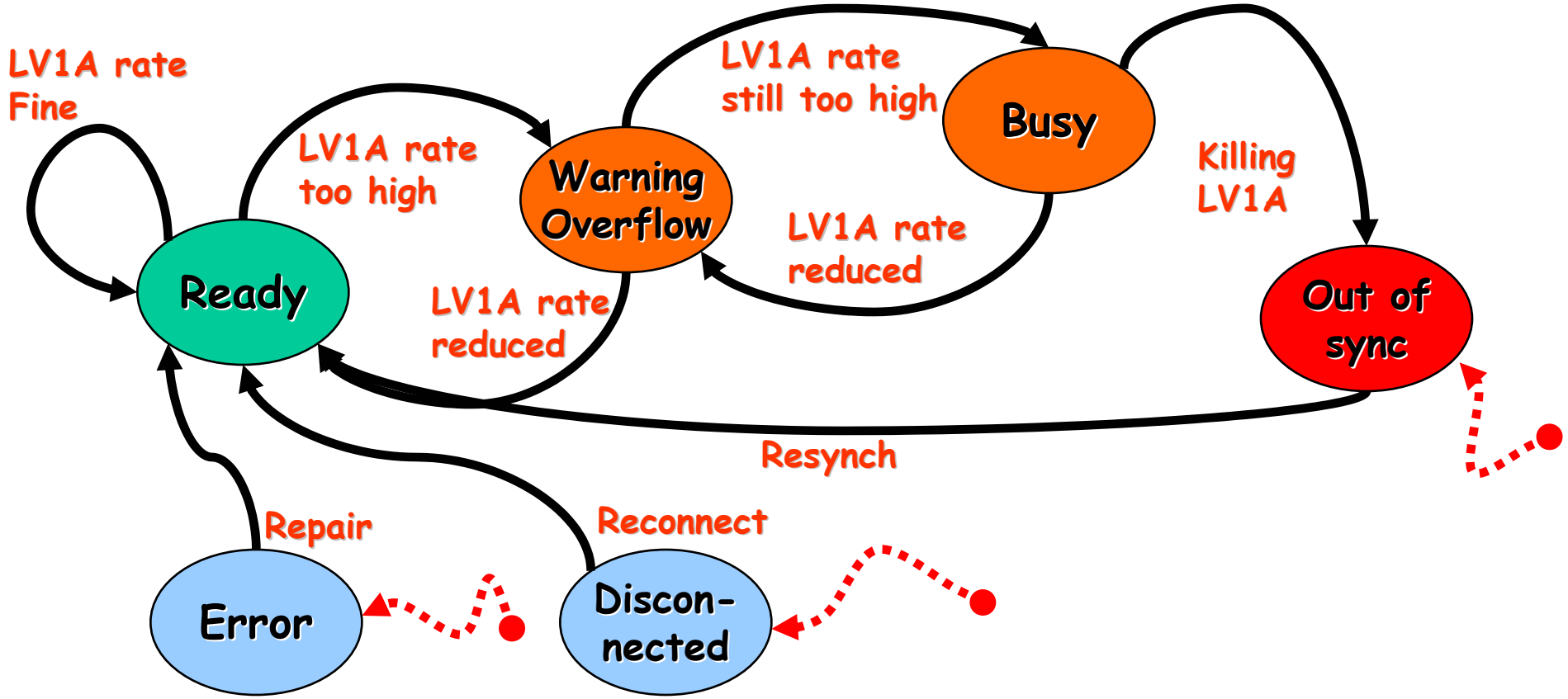
FMM and sTTS

- The FMM receives the current state of n devices and process them to form a single state that can be used by the TTS to modify (or not) the trigger rate

FMM design requirements

- Process (merges) the partition device states to form the detector partition status in a fast way (~100 ns)
- Monitors the dead time introduced by the partition devices
  - Identification of (potential) pathologic FEDs
- Keeps a history memory of the state changes
  - Allows to monitor the device states or playback for detailed analysis
- Generates input patterns for Trigger Control System
- Is also the output card for the aTTS

Partition device state machine



State encoding and priorities

- States are provided on 4 bits: max transition rate = 40 MHz but we expect ~100 Hz !
  - 6 states defined for FEDs using 7 values
  - 9 values “reserved”

- If a FED is in any reserved state, the FMM propagates a new state: illegal

- FEDs linked to an FMM can be in a different state: state priorities (decreasing order) are as follows:
  - Disconnect
  - Error
  - Out_of_sync
  - Busy
  - Overflow
  - Illegal
  - Ready

FMM features

- 24 connectors with LEDs, configurable as input or output at soldering time
  - Allows to deal with 1 or 2 partitions and enable the card to be aTTS output
- Mask register
  - a pathologic FED will not disturb the system once detected and identified
- Hardware dead-time monitors
  - early detection of potential problem
- Cyclic history memory: only state transitions are recorded with time tag
  - 2 MB/128 k transitions (16 bytes/transitions)
  - Time tag resolution/range: 25 ns/40 bit (~7.6 hours)
- System clock at 80 MHz, Inputs sampled at 80 MHz but processed at 40 MHz
- History data can be pushed directly to host PC (“ala” FEDKIT)
- FPGA configuration files can be updated from PCI and on-board JTAG

Processing/Merging functions

- Depending on the states
  - Logical OR
  - Arithmetic sum & threshold

- Can be modified on request thanks to the on-board FPGA

FMMs in CMS

- FMM with 20 inputs max, 4 outputs: modulable in 20->1, 2x [10->1] (½)
- Double outputs are needed on the last FMM in the tree
- In this case, 8 FMMs per crate, one slot for reset distribution, 6 crates total

Detector (# of FEDs)	Partition (# of FEDs)	# of FMM per partition	# of FMM per detector
Pixel (38)	Barrel (32) Forward (6)	2+ ½ ½	3
Tracker (440)	Inner (114) Outer (134) Endcap+(96) Endcap-(96)	6+ ½ 7+ ½ 5+ ½ 5+ ½	25
Preshower (~50)	SE+ (25) SE- (25)	2+ ½ 2+ ½	5
ECAL (54)	EB+ (18) EB- (18) EE+ (9) EE- (9)	1 1 ½ ½	3
HCAL (32)	HB+ (6) HB- (6) HE+ (5) HE- (5) HO+ (5) HO- (5)	½ ½ ½ ½ ½ ½	3

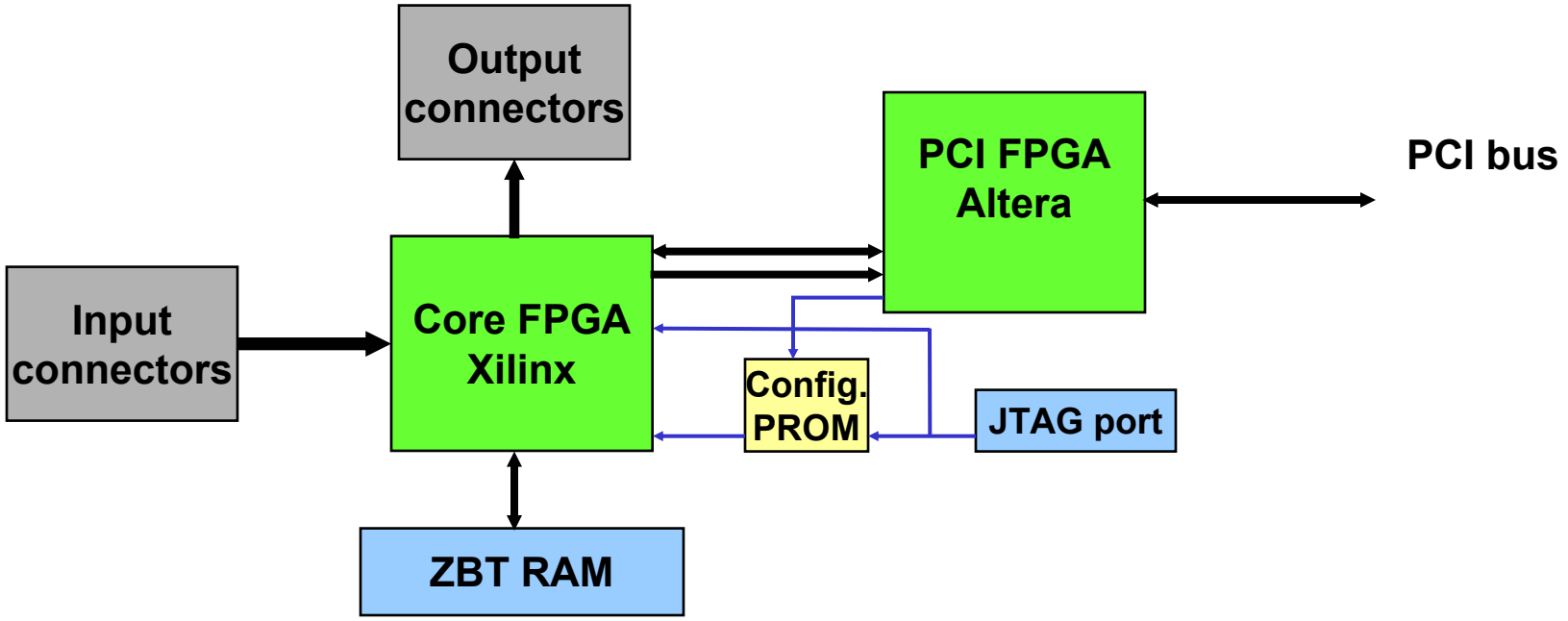
Detector (# of FEDs)	Partition (# of FEDs)	# of FMM per partition	# of FMM per detector
Mu-DT (5)	Barrel+ Barrel-	½ ½	1
Mu-RPC (6)	Barrel+ Barrel- Endcap+ Endcap-	½ ½ ½ ½	2
Mu-CSC (8)	Endcap+ Endcap-	½ ½	1
Calo-trig Glob–mu Glob-trig	Na Na Na	½ ½ ½	2
Mu-trig	CSC-trig DT trig	½ ½	1
Total	31 (636)		46

History capacity and BW

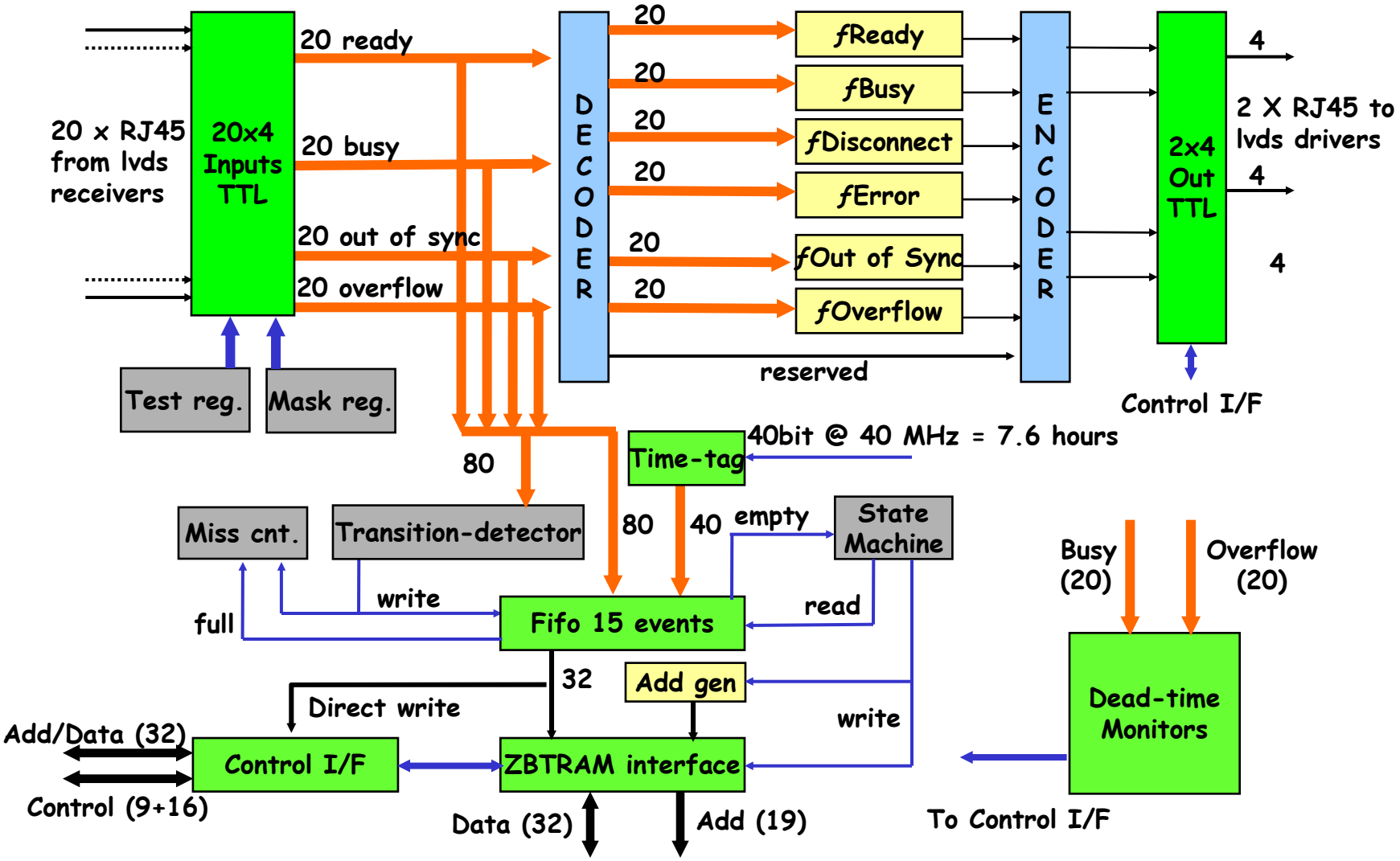
- Each transition generates 80 bits (4 x 20) + 40 bits (time tag) or 16 bytes
- 1MB of memory is 64K transitions
- Worst case bandwidth on PCI backplane is 12MB/sec (with 8 FMMs per crate)
- External memory of 2 MB is chosen

Transition rate (all inputs)	History length per MB (second)	Data rate to the history memory
10Hz	65000 (1.8 hour)	160 bytes/sec
100Hz	655 (~11 min)	1.5 kB/sec
1kHz Worries…	65	15 kB/sec
10kHz Pathologic…	6.5	156 kB/sec
100kHz Very Pathologic…	0.65	1.5 MB/sec

Block diagram



FPGA block diagram (20 inputs)

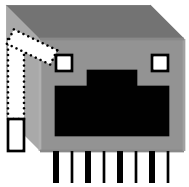


FMM implementation

- Compact PCI 6U double width form factor
- TTS connector allows standard RJ45 network cables
  - At 40 MHz transition rate, LVDS drivers allows hundreds meter of cable length
- PCI control interface re-used from FRL design
- Same location of JTAG port
  - enables the re-use of FRL testbed

TTS connector

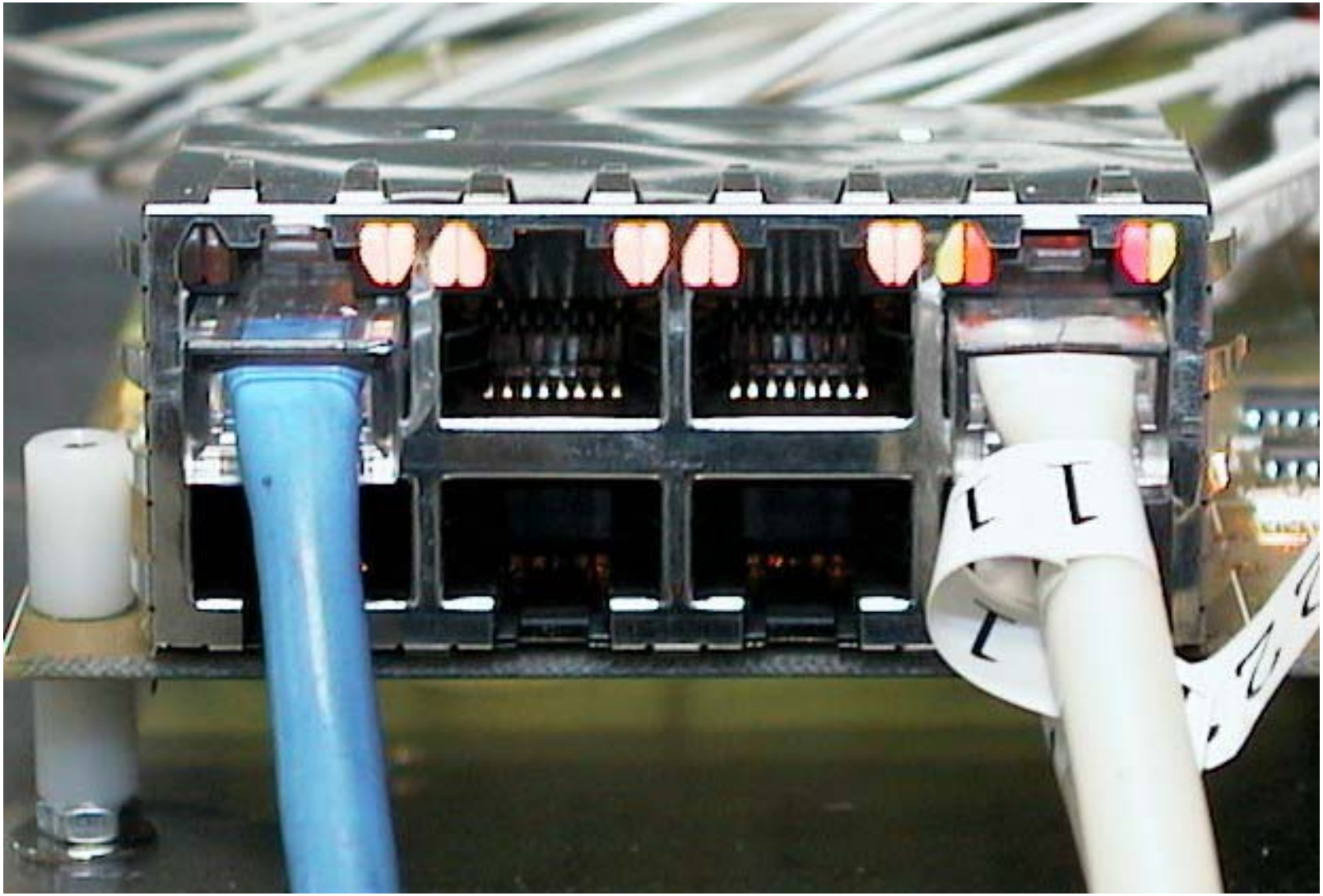
- Standard RJ45 connector is used
  - Low cost, reliable, small footprint, high-density front panel



•Socket with light-guides for bi-color LEDs

- Pin 1 -busy
- Pin 2 +busy
- Pin 3 -ready
- Pin 4 +overflow warning
- Pin 5 -overflow warning
- Pin 6 + ready
- Pin 7 -out of synch
- Pin 8 +out of synch

I/O block



Core FPGA

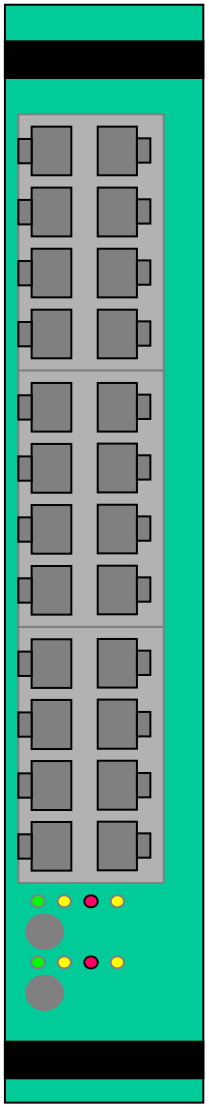
- I/O count: ~224 pins
  - 24 TTS inputs/outputs: 96 pins
  - Control I/F (32 A/D+misc): 48 pins
  - Memory I/F (32D/20A): ~60 pins
  - Misc. (Leds, prom, reset…) ~20 pins

- Logic gates: ~ 5000 FF (estimates based on proto1)
  - Memory I/F: 300FF, 100 LUT
  - Logic: ~750FF, ~875 LUT
  - Monitors (raw counters): 3200FF, (4 states monitored)
  - Pattern injection logic: ~700FF (comfortable…)

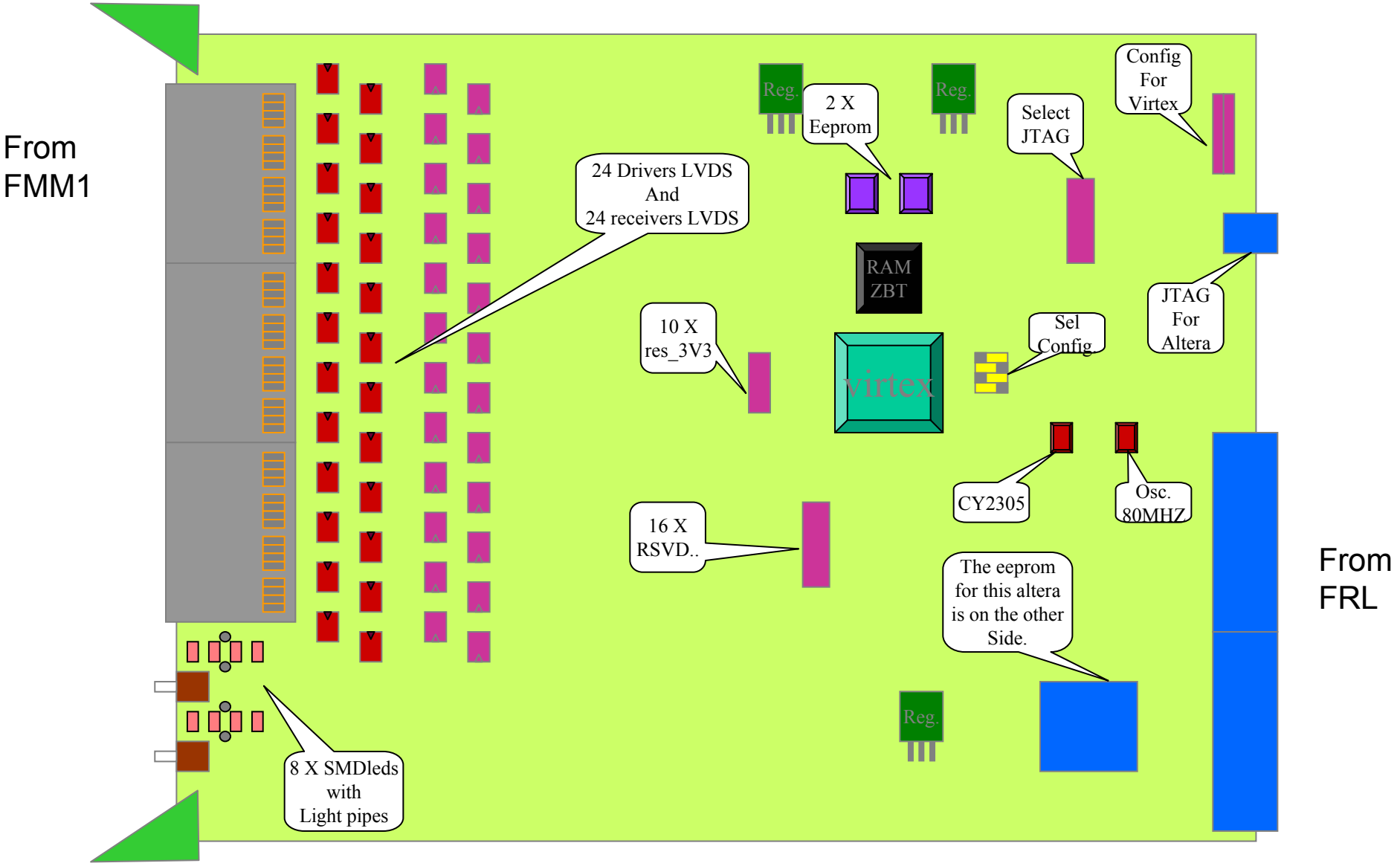
- Xilinx XC2VP7-5FG456 is selected: 248 I/Os, 10000 FF

Front Panel

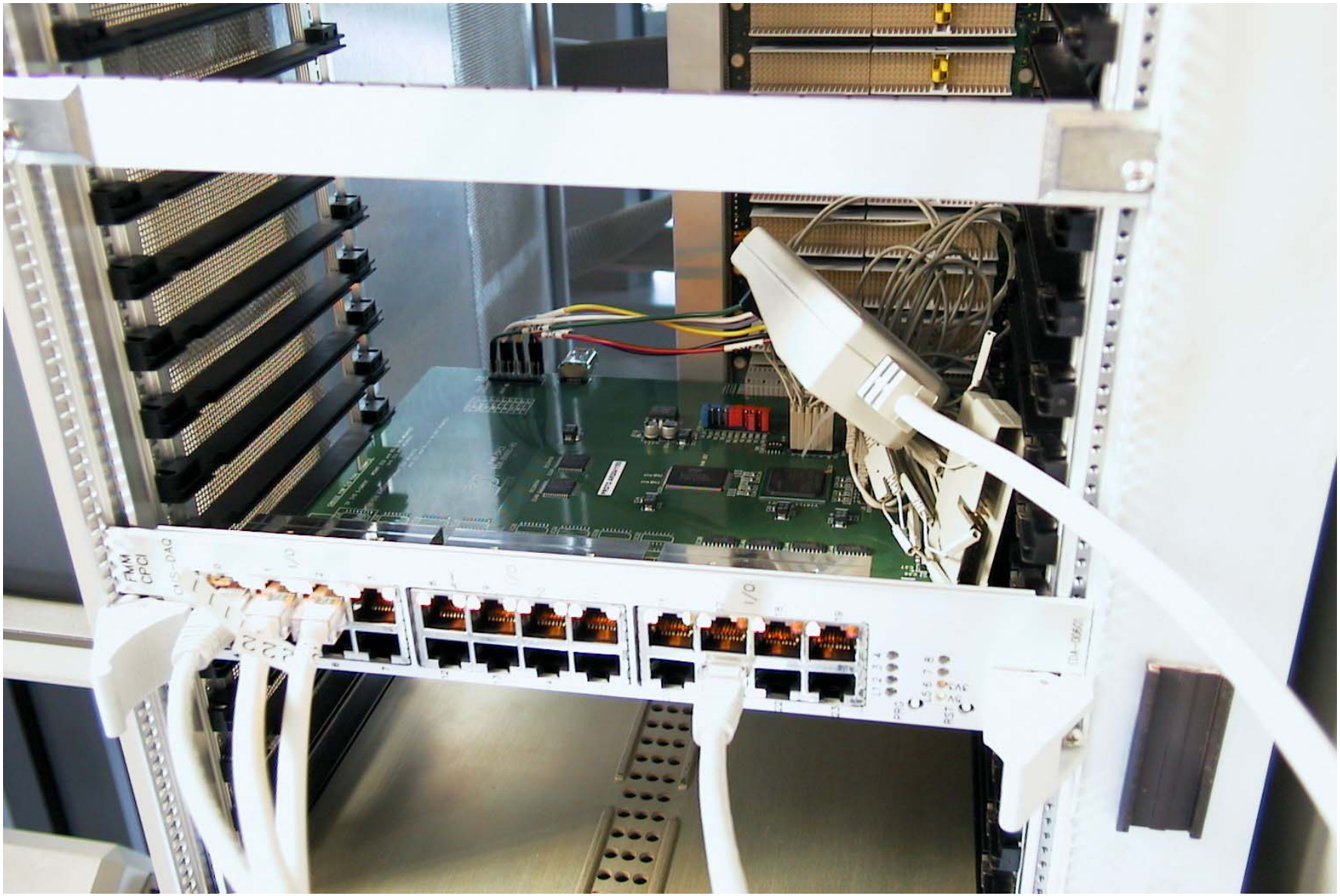
- 2U wide , 6U height Compact PCI
- Same format as FRL
- 24 TTS I/O
- 8 status leds
- 2 push-buttons: reset and reprog Core FPGA



PCB layout


From FMM1
24 Drivers LVDS And 24 receivers LVDS
Reg.
2 X Eeprom
Reg.
Select JTAG
Config For Virtex
RAM ZBT
JTAG For Altera
10 X res_3V3
virtex
Sel Config.
CY2305
Osc. 80MHZ
16 X RSVD..
The eeprom for this altera is on the other Side.
Reg.
8 X SMDleds with Light pipes
From FRL

Prototype picture



Status

- 2 PCB produced and populated
- Register/memory tests passed
- Inputs/Outputs tested “one by one” at computer speed

- Wait after a “helper module” to stress all inputs at 40 MHz

- After… we enter production !

- Production test software being debugged

End

What next after first prototype…

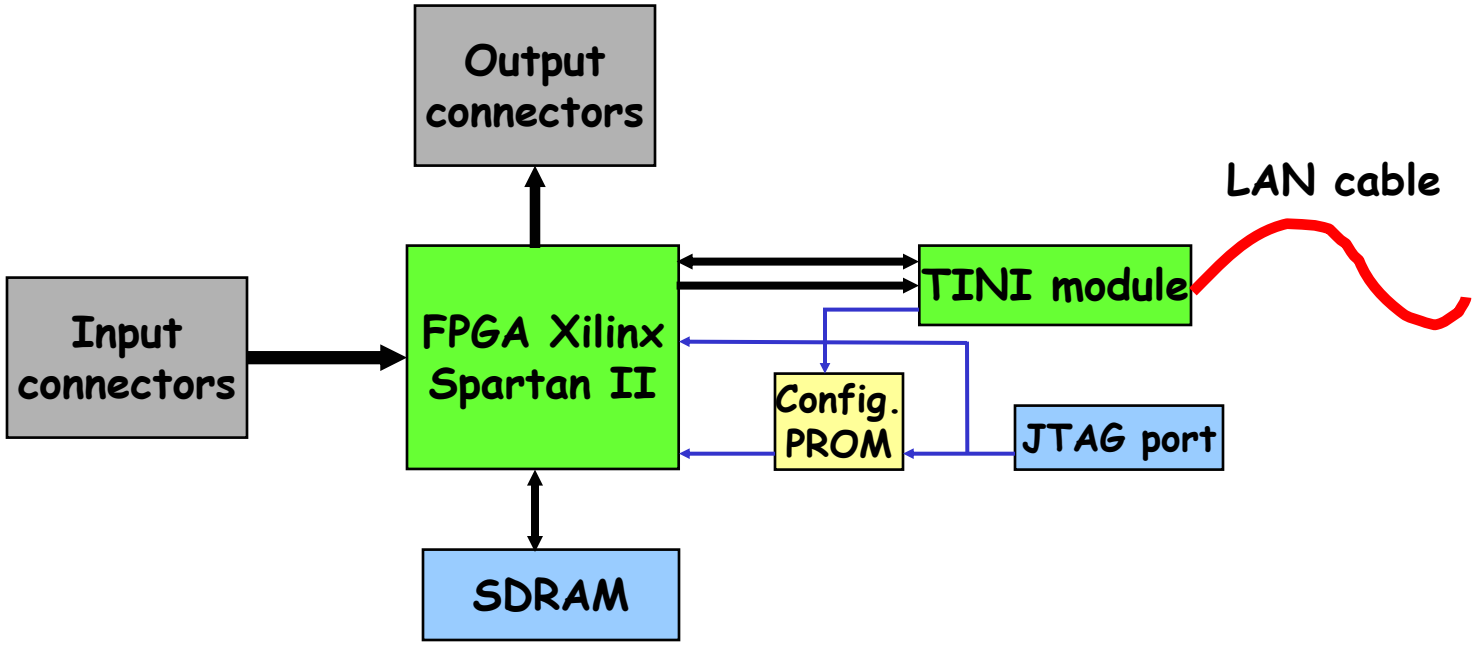
- Design the final prototype with
  - PCI interface
  - Compact PCI form factor (6 or 9U)
    - See if 32 inputs is optimal
  - Implement hardware monitoring engines

First prototype

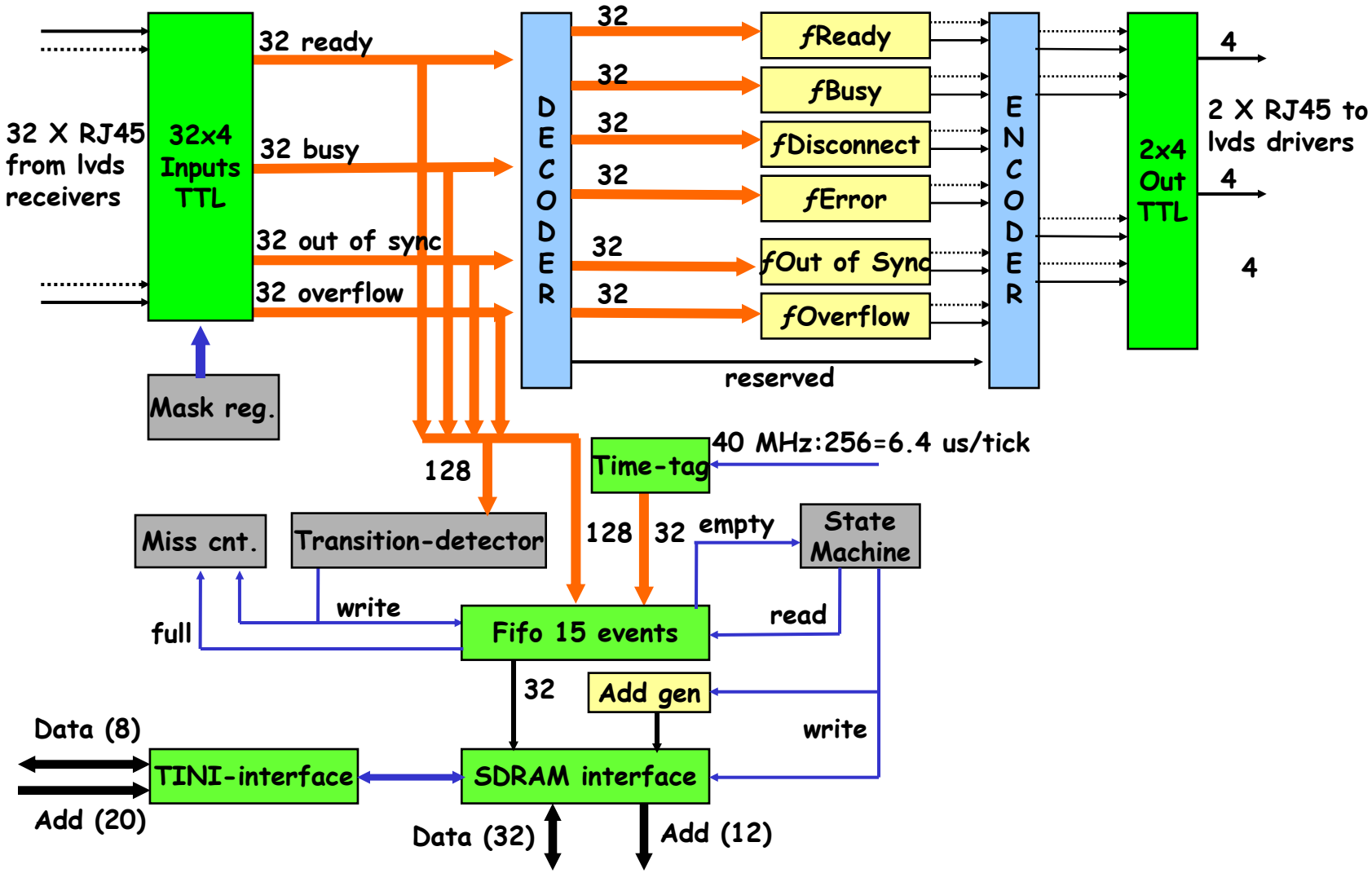
- Validation of FMM concept
- 19-inch rack mounted 1U box
- A Xilinx Spartan II is the core FPGA
- Standard UTP5 Input connector running LVDS levels
- External SDRAM for history memory
- TINI module (WEB) used as control interface
- No deadtime monitor engine

- Core FPGA functions validated

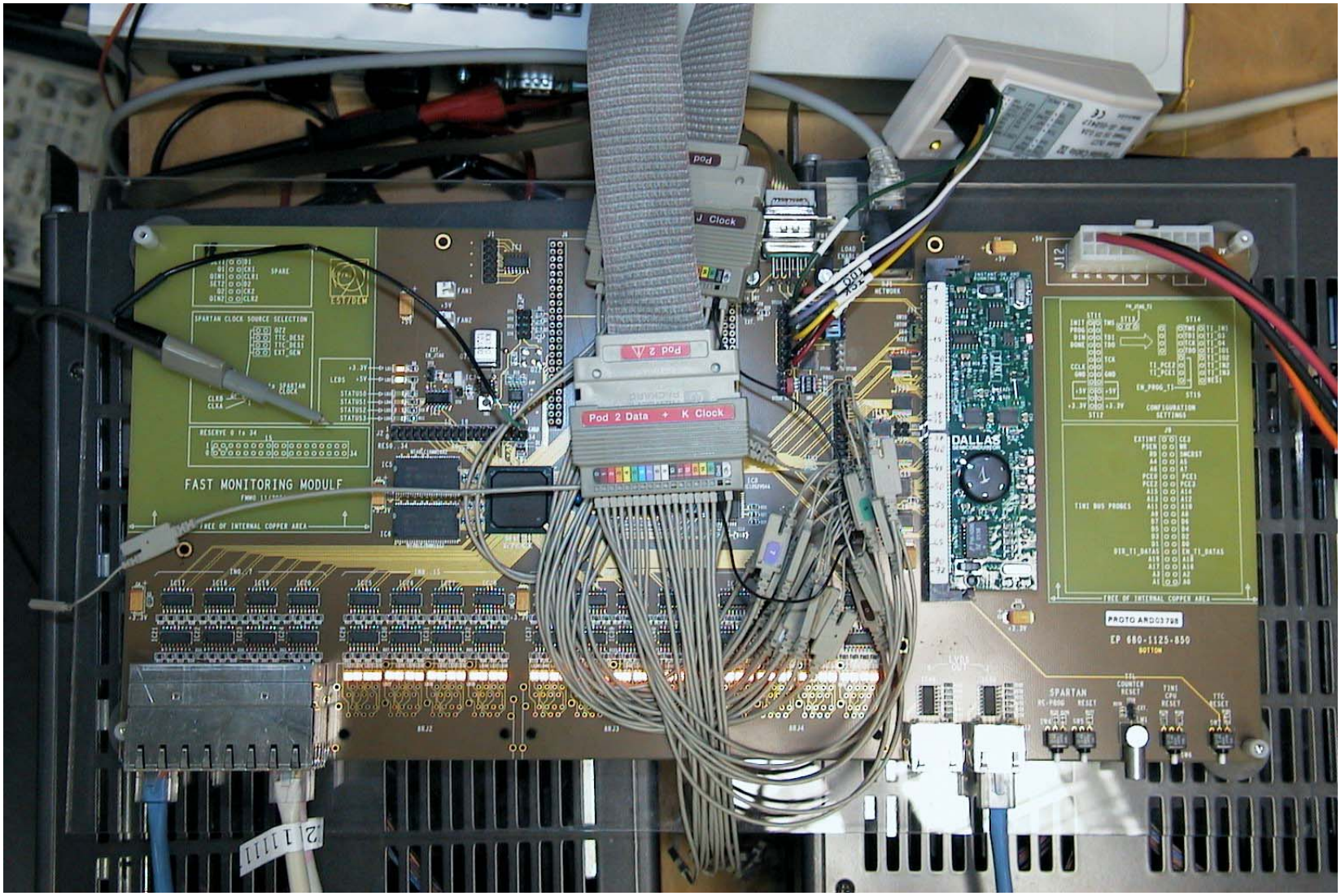
First proto block diagram



First proto FPGA block diagram



First prototype picture



First prototype performances

- History memory
  - 16 MB/840 k transitions (20 bytes/transitions)
  - Time tag resolution/range: 6.4 us/32 bit (~7.6 hours)

- Propagation time: 100 ns (4 clock cycles @ 25 ns)