The Fast Merging Module (FMM) for readout status processing in CMS DAQ

Second and final prototype

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on behalf of the CMS DAQ group
• DAQ designed for 100 kHz maximum average trigger rate but…
  – Higher instantaneous trigger rate is possible (Poisson)
  – DAQ must not die by overflow if it happens!
  (and it will…)

• The TTS adapts the trigger pace with the DAQ processing capabilities
  – sTTS for small buffer devices (fast response time, hardware parts)
  – aTTS for large buffer devices (slow response time, software messages)
• The FMM receives the current state of n devices and process them to form a single state that can be used by the TTS to modify (or not) the trigger rate
FMM design requirements

• Process (merges) the partition device states to form the detector partition status in a fast way (~100 ns)

• Monitors the dead time introduced by the partition devices
  – Identification of (potential) pathologic FEDs

• Keeps a history memory of the state changes
  – Allows to monitor the device states or playback for detailed analysis

• Generates input patterns for Trigger Control System

• Is also the output card for the aTTS
State encoding and priorities

• States are provided on 4 bits: max transition rate = 40 MHz but we expect ~100 Hz!
  – 6 states defined for FEDs using 7 values
  – 9 values “reserved”

• If a FED is in any reserved state, the FMM propagates a new state: illegal

• FEDs linked to an FMM can be in a different state: state priorities (decreasing order) are as follows:
  – Disconnect
  – Error
  – Out_of_sync
  – Busy
  – Overflow
  – Illegal
  – Ready
FMM features

- 24 connectors with LEDs, configurable as input or output at soldering time
  - Allows to deal with 1 or 2 partitions and enable the card to be aTTS output
- Mask register
  - a pathologic FED will not disturb the system once detected and identified
- Hardware dead-time monitors
  - early detection of potential problem
- Cyclic history memory: only state transitions are recorded with time tag
  - 2 MB/128 k transitions (16 bytes/transition)
  - Time tag resolution/range: 25 ns/40 bit (~7.6 hours)
- System clock at 80 MHz, Inputs sampled at 80 MHz but processed at 40 MHz
- History data can be pushed directly to host PC ("ala" FEDKIT)
- FPGA configuration files can be updated from PCI and on-board JTAG
Processing/Merging functions

• Depending on the states
  – Logical OR
  – Arithmetic sum & threshold

• Can be modified on request thanks to the on-board FPGA
FMMs in CMS

- FMM with 20 inputs max, 4 outputs: modulable in 20->1, 2x [10->1] (½)
- Double outputs are needed on the last FMM in the tree
- In this case, 8 FMMs per crate, one slot for reset distribution, 6 crates total

<table>
<thead>
<tr>
<th>Detector (# of FEDs)</th>
<th>Partition (# of FEDs)</th>
<th># of FMM per partition</th>
<th># of FMM per detector</th>
</tr>
</thead>
<tbody>
<tr>
<td>Pixel (38)</td>
<td>Barrel (32) Forward (6)</td>
<td>2+ ½ ½</td>
<td>3</td>
</tr>
<tr>
<td>Tracker (440)</td>
<td>Inner (114) Outer (134) Endcap+(96) Endcap-(96)</td>
<td>6+ ½ 7+ ½ 5+ ½ 5+ ½</td>
<td>25</td>
</tr>
<tr>
<td>Preshower (~50)</td>
<td>SE+ (25) SE- (25)</td>
<td>2+ ½ 2+ ½</td>
<td>5</td>
</tr>
<tr>
<td>ECAL (54)</td>
<td>EB+ (18) EB- (18) EE+ (9) EE- (9)</td>
<td>1 1 ½ ½ ½</td>
<td>3</td>
</tr>
<tr>
<td>HCAL (32)</td>
<td>HB+ (6) HB- (6) HE+ (5) HE- (5) HO+ (5) HO- (5)</td>
<td>½ ½ ½ ½ ½ ½</td>
<td>3</td>
</tr>
</tbody>
</table>

<table>
<thead>
<tr>
<th>Detector (# of FEDs)</th>
<th>Partition (# of FEDs)</th>
<th># of FMM per partition</th>
<th># of FMM per detector</th>
</tr>
</thead>
<tbody>
<tr>
<td>Mu-DT (5)</td>
<td>Barrel+ Barrel-</td>
<td>½ ½</td>
<td>1</td>
</tr>
<tr>
<td>Mu-RPC (6)</td>
<td>Barrel+ Barrel- Endcap+ Endcap-</td>
<td>½ ½ ½ ½</td>
<td>2</td>
</tr>
<tr>
<td>Mu-CSC (8)</td>
<td>Endcap+ Endcap-</td>
<td>½ ½</td>
<td>1</td>
</tr>
<tr>
<td>Calo-trig Glob–mu Glob-trig</td>
<td>Na Na Na Na</td>
<td>½ ½ ½ ½</td>
<td>2</td>
</tr>
<tr>
<td>Mu-trig CSC-trig DT trig</td>
<td></td>
<td>½ ½</td>
<td>1</td>
</tr>
<tr>
<td>Total</td>
<td>31 (636)</td>
<td></td>
<td>46</td>
</tr>
</tbody>
</table>
History capacity and BW

- Each transition generates 80 bits (4 x 20) + 40 bits (time tag) or 16 bytes
- 1MB of memory is 64K transitions
- Worst case bandwidth on PCI backplane is 12MB/sec (with 8 FMMs per crate)
- External memory of 2 MB is chosen

<table>
<thead>
<tr>
<th>Transition rate (all inputs)</th>
<th>History length per MB (second)</th>
<th>Data rate to the history memory</th>
</tr>
</thead>
<tbody>
<tr>
<td>10Hz</td>
<td>65000 (1.8 hour)</td>
<td>160 bytes/sec</td>
</tr>
<tr>
<td>100Hz</td>
<td>655 (~11 min)</td>
<td>1.5 kB/sec</td>
</tr>
<tr>
<td>1kHz</td>
<td>65</td>
<td>15 kB/sec</td>
</tr>
<tr>
<td>10kHz</td>
<td>6.5</td>
<td>156 kB/sec</td>
</tr>
<tr>
<td>100kHz</td>
<td>0.65</td>
<td>1.5 MB/sec</td>
</tr>
</tbody>
</table>
FPGA block diagram (20 inputs)

20 x RJ45 from lvds receivers

20 ready
20 busy
20 out of sync
20 overflow

20 x RJ45 to lvds drivers

40 bit @ 40 MHz = 7.6 hours

Busy (20)
Overflow (20)

Control I/F

Miss cnt.
Transition-detector

Fifo 15 events

Time-tag

State Machine

Add/Data (32)
Control (9+16)

Control I/F

ZBTRAM interface

Data (32)
Add (19)

Add gen

direct write

write

read

full

Monitors

Control I/F

Reserved

fReady
fBusy
fDisconnect
fError
fOut of Sync
fOverflow

Control I/F

Direct write

write

write

write

write
FMM implementation

- Compact PCI 6U double width form factor

- TTS connector allows standard RJ45 network cables
  - At 40 MHz transition rate, LVDS drivers allows hundreds meter of cable length

- PCI control interface re-used from FRL design

- Same location of JTAG port
  - enables the re-use of FRL testbed
**TTS connector**

- Standard RJ45 connector is used
  - Low cost, reliable, small footprint, high-density front panel

- Socket with light-guides for bi-color LEDs

- Pin 1 -busy
- Pin 2 +busy
- Pin 3 -ready
- Pin 4 +overflow warning
- Pin 5 -overflow warning
- Pin 6 +ready
- Pin 7 -out of synch
- Pin 8 +out of synch
I/O block
Core FPGA

- I/O count: ~224 pins
  - 24 TTS inputs/outputs: 96 pins
  - Control I/F (32 A/D+misc): 48 pins
  - Memory I/F (32D/20A): ~60 pins
  - Misc. (Leds, prom, reset…): ~20 pins

- Logic gates: ~5000 FF (estimates based on proto1)
  - Memory I/F: 300FF, 100 LUT
  - Logic: ~750FF, ~875 LUT
  - Monitors (raw counters): 3200FF, (4 states monitored)
  - Pattern injection logic: ~700FF (comfortable…)

- Xilinx XC2VP7-5FG456 is selected: 248 I/Os, 100k FF
• 2U wide, 6U height Compact PCI
• Same format as FRL
• 24 TTS I/O
• 8 status leds
• 2 push-buttons: reset and reprog Core FPGA
PCB layout

From FMM1:
- 8 X SMDleds with Light pipes
- 24 Drivers LVDS and 24 receivers LVDS
- 10 X res_3V3
- 16 X RSVD..

From FRL:
- 2 X Eeprom
- Select JTAG
- Config For Virtex
- JTAG For Altera
- The eeprom for this altera is on the other Side.
- CY2305
- Osc. 80MHZ

Reg.

Virtex

RAM

ZBT

Select Config

For Virtex

For Altera
Prototype picture
• 2 PCB produced and populated
• Register/memory tests passed
• Inputs/Outputs tested “one by one” at computer speed

• Wait after a “helper module” to stress all inputs at 40 MHz

• After… we enter production!

• Production test software being debugged
What next after first prototype...

• Design the final prototype with
  – PCI interface
  – Compact PCI form factor (6 or 9U)
    • See if 32 inputs is optimal
  – Implement hardware monitoring engines
First prototype

- Validation of FMM concept
- 19-inch rack mounted 1U box
- A Xilinx Spartan II is the core FPGA
- Standard UTP5 Input connector running LVDS levels
- External SDRAM for history memory
- TINI module (WEB) used as control interface
- No deadtime monitor engine

- Core FPGA functions validated
First proto block diagram

- **Input connectors**
- **Output connectors**
- **FPGA Xilinx Spartan II**
- **TINI module**
- **Config. PROM**
- **JTAG port**
- **SDRAM**
- **LAN cable**
First proto FPGA block diagram

32 X RJ45 from lvds receivers

32 ready
32 busy
32 out of sync
32 overflow

Mask reg.

32x4 Inputs TTL

32 ready
32 busy
32 out of sync
32 overflow

32 X RJ45 to lvds drivers

fReady
fBusy
fDisconnect
fError
fOut of Sync
fOverflow

reserved

2x4 Out TTL

40 MHz:256=6.4 us/tick

Miss cnt.

Transition-detector

Time-tag

Fifo 15 events

Add gen

Miss cnt.

Add (20)

TINI-interface

SDRAM interface

Data (8)

Add (32)

Data (32)

Add (12)

write

read

write
First prototype picture
First prototype performances

• History memory
  – 16 MB/840 k transitions (20 bytes/transition)
  – Time tag resolution/range: 6.4 us/32 bit (~7.6 hours)

• Propagation time: 100 ns (4 clock cycles @ 25 ns)